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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-2tq100

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

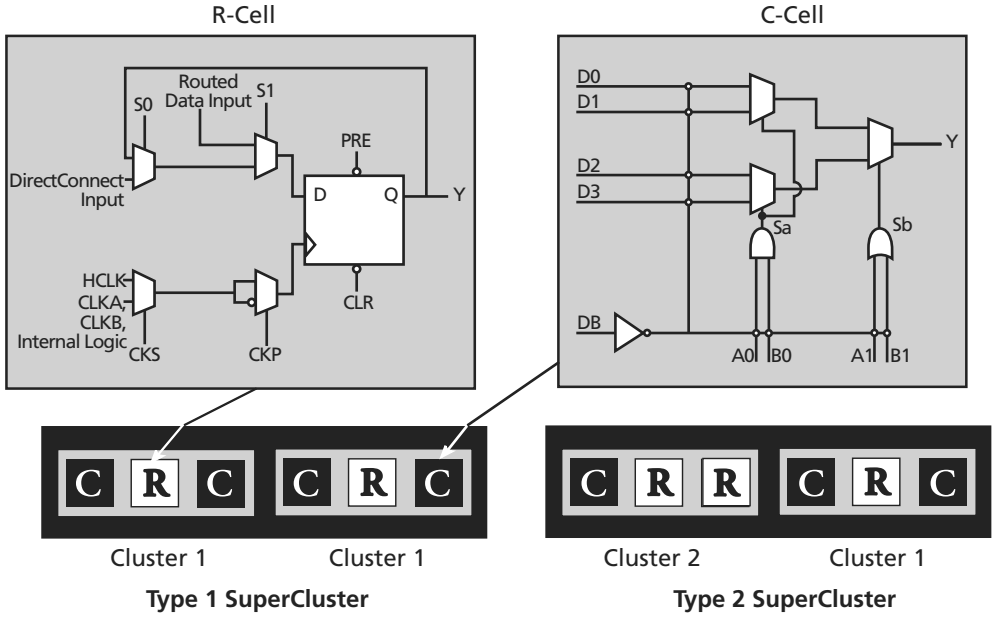


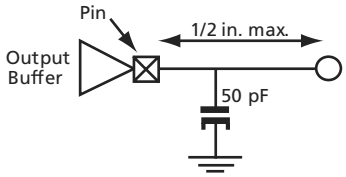
Figure 1-4 • **Cluster Organization**

Table 2-8 • **AC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44	–	mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ [3]	–	–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95	–	mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ [1, 3]	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ [3]	–	206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

θ_{JA} = Junction-to-air thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_C = Ambient temperature

P = total power dissipated by the device

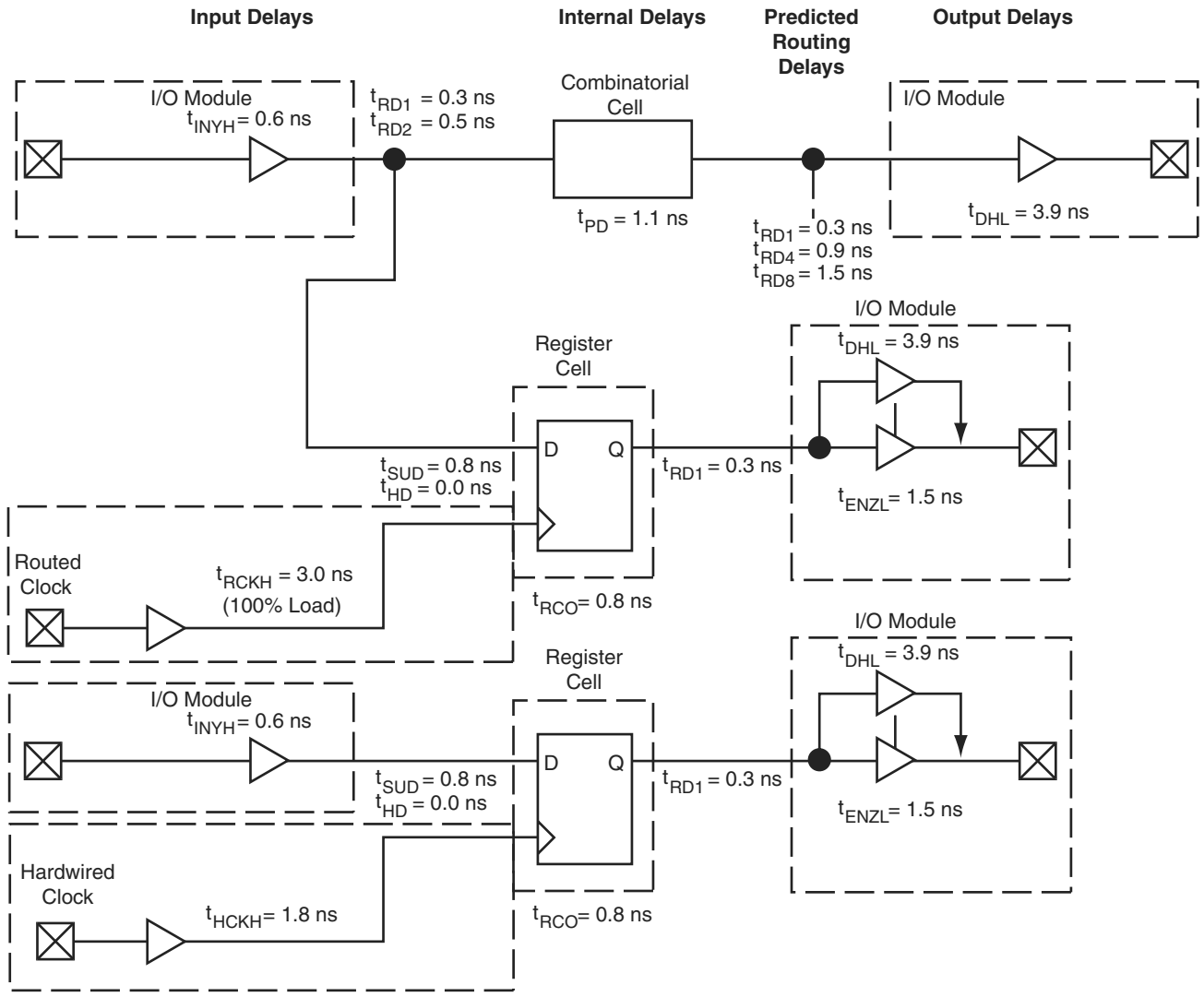
Table 2-12 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{JC}	θ_{JA}			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

1. *The A54SX08A PQ208 has no heat spreader.*
2. *The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.*

SX-A Timing Model



Note: **Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route.*

Figure 2-3 • **SX-A Timing Model**

Sample Path Calculations

Hardwired Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH}$
= 0.6 + 0.3 + 0.8 - 1.8 = – 0.1 ns

Clock-to-Out (Pad-to-Pad) = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 ns

Routed Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH}$
= 0.6 + 0.3 + 0.8 - 3.0 = –1.3 ns

Clock-to-Out (Pad-to-Pad) = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 ns

Table 2-16 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.3		1.5		1.7		2.6	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.5		0.5		0.8	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		1.9	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.2		1.3		1.6		2.2	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9		1.1		1.5	ns

Table 2-31 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-32 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing [2,3]												
t_{DLH}	Data-to-Pad Low to High		3.3		3.8		4.2		5.0		7.0	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		11.1		12.8		14.5		17.0		23.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.3		3.8		4.2		5.0		7.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.2		3.8		5.3	ns
d_{TLH}[4]	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[4]	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[4]	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-35 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[2]												
t_{PD}	Internal Array Module		1.0		1.1		1.3		1.5		2.0	ns
Predicted Routing Delays[3]												
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{RD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{RD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{RD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{RD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{RD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.1		1.5	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.3	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		1.0		1.1		1.3		1.7	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.7		0.7		0.9		1.2	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.2		1.3		1.5		2.1	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-38 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-38 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-40 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.3		2.7		3.0		3.6		5.0	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.2		3.8		5.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.0		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		3.2		3.7		4.2		5.0		6.9	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.7		4.2		4.9		6.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		10.3		11.9		13.5		15.8		22.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.2		3.7		4.2		5.0		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.7		4.2		4.9		6.9	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

208-Pin PQFP				
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V_{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

329-Pin PBGA	
Pin Number	**A54SX32A Function**
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC*	I/O
T26	NC*	I/O
U1	I/O	I/O
U2	V_{CCI}	V_{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V_{CCI}	V_{CCI}
U26	I/O	I/O
V1	NC*	I/O

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
V2	NC*	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V_{CCA}	V_{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC*	I/O
V26	NC*	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V_{CCA}	V_{CCA}
W24	I/O	I/O
W25	NC*	I/O
W26	NC*	I/O
Y1	NC*	I/O
Y2	NC*	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC*	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V_{CCI}	V_{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: **These pins must be left floating on the A54SX32A device.*

Previous Version	Changes in Current Version (v5.3)	Page
v4.0 (continued)	Table 2-12 was updated.	2-11
	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The ""Clock Resources" section"was updated	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.