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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-2tqg100i

Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

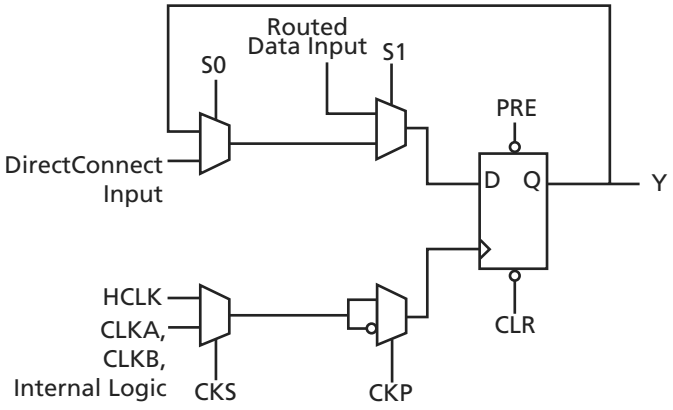

Figure 1-2 • **R-Cell**

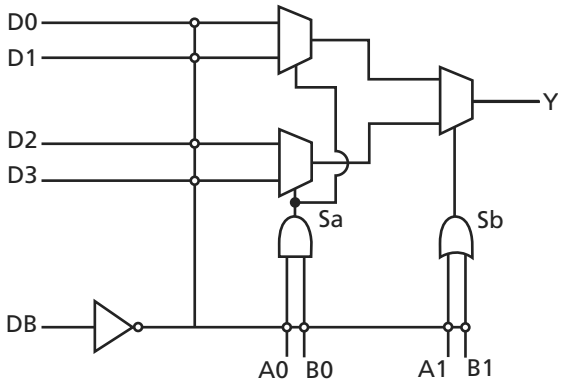

Figure 1-3 • **C-Cell**

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

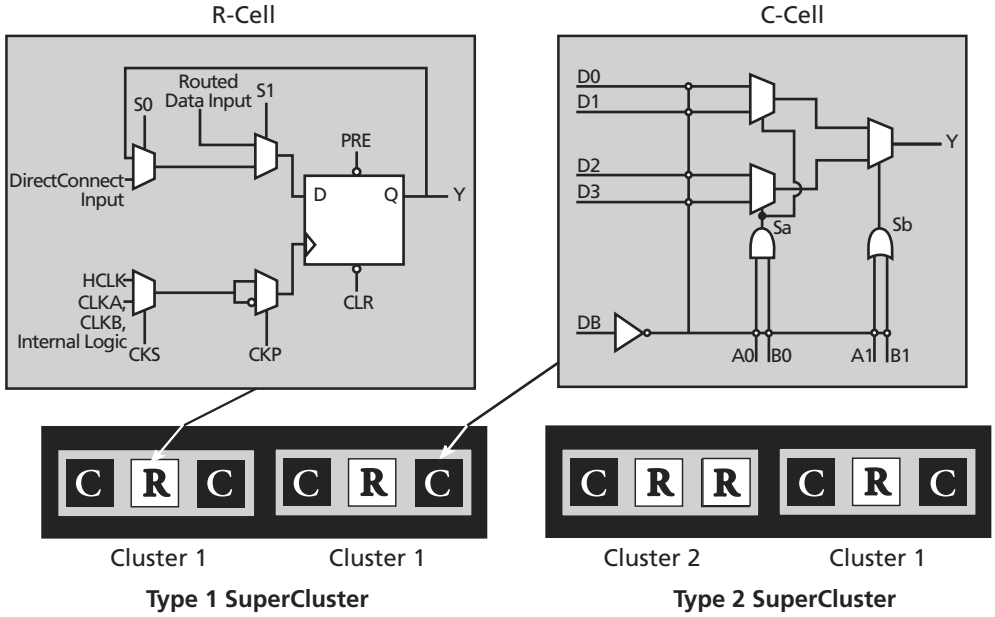

Figure 1-4 • **Cluster Organization**

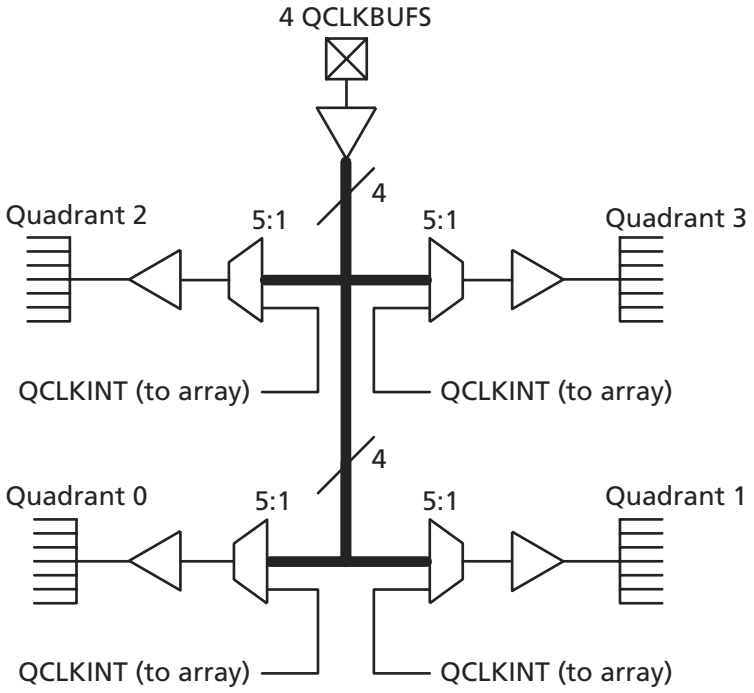

Figure 1-9 • **SX-A QCLK Architecture**

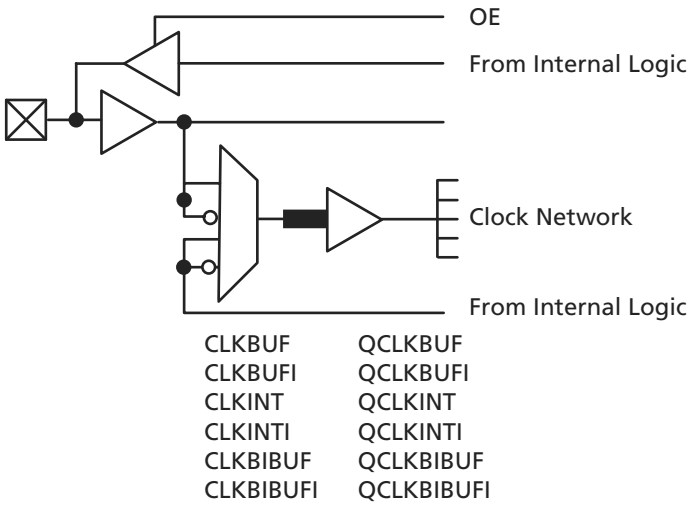

Figure 1-10 • **A54SX72A Routed Clock and QCLK Buffer**

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • **DC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	5.75	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{IH}	Input High Leakage Current[1]	V_{IN} = 2.7	–	70	µA
I_{IL}	Input Low Leakage Current[1]	V_{IN} = 0.5	–	–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4	–	V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA	–	0.55	V
C_{IN}	Input Pin Capacitance[3]		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.25 V)**

	Junction Temperature (T_J)						
V_{CCA}	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-16 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.3		1.5		1.7		2.6	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.5		0.5		0.8	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		1.9	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.2		1.3		1.6		2.2	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9		1.1		1.5	ns

Table 2-18 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing[1,2]										
t_{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[3]	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-24 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-27 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.5		2.8		3.3		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.7		7.7		8.7		10.2		14.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-30 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-33 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.4		2.9		4.0	ns
t_{DHL}	Data-to-Pad High to Low		2.0		2.3		2.6		3.1		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.4		2.9		4.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.0		2.3		2.6		3.1		4.3	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.6		3.0		3.4		4.0		5.6	ns
t_{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		9.0		10.4		11.8		13.8		19.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.6		3.0		3.4		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-34 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.1		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.5		2.9		4.1	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.6		7.6		8.6		10.1		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-35 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[2]												
t_{PD}	Internal Array Module		1.0		1.1		1.3		1.5		2.0	ns
Predicted Routing Delays[3]												
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{RD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{RD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{RD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{RD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{RD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.1		1.5	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.3	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		1.0		1.1		1.3		1.7	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.7		0.7		0.9		1.2	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.2		1.3		1.5		2.1	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-38 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: **All –3 speed grades have been discontinued.*

329-Pin PBGA	
Pin Number	**A54SX32A Function**
D11	V_{CCA}
D12	NC
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V_{CCI}
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND

329-Pin PBGA	
Pin Number	**A54SX32A Function**
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V_{CCA}
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	NC
L10	GND
L11	GND
L12	GND
L13	GND

329-Pin PBGA	
Pin Number	**A54SX32A Function**
L14	GND
L20	NC
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V_{CCA}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V_{CCA}
M21	I/O
M22	I/O
M23	V_{CCI}
N1	I/O
N2	TRST, I/O
N3	I/O
N4	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND

329-Pin PBGA	
Pin Number	**A54SX32A Function**
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V_{CCA}
U4	I/O
U20	I/O
U21	V_{CCA}
U22	I/O
U23	I/O
V1	V_{CCI}
V2	I/O
V3	I/O
V4	I/O
V20	I/O
V21	I/O

256-Pin FBGA

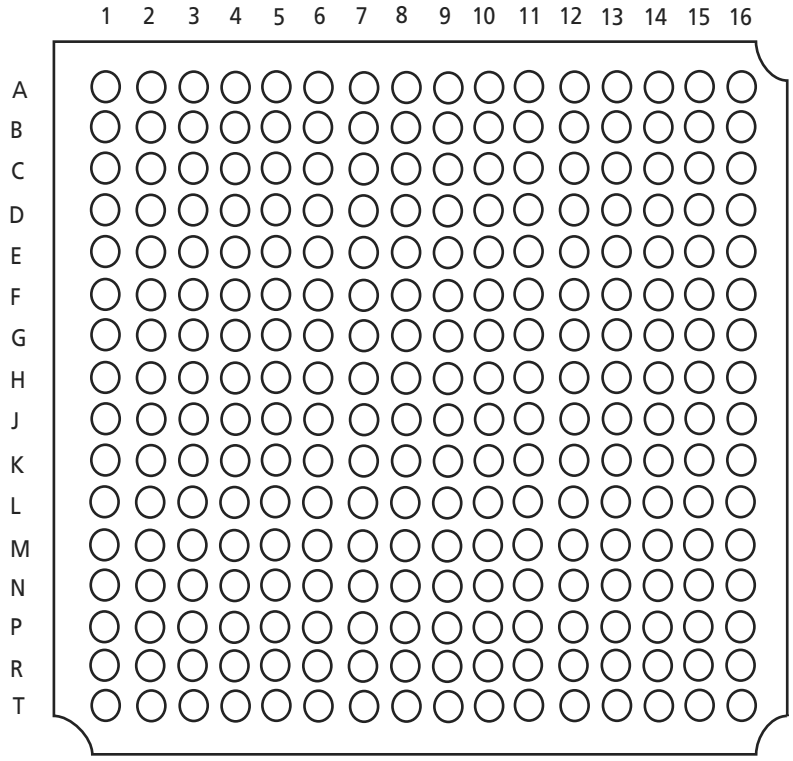

Figure 3-7 • **256-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC
A2	NC*	NC
A3	NC*	I/O
A4	NC*	I/O
A5	NC*	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC*	I/O
A12	NC*	I/O
A13	I/O	I/O
A14	NC*	NC
A15	NC*	I/O
A16	NC*	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC*	I/O
A22	NC*	I/O
A23	NC*	I/O
A24	NC*	I/O
A25	NC*	NC
A26	NC*	NC
AA1	NC*	I/O
AA2	NC*	I/O
AA3	V_{CCA}	V_{CCA}
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AA26	NC*	I/O
AB1	NC*	NC
AB2	V_{CCI}	V_{CCI}
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC*	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V_{CCA}	V_{CCA}
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC*	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC*	I/O
AB26	NC*	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC*	I/O
AC5	V_{CCI}	V_{CCI}
AC6	I/O	I/O
AC7	V_{CCI}	V_{CCI}
AC8	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V_{CCI}	V_{CCI}
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC*	I/O
AC24	I/O	I/O
AC25	NC*	I/O
AC26	NC*	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V_{CCI}	V_{CCI}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V_{CCI}	V_{CCI}
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V_{CCI}	V_{CCI}

Note: **These pins must be left floating on the A54SX32A device.*