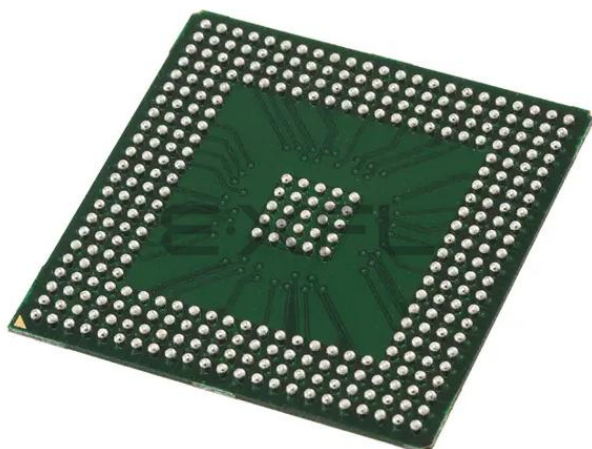




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

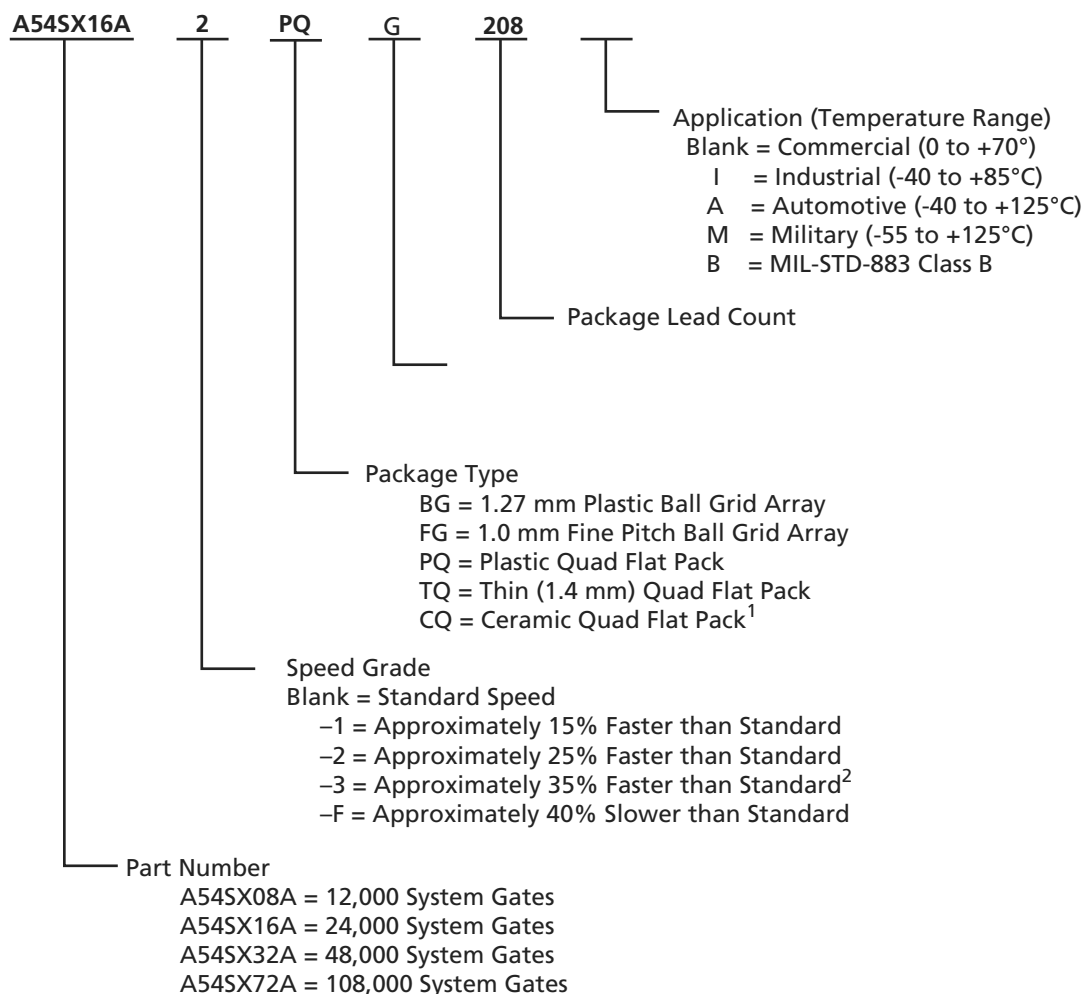
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	329-BBGA
Supplier Device Package	329-PBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-bg329i

Ordering Information



Notes:

- For more information about the CQFP package options, refer to the HiRel SX-A datasheet.
- All -3 speed grades have been discontinued.

Device Resources

Device	User I/Os (Including Clock Buffers)							
	208-Pin PQFP	100-Pin TQFP	144-Pin TQFP	176-Pin TQFP	329-Pin PBGA	144-Pin FBGA	256-Pin FBGA	484-Pin FBGA
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

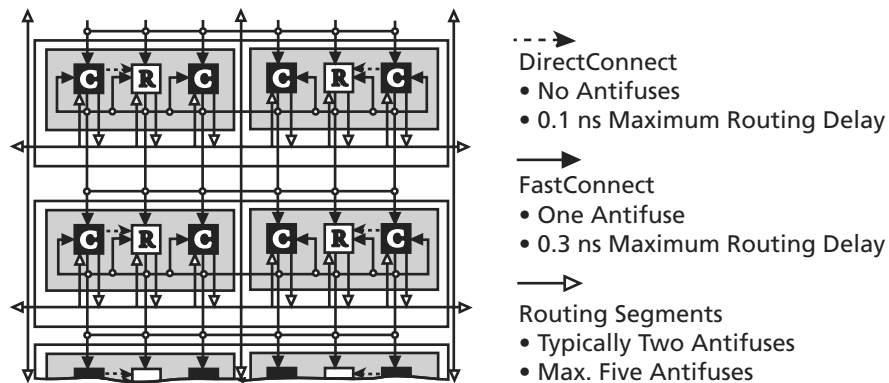


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

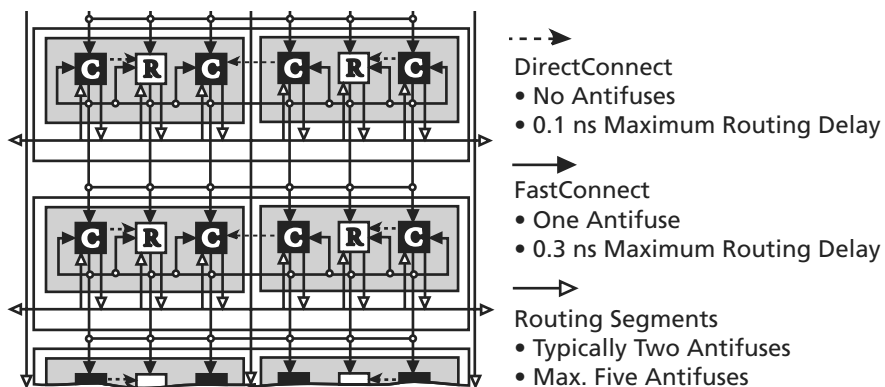


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • I/O Features

Function	Description
Input Buffer Threshold Selections	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) - I/O on an unpowered device does not sink current - Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μ s	0.025 V/ μ s	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μ s	μ s	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

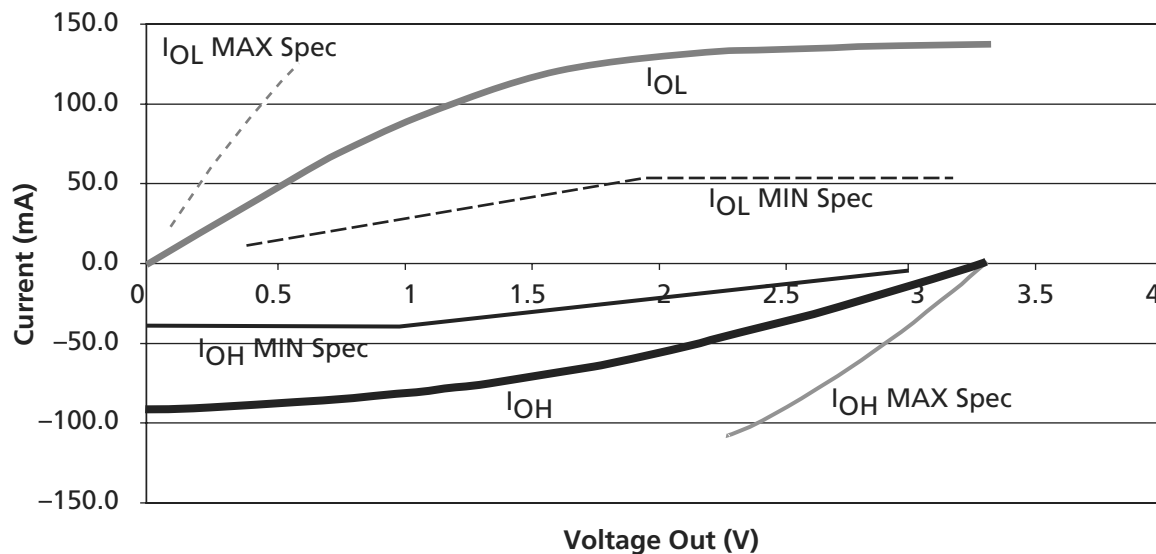


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Where:

- C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
 C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
 C_{EQI} = Equivalent capacitance of input buffers in pF
 C_{EQO} = Equivalent capacitance of output buffers in pF
 C_{EQCR} = Equivalent capacitance of CLKA/B in pF
 C_{EQHV} = Variable capacitance of HCLK in pF
 C_{EQHF} = Fixed capacitance of HCLK in pF
 C_L = Output lead capacitance in pF
 f_m = Average logic module switching rate in MHz
 f_n = Average input buffer switching rate in MHz
 f_p = Average output buffer switching rate in MHz
 f_{q1} = Average CLKA rate in MHz
 f_{q2} = Average CLKB rate in MHz
 f_{s1} = Average HCLK rate in MHz
 m = Number of logic modules switching at f_m
 n = Number of input buffers switching at f_n
 p = Number of output buffers switching at f_p
 q_1 = Number of clock loads on CLKA
 q_2 = Number of clock loads on CLKB
 r_1 = Fixed capacitance due to CLKA
 r_2 = Fixed capacitance due to CLKB
 s_1 = Number of clock loads on HCLK
 x = Number of I/Os at logic low
 y = Number of I/Os at logic high

Table 2-11 • CEQ Values for SX-A Devices

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQSM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}\text{C/W} \text{ is taken from Table 2-12 on page 2-11}$$

$$T_A = 125^{\circ}\text{C} \text{ is the maximum limit of ambient (from the datasheet)}$$

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_J = 110^{\circ}\text{C}$$

$$T_A = 70^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 18.0^{\circ}\text{C/W}$$

$$\theta_{JC} = 3.2^{\circ}\text{C/W}$$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{3.00 \text{ W}} = 13.33^{\circ}\text{C/W}$$

EQ 2-13

Table 2-14 • A54SX08A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays²										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{1,2}										
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-27 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6		ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.5		2.8		3.3		4.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9		ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6		ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.7		7.7		8.7		10.2		14.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4		ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-38 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.7		3.1		3.5		4.1		5.7		ns
t _{DHL}	Data-to-Pad High to Low	3.4		3.9		4.4		5.1		7.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.7		3.1		3.5		4.1		5.7		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.4		3.9		4.4		5.1		7.2		ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.1		3.7		5.1		ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.5		4.0		4.7		6.6		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.4		8.5		9.7		11.4		15.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.1		3.7		5.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.5		4.0		4.7		6.6		ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V _{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V _{CCA}	V _{CCA}	V _{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

329-Pin PBGA

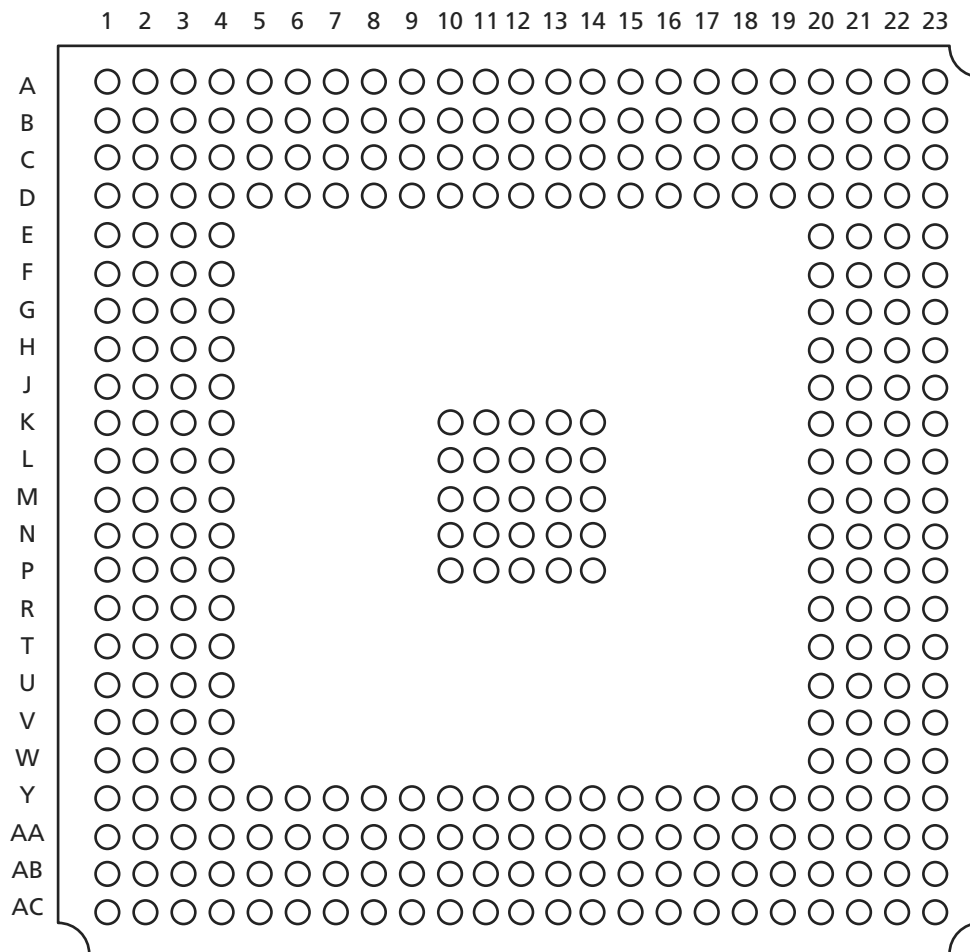


Figure 3-5 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

256-Pin FBGA			
Pin Number	A545X16A Function	A545X32A Function	A545X72A Function
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V _{CCI}	V _{CCI}	V _{CCI}
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	V _{CCI}	V _{CCI}	V _{CCI}
F10	V _{CCI}	V _{CCI}	V _{CCI}
F11	I/O	I/O	I/O
F12	V _{CCA}	V _{CCA}	V _{CCA}
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V _{CCI}	V _{CCI}	V _{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V _{CCI}	V _{CCI}	V _{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V _{CCA}	V _{CCA}	V _{CCA}

256-Pin FBGA			
Pin Number	A545X16A Function	A545X32A Function	A545X72A Function
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V _{CCA}	V _{CCA}	V _{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V _{CCI}	V _{CCI}	V _{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V _{CCI}	V _{CCI}	V _{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V _{CCI}	V _{CCI}	V _{CCI}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V _{CCI}	V _{CCI}	V _{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V _{CCA}	V _{CCA}	V _{CCA}

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V _{CCA}	V _{CCA}	V _{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC *	I/O
T26	NC *	I/O
U1	I/O	I/O
U2	V _{CCI}	V _{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V _{CCI}	V _{CCI}
U26	I/O	I/O
V1	NC *	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
V2	NC *	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V _{CCA}	V _{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC *	I/O
V26	NC *	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V _{CCA}	V _{CCA}
W24	I/O	I/O
W25	NC *	I/O
W26	NC *	I/O
Y1	NC *	I/O
Y2	NC *	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC *	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V _{CCI}	V _{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

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