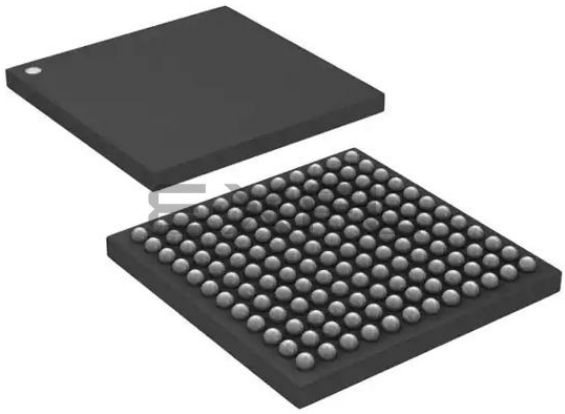

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 111 |
| Number of Gates | 48000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx32a-ffg144 |

## Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

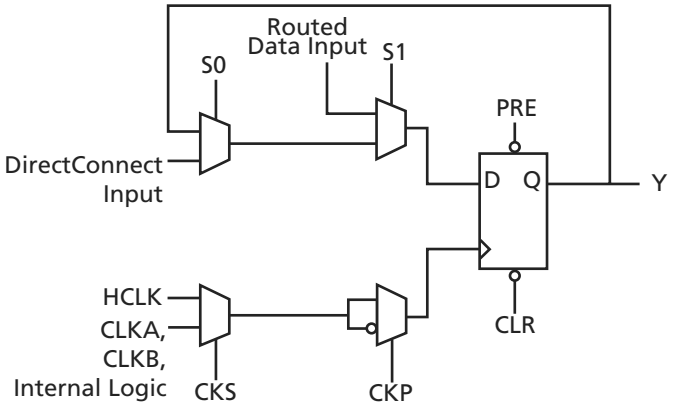


*Figure 1-2* • **R-Cell**

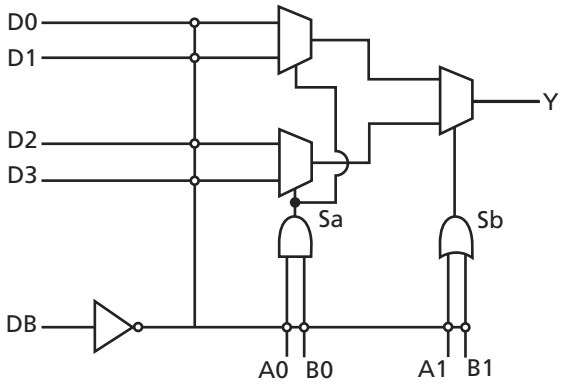


*Figure 1-3* • **C-Cell**

## Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

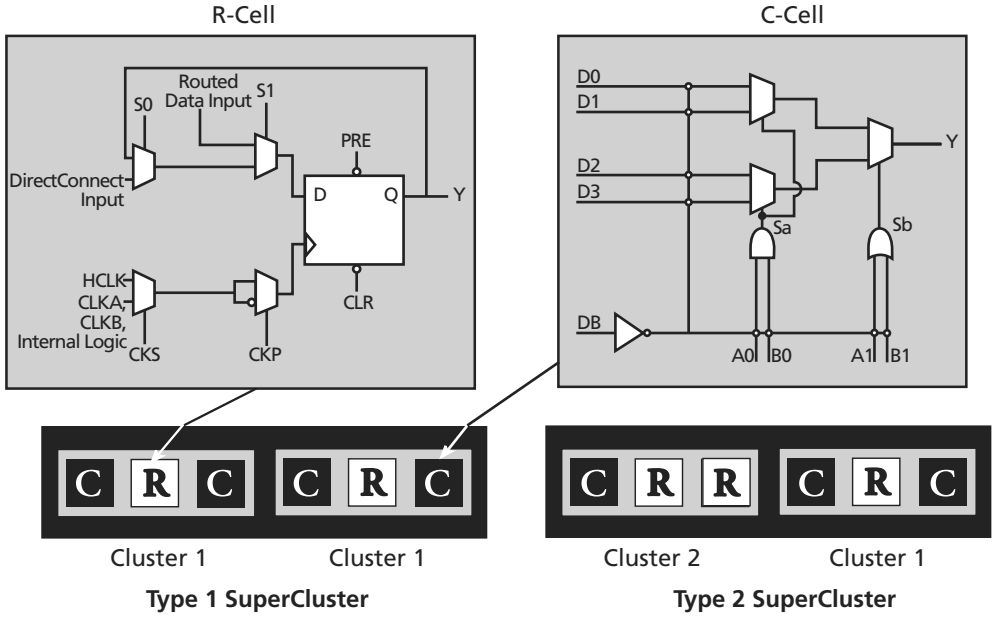


*Figure 1-4* • **Cluster Organization**

# Other Architectural Features

## Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 µ / 0.25 µ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

## Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

## User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).


*Figure 1-11* • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

## I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than $V_{CCI}$ and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and $V_{CCI}$ is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before $V_{CCA}$ reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

## SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

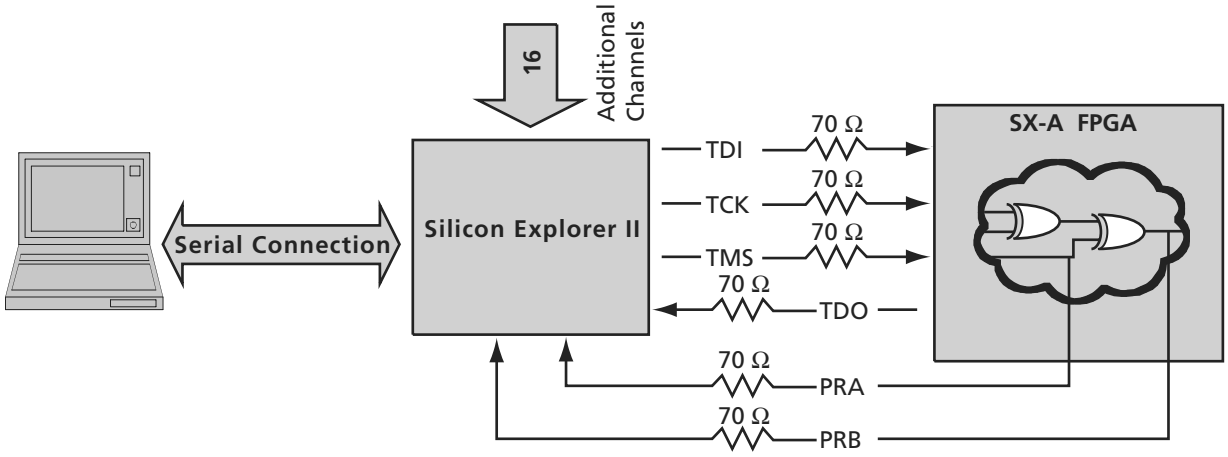


*Figure 1-13* • **Probe Setup**

# Pin Description

**CLKA/B, I/O Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

**QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

**GND Ground**

Low supply voltage.

**HCLK Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

**I/O Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

**NC No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

**PRA/B, I/O Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK, I/O Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI, I/O Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO, I/O Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

**TMS Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**TRST, I/O Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

**$V_{CCI}$ Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All $V_{CCI}$ power pins in the device should be connected.

**$V_{CCA}$ Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All $V_{CCA}$ power pins in the device should be connected.

# Detailed Specifications

## Operating Conditions

*Table 2-1* • **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CCI}$ | DC Supply Voltage for I/Os | –0.3 to +6.0 | V |
| $V_{CCA}$ | DC Supply Voltage for Arrays | –0.3 to +3.0 | V |
| $V_I$ | Input Voltage | –0.5 to +5.75 | V |
| $V_O$ | Output Voltage | –0.5 to + $V_{CCI}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

***Note:*** **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".*

*Table 2-2* • **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Units |
|---|---|---|---|
| Temperature Range | 0 to +70 | –40 to +85 | °C |
| 2.5 V Power Supply Range ($V_{CCA}$ and $V_{CCI}$) | 2.25 to 2.75 | 2.25 to 2.75 | V |
| 3.3 V Power Supply Range ($V_{CCI}$) | 3.0 to 3.6 | 3.0 to 3.6 | V |
| 5 V Power Supply Range ($V_{CCI}$) | 4.75 to 5.25 | 4.75 to 5.25 | V |

## Typical SX-A Standby Current

*Table 2-3* • **Typical Standby Current for SX-A at 25°C with $V_{CCA}$ = 2.5 V**

| Product | $V_{CCI}$ = 2.5 V | $V_{CCI}$ = 3.3 V | $V_{CCI}$ = 5 V |
|---|---|---|---|
| A54SX08A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX16A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX32A | 0.9 mA | 1.0 mA | 3.0 mA |
| A54SX72A | 3.6 mA | 3.8 mA | 4.5 mA |

*Table 2-4* • **Supply Voltages**

| $V_{CCA}$ | $V_{CCI}$* | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|
| 2. 5 V | 2.5 V | 5.75 V | 2.7 V |
| 2.5 V | 3.3 V | 5.75 V | 3.6 V |
| 2.5 V | 5 V | 5.75 V | 5.25 V |

***Note:*** **3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.*

# PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

*Table 2-7* • **DC Specifications (5 V PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 2.25 | 2.75 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 4.75 | 5.25 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | 5.75 | V |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.8 | V |
| $I_{IH}$ | Input High Leakage Current[1] | $V_{IN}$ = 2.7 | – | 70 | µA |
| $I_{IL}$ | Input Low Leakage Current[1] | $V_{IN}$ = 0.5 | – | –70 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –2 mA | 2.4 | – | V |
| $V_{OL}$ | Output Low Voltage[2] | $I_{OUT}$ = 3 mA, 6 mA | – | 0.55 | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | – | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |

***Notes:***

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

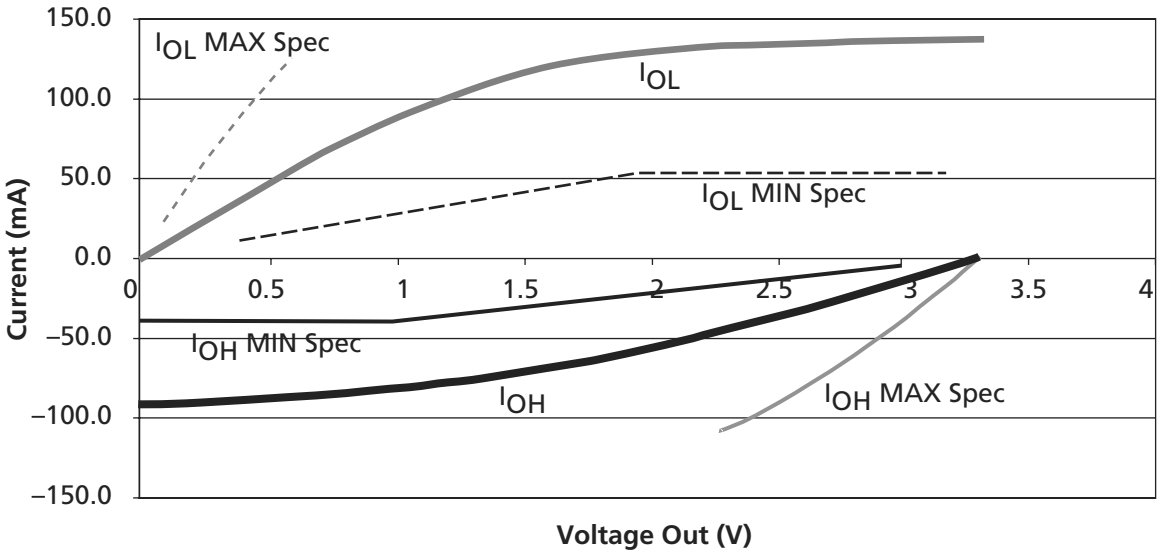


*Figure 2-2* • **3.3 V PCI V/I Curve for SX-A Family**

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7\ V_{CCI} < V_{OUT} < V_{CCI}$

*EQ 2-3*

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18\ V_{CCI}$

*EQ 2-4*

# Timing Characteristics

*Table 2-14* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |

***Notes:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-19* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **3.3 V PCI Output Module Timing[1]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $d_{TLH}$[2] | Delta Low to High | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[2] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[3]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 10.4 | | 11.8 | | 13.8 | | 19.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3 | | 3.4 | | 4 | | 5.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3 | | 3.3 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[2] | Delta Low to High | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[2] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[2] | Delta High to Low—low slew | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *Delays based on 10 pF loading and 25 Ω resistance.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
3. *Delays based on 35 pF loading.*

*Table 2-35* • **A54SX72A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

# Package Pin Assignments

## 208-Pin PQFP

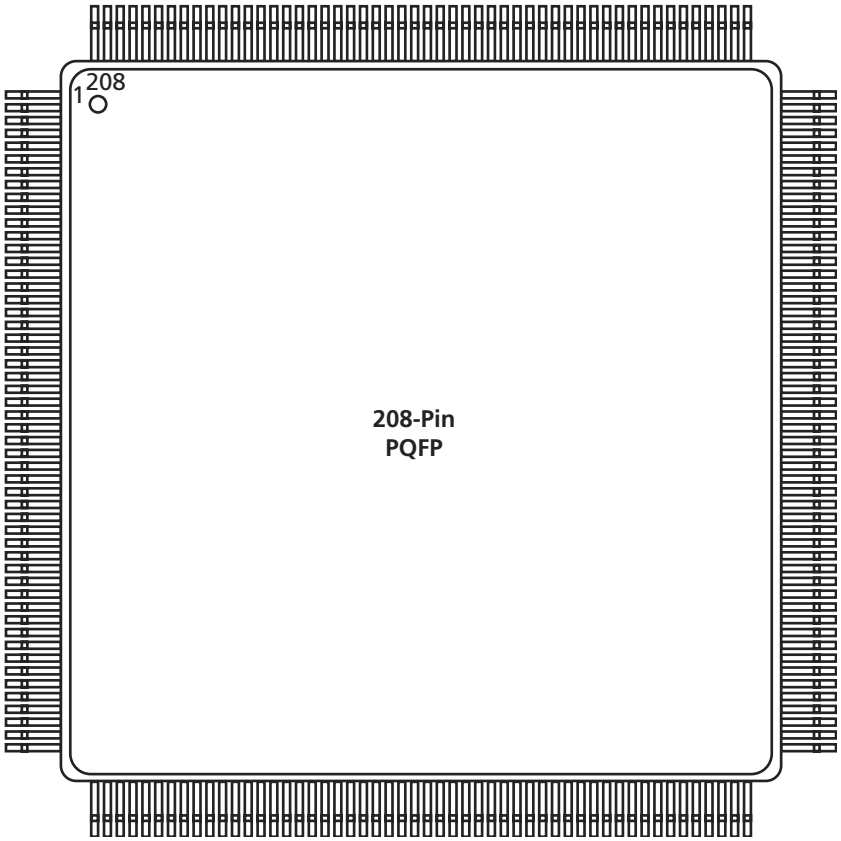


*Figure 3-1* • **208-Pin PQFP (Top View)**

### Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O | I/O |
| 73 | NC | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | QCLKA |
| 75 | NC | I/O | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O | PRB,I/O |
| 77 | GND | GND | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND | GND | GND |
| 80 | NC | NC | NC | NC |
| 81 | I/O | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O | $V_{CCI}$ |
| 84 | I/O | I/O | I/O | QCLKB |
| 85 | NC | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O | I/O |
| 88 | NC | I/O | I/O | I/O |
| 89 | I/O | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O | I/O |
| 91 | NC | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O | I/O |
| 94 | NC | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O | I/O |
| 97 | NC | I/O | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O | I/O |
| 105 | GND | GND | GND | GND |

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 106 | NC | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O | I/O |
| 108 | NC | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | NC | I/O | I/O | GND |
| 117 | I/O | I/O | I/O | $V_{CCA}$ |
| 118 | I/O | I/O | I/O | I/O |
| 119 | NC | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O | I/O |
| 122 | NC | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O | I/O |
| 125 | NC | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O | I/O |
| 129 | GND | GND | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND | GND | GND |
| 132 | NC | NC | NC | I/O |
| 133 | I/O | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O | I/O |
| 135 | NC | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O | I/O |
| 138 | NC | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O | I/O |

# 176-Pin TQFP

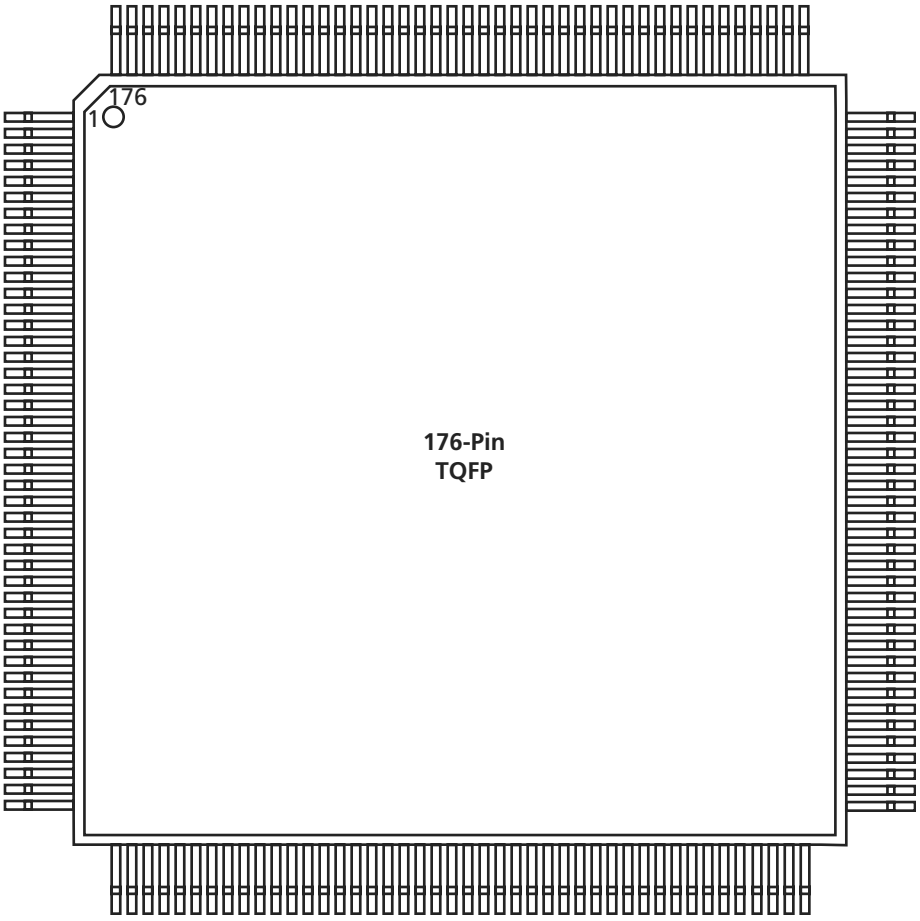


*Figure 3-4* • **176-Pin TQFP (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 329-Pin PBGA

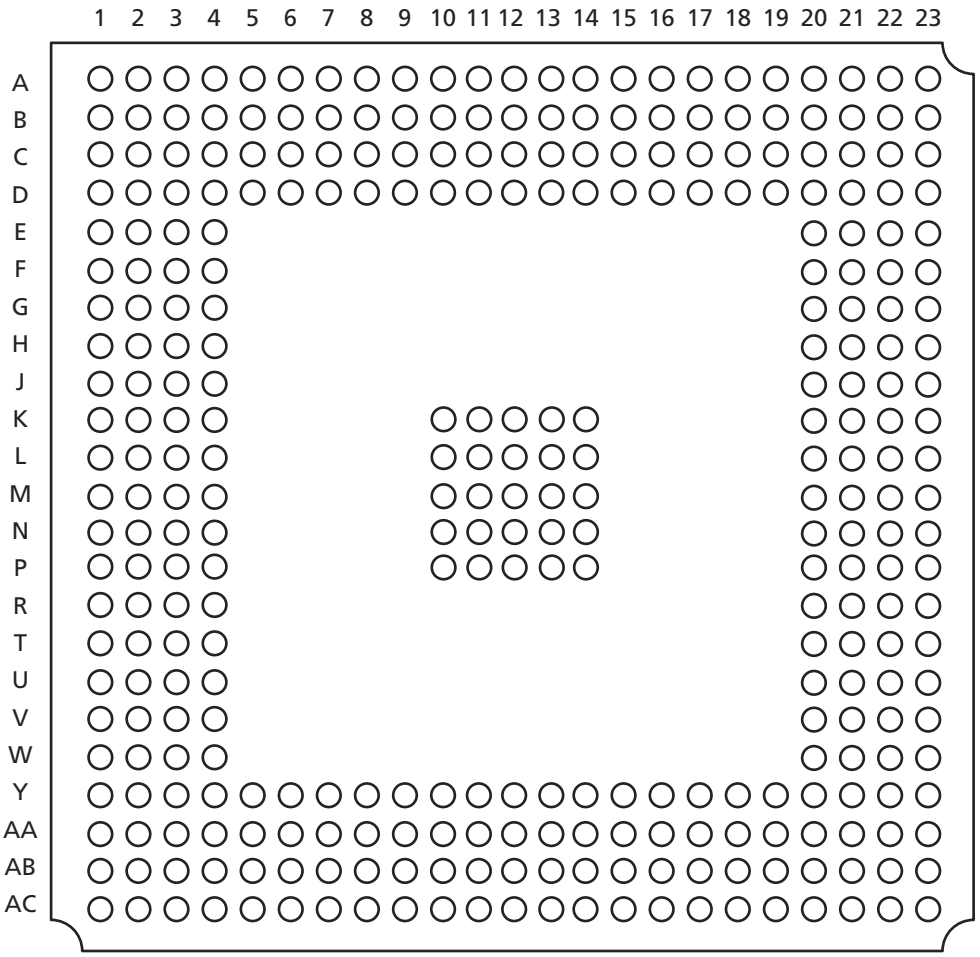


*Figure 3-5* • **329-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 144-Pin FBGA

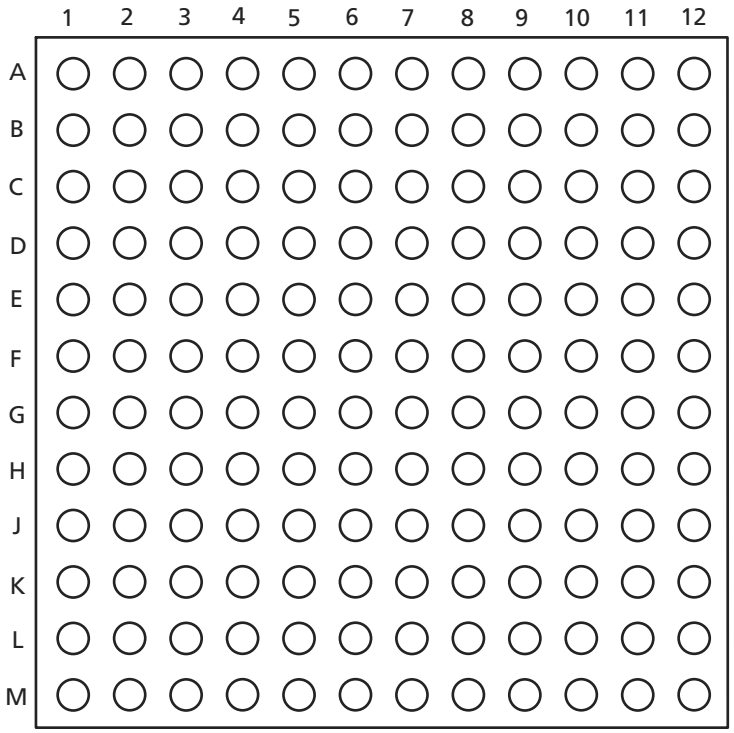


*Figure 3-6* • **144-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 144-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| G1 | I/O | I/O | I/O |
| G2 | GND | GND | GND |
| G3 | I/O | I/O | I/O |
| G4 | I/O | I/O | I/O |
| G5 | GND | GND | GND |
| G6 | GND | GND | GND |
| G7 | GND | GND | GND |
| G8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| G9 | I/O | I/O | I/O |
| G10 | I/O | I/O | I/O |
| G11 | I/O | I/O | I/O |
| G12 | I/O | I/O | I/O |
| H1 | TRST, I/O | TRST, I/O | TRST, I/O |
| H2 | I/O | I/O | I/O |
| H3 | I/O | I/O | I/O |
| H4 | I/O | I/O | I/O |
| H5 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H6 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H9 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H10 | I/O | I/O | I/O |
| H11 | I/O | I/O | I/O |
| H12 | NC | NC | NC |
| J1 | I/O | I/O | I/O |
| J2 | I/O | I/O | I/O |
| J3 | I/O | I/O | I/O |
| J4 | I/O | I/O | I/O |
| J5 | I/O | I/O | I/O |
| J6 | PRB, I/O | PRB, I/O | PRB, I/O |
| J7 | I/O | I/O | I/O |
| J8 | I/O | I/O | I/O |
| J9 | I/O | I/O | I/O |
| J10 | I/O | I/O | I/O |
| J11 | I/O | I/O | I/O |
| J12 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |

| 144-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| K1 | I/O | I/O | I/O |
| K2 | I/O | I/O | I/O |
| K3 | I/O | I/O | I/O |
| K4 | I/O | I/O | I/O |
| K5 | I/O | I/O | I/O |
| K6 | I/O | I/O | I/O |
| K7 | GND | GND | GND |
| K8 | I/O | I/O | I/O |
| K9 | I/O | I/O | I/O |
| K10 | GND | GND | GND |
| K11 | I/O | I/O | I/O |
| K12 | I/O | I/O | I/O |
| L1 | GND | GND | GND |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | HCLK | HCLK | HCLK |
| L8 | I/O | I/O | I/O |
| L9 | I/O | I/O | I/O |
| L10 | I/O | I/O | I/O |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| M8 | I/O | I/O | I/O |
| M9 | I/O | I/O | I/O |
| M10 | I/O | I/O | I/O |
| M11 | TDO, I/O | TDO, I/O | TDO, I/O |
| M12 | I/O | I/O | I/O |

# 484-Pin FBGA

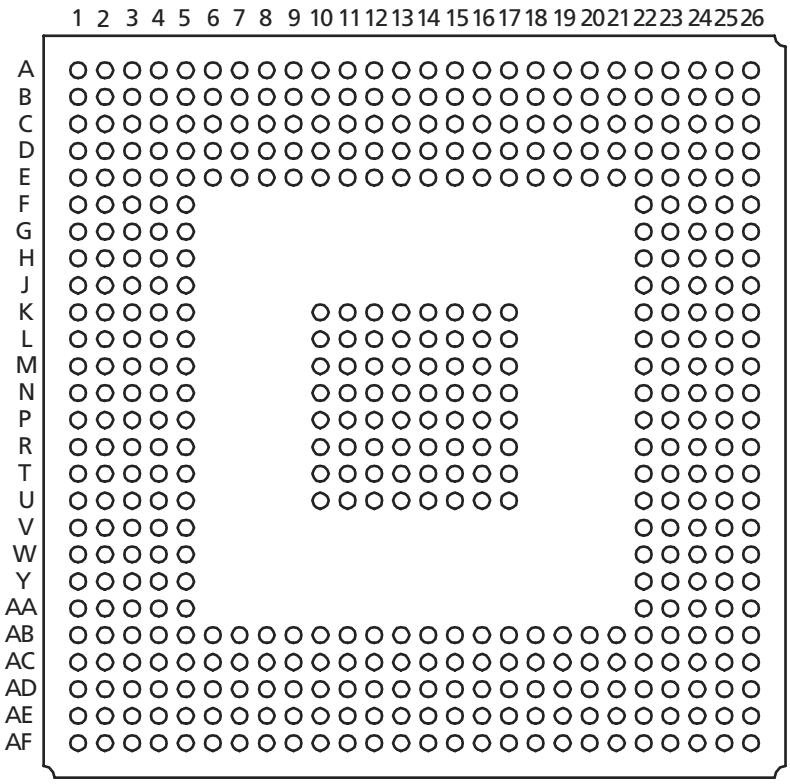


*Figure 3-8* • **484-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| K10 | GND | GND |
| K11 | GND | GND |
| K12 | GND | GND |
| K13 | GND | GND |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | GND | GND |
| K17 | GND | GND |
| K22 | I/O | I/O |
| K23 | I/O | I/O |
| K24 | NC* | NC |
| K25 | NC* | I/O |
| K26 | NC* | I/O |
| L1 | NC* | I/O |
| L2 | NC* | I/O |
| L3 | I/O | I/O |
| L4 | I/O | I/O |
| L5 | I/O | I/O |
| L10 | GND | GND |
| L11 | GND | GND |
| L12 | GND | GND |
| L13 | GND | GND |
| L14 | GND | GND |
| L15 | GND | GND |
| L16 | GND | GND |
| L17 | GND | GND |
| L22 | I/O | I/O |
| L23 | I/O | I/O |
| L24 | I/O | I/O |
| L25 | I/O | I/O |
| L26 | I/O | I/O |
| M1 | NC* | NC |
| M2 | I/O | I/O |
| M3 | I/O | I/O |
| M4 | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| M5 | I/O | I/O |
| M10 | GND | GND |
| M11 | GND | GND |
| M12 | GND | GND |
| M13 | GND | GND |
| M14 | GND | GND |
| M15 | GND | GND |
| M16 | GND | GND |
| M17 | GND | GND |
| M22 | I/O | I/O |
| M23 | I/O | I/O |
| M24 | I/O | I/O |
| M25 | NC* | I/O |
| M26 | NC* | I/O |
| N1 | I/O | I/O |
| N2 | $V_{CCI}$ | $V_{CCI}$ |
| N3 | I/O | I/O |
| N4 | I/O | I/O |
| N5 | I/O | I/O |
| N10 | GND | GND |
| N11 | GND | GND |
| N12 | GND | GND |
| N13 | GND | GND |
| N14 | GND | GND |
| N15 | GND | GND |
| N16 | GND | GND |
| N17 | GND | GND |
| N22 | $V_{CCA}$ | $V_{CCA}$ |
| N23 | I/O | I/O |
| N24 | I/O | I/O |
| N25 | I/O | I/O |
| N26 | NC* | NC |
| P1 | NC* | I/O |
| P2 | NC* | I/O |
| P3 | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| P4 | I/O | I/O |
| P5 | $V_{CCA}$ | $V_{CCA}$ |
| P10 | GND | GND |
| P11 | GND | GND |
| P12 | GND | GND |
| P13 | GND | GND |
| P14 | GND | GND |
| P15 | GND | GND |
| P16 | GND | GND |
| P17 | GND | GND |
| P22 | I/O | I/O |
| P23 | I/O | I/O |
| P24 | $V_{CCI}$ | $V_{CCI}$ |
| P25 | I/O | I/O |
| P26 | I/O | I/O |
| R1 | NC* | I/O |
| R2 | NC* | I/O |
| R3 | I/O | I/O |
| R4 | I/O | I/O |
| R5 | TRST, I/O | TRST, I/O |
| R10 | GND | GND |
| R11 | GND | GND |
| R12 | GND | GND |
| R13 | GND | GND |
| R14 | GND | GND |
| R15 | GND | GND |
| R16 | GND | GND |
| R17 | GND | GND |
| R22 | I/O | I/O |
| R23 | I/O | I/O |
| R24 | I/O | I/O |
| R25 | NC* | I/O |
| R26 | NC* | I/O |
| T1 | NC* | I/O |
| T2 | NC* | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*

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