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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	203
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-ffg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Information



Notes:

1. For more information about the CQFP package options, refer to the HiRel SX-A datasheet.

2. All –3 speed grades have been discontinued.

Device Resources

User I/Os (Including Clock Buffers)										
Device	208-Pin100-Pin144-Pin176-Pin329-Pin144-Pin256-Pin48PQFPTQFPTQFPTQFPPBGAFBGAFBGAFBGAFB									
A54SX08A	130	81	113	-	-	111	-	-		
A54SX16A	175	81	113	-	-	111	180	-		
A54SX32A	174	81	113	147	249	111	203	249		
A54SX72A	171	-	-	-	-	_	203	360		

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array



Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters



Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications.

Function	Description
Input Buffer Threshold Selections	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	 "Hot-Swap" Capability (3.3 V PCI is not hot swappable) I/O on an unpowered device does not sink current Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V _{CCA} and V _{CCI} can be powered in any order

Table 1-2 • I/O Features

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μs	0.025 V/ μs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μs	μs	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2



Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6	٠	Boundary-Scan Pin Configurations an	d
		Functions	

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test- Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function				
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)				
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up				
Reserve Probe	Keeps pins from being used or regular I/O				

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 •	JTAG	Instruction	Code
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Instructions (IR4:IR0)	Binary Code
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HighZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-8 JTAG Instruction Code

Device	Process	Revision	Bits 31-28	Bits 27-12
A54SX08A	0.22 µ	0	8, 9	40B4, 42B4
		1	А, В	40B4, 42B4
A54SX16A	0.22 µ	0	9	4088, 4288
		1	В	4088, 4288
	0.25 µ	1	В	22B8
A54SX32A	0.2 2µ	0	9	40BD, 42BD
		1	В	40BD, 42BD
	0.25 µ	1	В	22BD
A54SX72A	0.22 µ	0	9	40B2, 42B2
		1	В	40B2, 42B2
	0.25 µ	1	В	22B2

Electrical Specifications

Table 2-5 • 3.3 V LVTTL and 5 V TTL Electrical Specifications

			Comm	ercial	Industrial		
Symbol	Parameter		Min.	Max.	Min.	Max.	Units
V _{OH}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	$(I_{OH} = -1 \text{ mA})$	0.9 V _{CCI}		0.9 V _{CCI}		V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OH} = -8 mA)	2.4		2.4		V
V _{OL}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 1 mA)		0.4		0.4	V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 12 mA)		0.4		0.4	V
V _{IL}	Input Low Voltage			0.8		0.8	V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current		-10	10	-10	10	μΑ
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

		Parameter		nercial	Indu	strial	
Symbol	Parameter		Min.	Max.	Min.	Max.	Units
V _{OH}	$V_{DD} = MIN,$	$(I_{OH} = -100 \ \mu A)$	2.1		2.1		V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	$V_{DD} = MIN,$ $V_{I} = V_{UI} \text{ or } V_{U}$	$(I_{OH} = -1 \text{ mA})$	2.0		2.0		V
		(l - 2mA)	17		17		V
	$V_{DD} = V_{IH}$ or V_{IL}	(I _{OH} =2 IIIA)	1.7		1.7		v
V _{OL}	$V_{DD} = MIN,$	(I _{OL} = 100 μA)		0.2		0.2	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	$V_{DD} = MIN,$	(I _{OL} = 1 mA)		0.4		0.4	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$	-					
	$V_{DD} = MIN,$	(I _{OL} = 2 mA)		0.7		0.7	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
V _{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
$I_{\rm IL}/I_{\rm IH}$	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μΑ
I _{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	рF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}$$
C/W is taken from Table 2-12 on page 2-11

 $T_A = 125$ °C is the maximum limit of ambient (from the datasheet)

Max. Allowed Power =
$$\frac{\text{Max Junction Temp - Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_{J} = 110^{\circ}C$$

 $T_{A} = 70^{\circ}C$

From the datasheet:

 $\theta_{JA} = 18.0^{\circ}C/W$ $\theta_{JC} = 3.2^{\circ}C/W$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{Max Junction Temp - Max. Ambient Temp}{P} = \frac{110^{\circ}C - 70^{\circ}C}{3.00 W} = 13.33^{\circ}C/W$$

EQ 2-13

Timing Characteristics

Table 2-14 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 S	peed	-1 S	peed	Std. S	5peed	-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	igation Delays ¹									
t _{PD}	Internal Array Module		0.9		1.1		1.2		1.7	ns
Predicted Ro	outing Delays ²			4						
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns
R-Cell Timin	g									<u></u>
t _{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.7		0.9		1.2	ns
t _{sud}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays			1						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.8		0.9		1.0		1.4	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.0		1.2		1.4		1.9	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.3	ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.1		1.3		1.8	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-15 • A54SX08A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _C	_{CI} = 2.25 V, T _J = 70°C)
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		-2 Speed -		-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lardwired) Array Clock Networks			8				8		
t _{НСКН}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Arra	y Clock Networks									
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-27 A54SX16A Timing Characteristics

		-3 Speed ¹	-2 S	peed	-1 Speed		Std. 9	Speed	–F S	peed	
Parameter	Description	Min. Max	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
5 V PCI Out	put Module Timing ²										
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6	ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.5		2.8		3.3		4.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9	ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Out	put Module Timing ⁴								-		
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6	ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.7		7.7		8.7		10.2		14.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4	ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 50 pF loading.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.

Table 2-28 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-3 Sp	beed ¹	-2 S	peed	-1 S	peed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	agation Delays ²											
t _{PD}	Internal Array Module		0.8		0.9		1.1		1.2		1.7	ns
Predicted R	outing Delays ³											
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timin	ng											
t _{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays					-						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.2		1.3		1.5		1.8		2.5	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.6		0.7		0.8		0.9		1.3	ns
t _{INYH}	lnput Data Pad to Y High 3.3 V LVTTL		0.8		0.9		1.0		1.2		1.6	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.4		1.6		1.8		2.2		3.0	ns

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-29 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _c	_{CCI} = 2.25 V, T _J = 70°C)
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		-3 Sp	beed*	-2 S	-2 Speed		peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Netwo	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Arr	ay Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-34 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions	$V_{CCA} = 2.25 V, V_{CC}$	_{Cl} = 4.75 V, T _J = 70°C)
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		-3 Speed ¹	-2 Spe	-2 Speed		k	Std. S	Speed	–F S	peed	
Parameter	Description	Min. Max.	Min. M	lax.	Min. Ma	х.	Min.	Max.	Min.	Max.	Units
5 V PCI Out	put Module Timing ²										
t _{DLH}	Data-to-Pad Low to High	2.1	2	2.4	2.8	3		3.2		4.5	ns
t _{DHL}	Data-to-Pad High to Low	2.8	3	3.2	3.6	5		4.2		5.9	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3	1	1.5	1.7	7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.1	2	2.4	2.8	3		3.2		4.5	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0	3	3.5	3.9	9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8	3	3.2	3.6	5		4.2		5.9	ns
d _{TLH} ³	Delta Low to High	0.016	0.	016	0.0	2		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low	0.026	0	.03	0.03	32		0.04		0.052	ns/pF
5 V TTL Out	put Module Timing ⁴										
t _{DLH}	Data-to-Pad Low to High	1.9	2	2.2	2.5	5		2.9		4.1	ns
t _{DHL}	Data-to-Pad High to Low	2.5	Ź	2.9	3.3	3		3.9		5.4	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.6	7	7.6	8.6	5		10.1		14.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1	2	2.4	2.7	7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4	8	8.4	9.5	5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9	2	2.2	2.!	5		2.9		4.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6	2	4.2	4.7	7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5	Ź	2.9	3.3	3		3.9		5.4	ns
d _{TLH} ³	Delta Low to High	0.014	0.	017	0.0	17		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low	0.023	0.	029	0.03	31		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043	0.	046	0.0	57		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 50 pF loading.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.

Table 2-35 A54SX72A Timing Characteristics (Continued)

		-3 Sp	beed ¹	-2 S	peed	-1 S	peed	Std. 9	5peed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t _{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t _{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t _{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Modu	le Predicted Routing Delays ³											
t _{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t _{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t _{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t _{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t _{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t _{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

(Worst-Case Commercial Conditions, $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 3.0 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-36 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 V$, $V_{CCI} = 2.25 V$, $T_J = 70^{\circ}C$:)
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		-3 Sp	beed*	-2 S	peed	–1 Speed		-1 Speed Std. Spee		ed –F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-39 A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 2.3 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

		-3 Speed	-2 9	peed	–1 Speed	–1 Speed Std. Speed		J –F Speed		
Parameter	Description	Min. Max	. Min.	Max.	Min. Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2, 3}									
t _{DLH}	Data-to-Pad Low to High	3.9		4.5	5.1		6.0		8.4	ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.6	4.1		4.8		6.7	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12.7		14.6	16.5		19.4		27.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8	3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8		13.7	15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.9		4.5	5.1		6.0		8.4	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5	2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.6	4.1		4.8		6.7	ns
d_{TLH}^{4}	Delta Low to High	0.03	1	0.037	0.043		0.051		0.071	ns/pF
${\sf d_{THL}}^4$	Delta High to Low	0.01	7	0.017	0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.05	7	0.06	0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-40 A54SX72A Timing Characteristics

(Worst-Case Commercial	Conditions $V_{CCA} = 2.25$	$V_{V_{CCI}} = 3.0$	$I_{1} = 70^{\circ}C$
(.,.,,

		-3 Speed ¹	–2 Spee	-2 Speed -1 Speed		1 Speed Std. Speed		I –F Speed			
Parameter	Description	Min. Max.	Min. M	ax.	Min. M	ax.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Output Module Timing ²											
t _{DLH}	Data-to-Pad Low to High	2.3	2	.7	3	8.0		3.6		5.0	ns
t _{DHL}	Data-to-Pad High to Low	2.5	2	.9	3	8.2		3.8		5.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4	1	.7	1	.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2	.7	3	0.0		3.6		5.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5	2	.8	3	8.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5	2	.9	3	8.2		3.8		5.3	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	.03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0	015	0.0	015		0.015		0.025	ns/pF
3.3 V LVTTL	Output Module Timing ⁴				•						
t _{DLH}	Data-to-Pad Low to High	3.2	3	.7	4	.2		5.0		6.9	ns
t _{DHL}	Data-to-Pad High to Low	3.2	3	.7	4	.2		4.9		6.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3	11	1.9	13	3.5		15.8		22.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2	2	.6	2	.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8	18	3.9	2	1.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2	3	.7	4	.2		5.0		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9	3	.3	3	8.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2	3	.7	4	.2		4.9		6.9	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	.03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0)15	0.0	015		0.015		0.025	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053	0.0)53	0.0	067		0.073		0.107	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 10 pF loading and 25 Ω resistance.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.



100-Pin TQFP



Figure 3-2 • 100-Pin TQFP

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

	144-Pi	n TQFP		144-Pin TQFP					
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function		
75	I/O	I/O	I/O	111	I/O	I/O	I/O		
76	I/O	I/O	I/O	112	I/O	I/O	I/O		
77	I/O	I/O	I/O	113	I/O	I/O	I/O		
78	I/O	I/O	I/O	114	I/O	I/O	I/O		
79	V _{CCA}	V _{CCA}	V _{CCA}	115	V _{CCI}	V _{CCI}	V _{CCI}		
80	V _{CCI}	V _{CCI}	V _{CCI}	116	I/O	I/O	I/O		
81	GND	GND	GND	117	I/O	I/O	I/O		
82	I/O	I/O	I/O	118	I/O	I/O	I/O		
83	I/O	I/O	I/O	119	I/O	I/O	I/O		
84	I/O	I/O	I/O	120	I/O	I/O	I/O		
85	I/O	I/O	I/O	121	I/O	I/O	I/O		
86	I/O	I/O	I/O	122	I/O	I/O	I/O		
87	I/O	I/O	I/O	123	I/O	I/O	I/O		
88	I/O	I/O	I/O	124	I/O	I/O	I/O		
89	V _{CCA}	V _{CCA}	V _{CCA}	125	CLKA	CLKA	CLKA		
90	NC	NC	NC	126	CLKB	CLKB	CLKB		
91	I/O	I/O	I/O	127	NC	NC	NC		
92	I/O	I/O	I/O	128	GND	GND	GND		
93	I/O	I/O	I/O	129	V _{CCA}	V _{CCA}	V _{CCA}		
94	I/O	I/O	I/O	130	I/O	I/O	I/O		
95	I/O	I/O	I/O	131	PRA, I/O	PRA, I/O	PRA, I/O		
96	I/O	I/O	I/O	132	I/O	I/O	I/O		
97	I/O	I/O	I/O	133	I/O	I/O	I/O		
98	V _{CCA}	V _{CCA}	V _{CCA}	134	I/O	I/O	I/O		
99	GND	GND	GND	135	I/O	I/O	I/O		
100	I/O	I/O	I/O	136	I/O	I/O	I/O		
101	GND	GND	GND	137	I/O	I/O	I/O		
102	V _{CCI}	V _{CCI}	V _{CCI}	138	I/O	I/O	I/O		
103	I/O	I/O	I/O	139	I/O	I/O	I/O		
104	I/O	I/O	I/O	140	V _{CCI}	V _{CCI}	V _{CCI}		
105	I/O	I/O	I/O	141	I/O	I/O	I/O		
106	I/O	I/O	I/O	142	I/O	I/O	I/O		
107	I/O	I/O	I/O	143	I/O	I/O	I/O		
108	I/O	I/O	I/O	144	TCK, I/O	TCK, I/O	TCK, I/O		
109	GND	GND	GND						
110	I/O	I/O	I/O						



256-Pin FBGA



Figure 3-7 • 256-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.