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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx32a-fgg144m

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Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000

different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

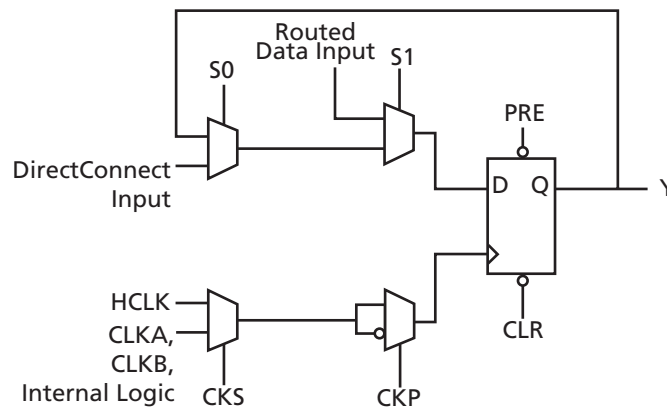


Figure 1-2 • R-Cell

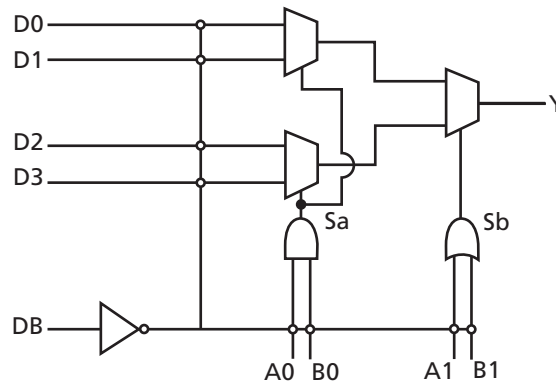


Figure 1-3 • C-Cell

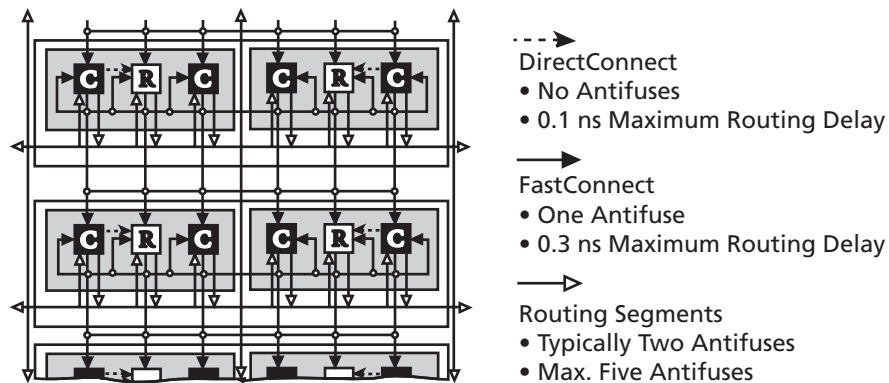


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

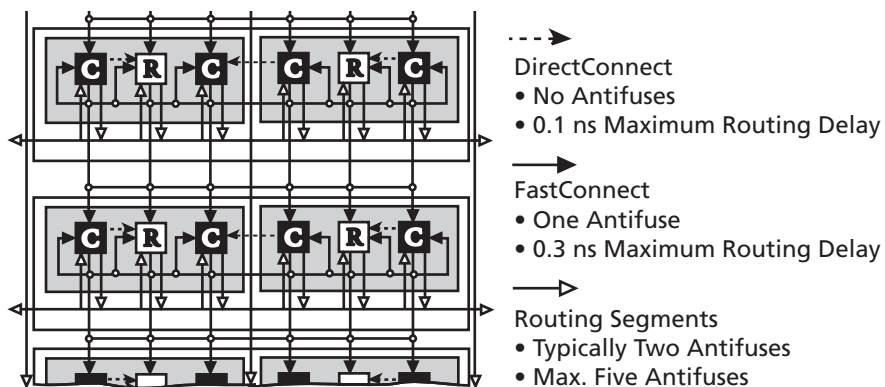


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, [Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications](#).

Table 1-2 • I/O Features

Function	Description
Input Buffer Threshold Selections	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) - I/O on an unpowered device does not sink current - Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μ s	0.025 V/ μ s	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μ s	μ s	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to [Table 1-6 on page 1-9](#)). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CC} Supply Voltage

Supply voltage for I/Os. See [Table 2-2 on page 2-1](#). All V_{CC} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See [Table 2-2 on page 2-1](#). All V_{CCA} power pins in the device should be connected.

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

$$\theta_{CS} = 0.37^{\circ}\text{C/W}$$

= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{thermal resistance of the heat sink in } ^{\circ}\text{C/W}$$

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33^{\circ}\text{C/W} - 3.20^{\circ}\text{C/W} - 0.37^{\circ}\text{C/W}$$

$$\theta_{SA} = 9.76^{\circ}\text{C/W}$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Table 2-16 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.3		1.5		1.7		2.6	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.1		1.3		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.5		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		1.9	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.2		1.3		1.6		2.2	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.8		0.9		1.1		1.5	ns

Table 2-20 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH} ²	Delta Low to High	0.016		0.02		0.022		0.032		ns/pF
d _{THL} ²	Delta High to Low	0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.6		8.6		10.1		14.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH}	Delta Low to High	0.017		0.017		0.023		0.031		ns/pF
d _{THL}	Delta High to Low	0.029		0.031		0.037		0.051		ns/pF
d _{THLS}	Delta High to Low—low slew	0.046		0.057		0.066		0.089		ns/pF

Notes:

- Delays based on 50 pF loading.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-25 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{2, 3}												
t _{DLH}	Data-to-Pad Low to High	3.4		3.9		4.5		5.2		7.3		ns
t _{DHL}	Data-to-Pad High to Low	2.6		3.0		3.3		3.9		5.5		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	11.6		13.4		15.2		17.9		25.0		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8		3.2		3.7		5.2		ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8		13.7		15.5		18.2		25.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.4		3.9		4.5		5.2		7.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5		2.8		3.3		4.7		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.6		3.0		3.3		3.9		5.5		ns
d _{TLH} ⁴	Delta Low to High	0.031		0.037		0.043		0.051		0.071		ns/pF
d _{THL} ⁴	Delta High to Low	0.017		0.017		0.023		0.023		0.037		ns/pF
d _{THLS} ⁴	Delta High to Low—low slew	0.057		0.06		0.071		0.086		0.117		ns/pF

Note:

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-28 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	0.8		0.9		1.1		1.2		1.7		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	1.2		1.3		1.5		1.8		2.5		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.6		0.7		0.8		0.9		1.3		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.8		0.9		1.0		1.2		1.6		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	1.4		1.6		1.8		2.2		3.0		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-40 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.3		2.7		3.0		3.6		5.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.0		3.6		5.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	3.2		3.7		4.2		5.0		6.9		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.7		4.2		4.9		6.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3		11.9		13.5		15.8		22.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2		3.7		4.2		5.0		6.9		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.7		4.2		4.9		6.9		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HLH|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t _{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d _{TLH} ³	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t _{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d _{TLH} ³	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V _{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

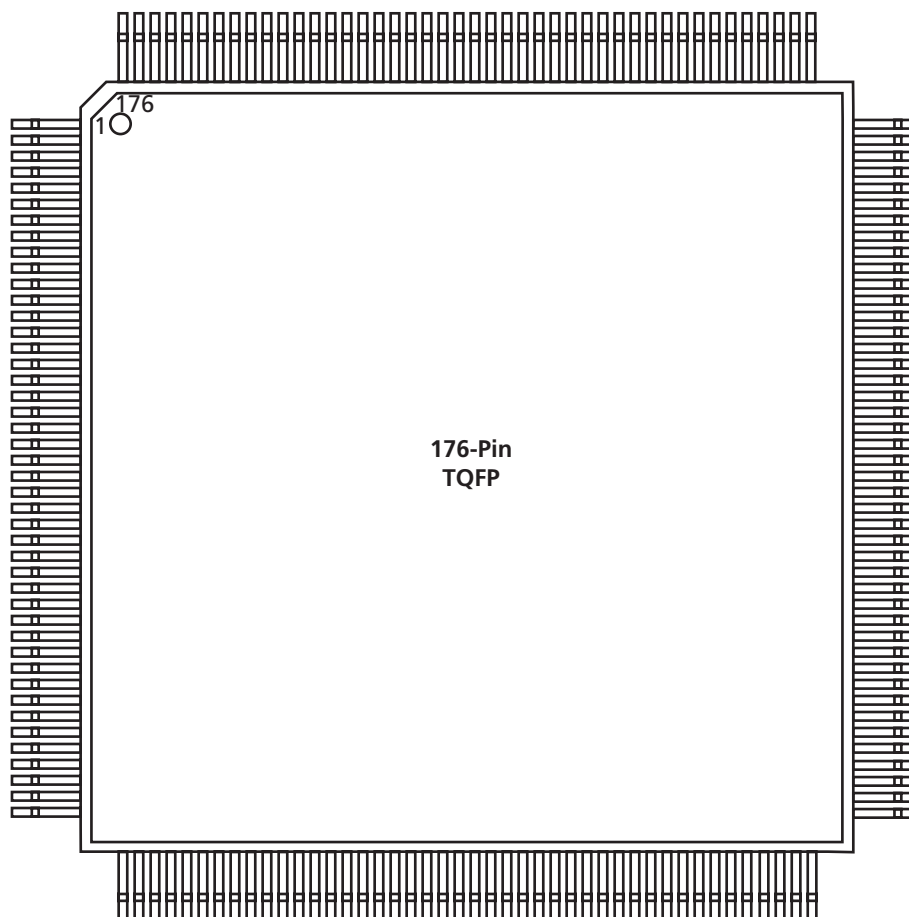


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA	
Pin Number	A545X32A Function
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V _{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V _{CCA}	V _{CCA}	V _{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D1	I/O	I/O	I/O
D2	V _{CCI}	V _{CCI}	V _{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V _{CCI}	V _{CCI}	V _{CCI}
E7	V _{CCI}	V _{CCI}	V _{CCI}
E8	V _{CCI}	V _{CCI}	V _{CCI}
E9	V _{CCA}	V _{CCA}	V _{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V _{CCI}	V _{CCI}
AD24	NC*	I/O
AD25	NC*	I/O
AD26	NC*	I/O
AE1	NC*	NC
AE2	I/O	I/O
AE3	NC*	I/O
AE4	NC*	I/O
AE5	NC*	I/O
AE6	NC*	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	NC*	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	NC*	I/O
AE16	NC*	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	NC*	I/O
AE22	NC*	I/O
AE23	NC*	I/O
AE24	NC*	I/O
AE25	NC*	NC
AE26	NC*	NC

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AF1	NC*	NC
AF2	NC*	NC
AF3	NC	I/O
AF4	NC*	I/O
AF5	NC*	I/O
AF6	NC*	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	NC*	I/O
AF12	NC*	NC
AF13	HCLK	HCLK
AF14	I/O	QCLKB
AF15	NC*	I/O
AF16	NC*	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	NC*	I/O
AF21	NC*	I/O
AF22	NC*	I/O
AF23	NC*	I/O
AF24	NC*	I/O
AF25	NC*	NC
AF26	NC*	NC
B1	NC*	NC
B2	NC*	NC
B3	NC*	I/O
B4	NC*	I/O
B5	NC*	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
B10	I/O	I/O
B11	NC*	I/O
B12	NC*	I/O
B13	V _{CCI}	V _{CCI}
B14	CLKA	CLKA
B15	NC*	I/O
B16	NC*	I/O
B17	I/O	I/O
B18	V _{CCI}	V _{CCI}
B19	I/O	I/O
B20	I/O	I/O
B21	NC*	I/O
B22	NC*	I/O
B23	NC*	I/O
B24	NC*	I/O
B25	I/O	I/O
B26	NC*	NC
C1	NC*	I/O
C2	NC*	I/O
C3	NC*	I/O
C4	NC*	I/O
C5	I/O	I/O
C6	V _{CCI}	V _{CCI}
C7	I/O	I/O
C8	I/O	I/O
C9	V _{CCI}	V _{CCI}
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	PRA, I/O	PRA, I/O
C14	I/O	I/O
C15	I/O	QCLKD
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC *	NC
K25	NC *	I/O
K26	NC *	I/O
L1	NC *	I/O
L2	NC *	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC *	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC *	I/O
M26	NC *	I/O
N1	I/O	I/O
N2	V _{CCI}	V _{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V _{CCA}	V _{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC *	NC
P1	NC *	I/O
P2	NC *	I/O
P3	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
P4	I/O	I/O
P5	V _{CCA}	V _{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V _{CCI}	V _{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC *	I/O
R2	NC *	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	NC *	I/O
R26	NC *	I/O
T1	NC *	I/O
T2	NC *	I/O

Note: *These pins must be left floating on the A54SX32A device.