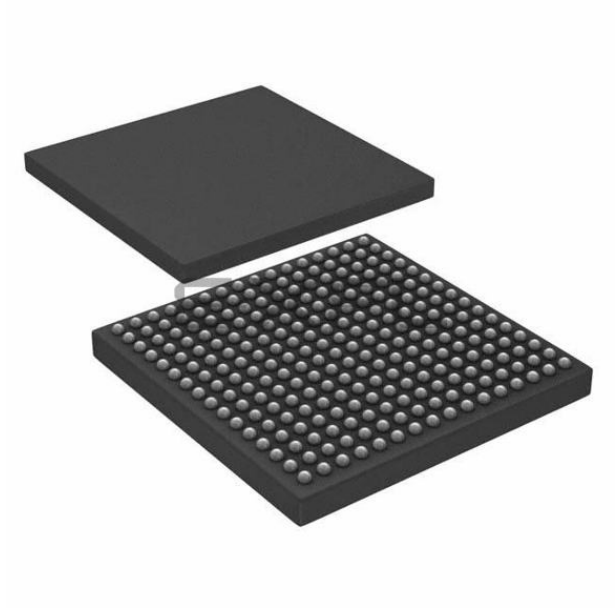

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 203 |
| Number of Gates | 48000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-fgg256 |

## Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

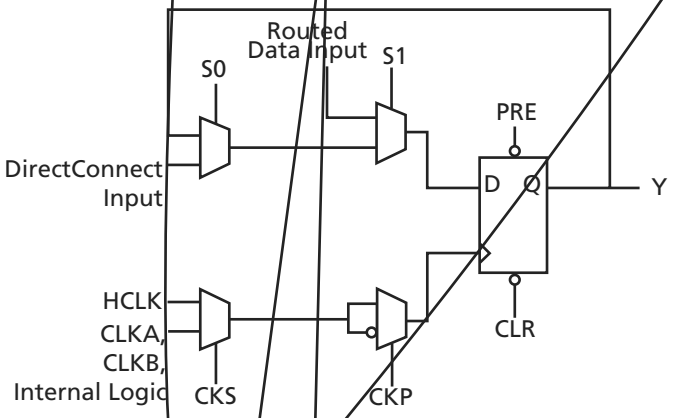


*Figure 1-2* • **R-Cell**

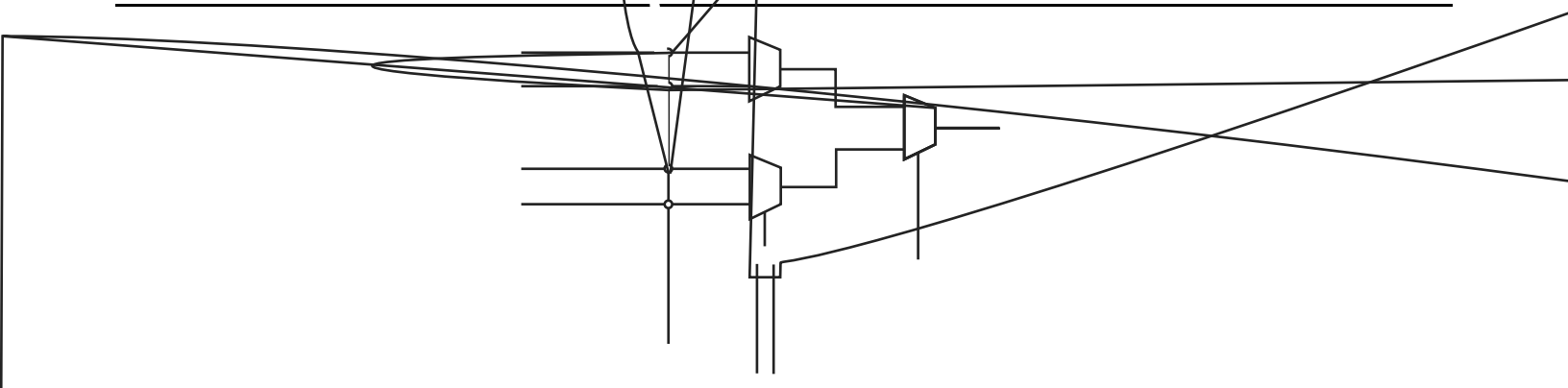

*Figure 1-3* • **C-Cell**

# Other Architectural Features

## Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 µ / 0.25 µ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

## Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

## User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).


*Figure 1-11* • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

## I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than $V_{CCI}$ and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and $V_{CCI}$ is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before $V_{CCA}$ reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

## JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

*Table 1-7* • **JTAG Instruction Code**

| **Instructions (IR4:IR0)** | **Binary Code** |
|---|---|
| EXTEST | 00000 |
| SAMPLE/PRELOAD | 00001 |
| INTEST | 00010 |
| USERCODE | 00011 |
| IDCODE | 00100 |
| HighZ | 01110 |
| CLAMP | 01111 |
| Diagnostic | 10000 |
| BYPASS | 11111 |
| Reserved | All others |

*Table 1-8* • **JTAG Instruction Code**

| **Device** | **Process** | **Revision** | **Bits 31-28** | **Bits 27-12** |
|---|---|---|---|---|
| A54SX08A | 0.22 µ | 0 | 8, 9 | 40B4, 42B4 |
| | | 1 | A, B | 40B4, 42B4 |
| A54SX16A | 0.22 µ | 0 | 9 | 40B8, 42B8 |
| | | 1 | B | 40B8, 42B8 |
| | 0.25 µ | 1 | B | 22B8 |
| A54SX32A | 0.2 2µ | 0 | 9 | 40BD, 42BD |
| | | 1 | B | 40BD, 42BD |
| | 0.25 µ | 1 | B | 22BD |
| A54SX72A | 0.22 µ | 0 | 9 | 40B2, 42B2 |
| | | 1 | B | 40B2, 42B2 |
| | 0.25 µ | 1 | B | 22B2 |

## Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$\theta_{JA}$ = 17.1°C/W is taken from Table 2-12 on page 2-11

$T_A$ = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°C - 125°C}{17.1°C/W} = 1.46\ W$$

*EQ 2-11*

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

## Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

## Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data $T_J$ and $T_A$ are given as follows:

$T_J$ = 110°C

$T_A$ = 70°C

From the datasheet:

$\theta_{JA}$ = 18.0°C/W

$\theta_{JC}$ = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°C - 70°C}{18.0°C/W} = 2.22\ W$$

*EQ 2-12*

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°C - 70°C}{3.00\ W} = 13.33°C/W$$

*EQ 2-13*

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 2-14*

where:

$\theta_{CS}$ = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

*Table 2-16* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.6 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.5 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |

*Table 2-17* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.5 | | 2.3 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 1.0 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-25* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **2.5 V LVCMOS Output Module Timing [2, 3]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 11.6 | | 13.4 | | 15.2 | | 17.9 | | 25.0 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[4] | Delta Low to High | | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[4] | Delta High to Low | | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[4] | Delta High to Low—low slew | | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

*Table 2-29* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.0 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-35* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.0 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-38* • **A54SX72A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{QCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.4 | | 3.4 | ns |
| $t_{QCHKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.5 | ns |
| $t_{QPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{QPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{QCKSW}$ | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{QCKSW}$ | Maximum Skew (50% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{QCKSW}$ | Maximum Skew (100% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

# 100-Pin TQFP

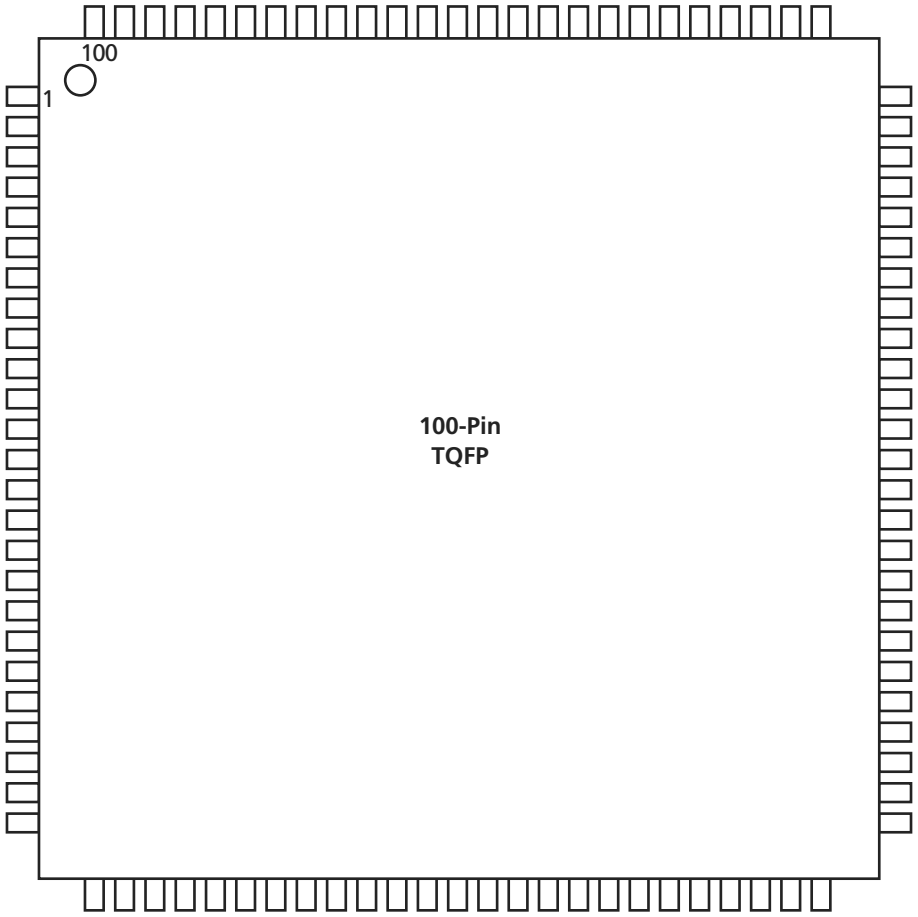


*Figure 3-2* • **100-Pin TQFP**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 144-Pin TQFP

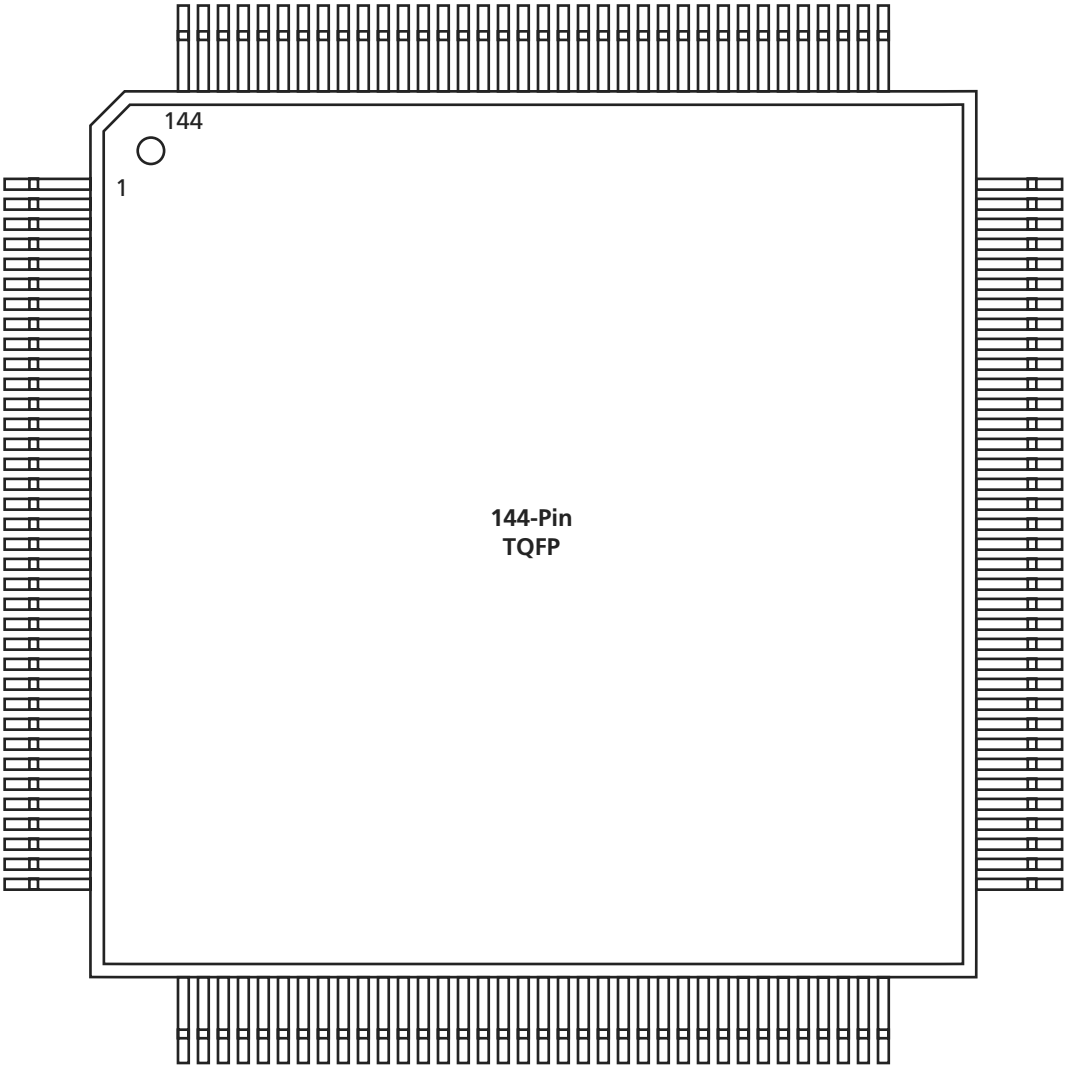


*Figure 3-3* • **144-Pin TQFP (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | NC | NC | NC |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | TRST, I/O | TRST, I/O | TRST, I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |
| 37 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | NC | NC | NC |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 1 | GND |
| 2 | TDI, I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | TMS |
| 11 | $V_{CCI}$ |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | GND |
| 22 | $V_{CCA}$ |
| 23 | GND |
| 24 | I/O |
| 25 | TRST, I/O |
| 26 | I/O |
| 27 | I/O |
| 28 | I/O |
| 29 | I/O |
| 30 | I/O |
| 31 | I/O |
| 32 | $V_{CCI}$ |
| 33 | $V_{CCA}$ |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | GND |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | $V_{CCI}$ |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |
| 59 | I/O |
| 60 | I/O |
| 61 | I/O |
| 62 | I/O |
| 63 | I/O |
| 64 | PRB, I/O |
| 65 | GND |
| 66 | $V_{CCA}$ |
| 67 | NC |
| 68 | I/O |
| 69 | HCLK |
| 70 | I/O |
| 71 | I/O |
| 72 | I/O |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | I/O |
| 80 | I/O |
| 81 | I/O |
| 82 | $V_{CCI}$ |
| 83 | I/O |
| 84 | I/O |
| 85 | I/O |
| 86 | I/O |
| 87 | TDO, I/O |
| 88 | I/O |
| 89 | GND |
| 90 | I/O |
| 91 | I/O |
| 92 | I/O |
| 93 | I/O |
| 94 | I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | $V_{CCA}$ |
| 99 | $V_{CCI}$ |
| 100 | I/O |
| 101 | I/O |
| 102 | I/O |
| 103 | I/O |
| 104 | I/O |
| 105 | I/O |
| 106 | I/O |
| 107 | I/O |
| 108 | GND |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 109 | $V_{CCA}$ |
| 110 | GND |
| 111 | I/O |
| 112 | I/O |
| 113 | I/O |
| 114 | I/O |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | I/O |
| 119 | I/O |
| 120 | I/O |
| 121 | I/O |
| 122 | $V_{CCA}$ |
| 123 | GND |
| 124 | $V_{CCI}$ |
| 125 | I/O |
| 126 | I/O |
| 127 | I/O |
| 128 | I/O |
| 129 | I/O |
| 130 | I/O |
| 131 | I/O |
| 132 | I/O |
| 133 | GND |
| 134 | I/O |
| 135 | I/O |
| 136 | I/O |
| 137 | I/O |
| 138 | I/O |
| 139 | I/O |
| 140 | $V_{CCI}$ |
| 141 | I/O |
| 142 | I/O |
| 143 | I/O |
| 144 | I/O |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | I/O |
| 149 | I/O |
| 150 | I/O |
| 151 | I/O |
| 152 | CLKA |
| 153 | CLKB |
| 154 | NC |
| 155 | GND |
| 156 | $V_{CCA}$ |
| 157 | PRA, I/O |
| 158 | I/O |
| 159 | I/O |
| 160 | I/O |
| 161 | I/O |
| 162 | I/O |
| 163 | I/O |
| 164 | I/O |
| 165 | I/O |
| 166 | I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | $V_{CCI}$ |
| 170 | I/O |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | TCK, I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| D11 | $V_{CCA}$ |
| D12 | NC |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | $V_{CCI}$ |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | $V_{CCA}$ |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | NC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| L14 | GND |
| L20 | NC |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | $V_{CCA}$ |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | $V_{CCA}$ |
| M21 | I/O |
| M22 | I/O |
| M23 | $V_{CCI}$ |
| N1 | I/O |
| N2 | TRST, I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |
| T22 | I/O |
| T23 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | $V_{CCA}$ |
| U4 | I/O |
| U20 | I/O |
| U21 | $V_{CCA}$ |
| U22 | I/O |
| U23 | I/O |
| V1 | $V_{CCI}$ |
| V2 | I/O |
| V3 | I/O |
| V4 | I/O |
| V20 | I/O |
| V21 | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| A1 | NC* | NC |
| A2 | NC* | NC |
| A3 | NC* | I/O |
| A4 | NC* | I/O |
| A5 | NC* | I/O |
| A6 | I/O | I/O |
| A7 | I/O | I/O |
| A8 | I/O | I/O |
| A9 | I/O | I/O |
| A10 | I/O | I/O |
| A11 | NC* | I/O |
| A12 | NC* | I/O |
| A13 | I/O | I/O |
| A14 | NC* | NC |
| A15 | NC* | I/O |
| A16 | NC* | I/O |
| A17 | I/O | I/O |
| A18 | I/O | I/O |
| A19 | I/O | I/O |
| A20 | I/O | I/O |
| A21 | NC* | I/O |
| A22 | NC* | I/O |
| A23 | NC* | I/O |
| A24 | NC* | I/O |
| A25 | NC* | NC |
| A26 | NC* | NC |
| AA1 | NC* | I/O |
| AA2 | NC* | I/O |
| AA3 | $V_{CCA}$ | $V_{CCA}$ |
| AA4 | I/O | I/O |
| AA5 | I/O | I/O |
| AA22 | I/O | I/O |
| AA23 | I/O | I/O |
| AA24 | I/O | I/O |
| AA25 | NC* | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AA26 | NC* | I/O |
| AB1 | NC* | NC |
| AB2 | $V_{CCI}$ | $V_{CCI}$ |
| AB3 | I/O | I/O |
| AB4 | I/O | I/O |
| AB5 | NC* | I/O |
| AB6 | I/O | I/O |
| AB7 | I/O | I/O |
| AB8 | I/O | I/O |
| AB9 | I/O | I/O |
| AB10 | I/O | I/O |
| AB11 | I/O | I/O |
| AB12 | PRB, I/O | PRB, I/O |
| AB13 | $V_{CCA}$ | $V_{CCA}$ |
| AB14 | I/O | I/O |
| AB15 | I/O | I/O |
| AB16 | I/O | I/O |
| AB17 | I/O | I/O |
| AB18 | I/O | I/O |
| AB19 | I/O | I/O |
| AB20 | TDO, I/O | TDO, I/O |
| AB21 | GND | GND |
| AB22 | NC* | I/O |
| AB23 | I/O | I/O |
| AB24 | I/O | I/O |
| AB25 | NC* | I/O |
| AB26 | NC* | I/O |
| AC1 | I/O | I/O |
| AC2 | I/O | I/O |
| AC3 | I/O | I/O |
| AC4 | NC* | I/O |
| AC5 | $V_{CCI}$ | $V_{CCI}$ |
| AC6 | I/O | I/O |
| AC7 | $V_{CCI}$ | $V_{CCI}$ |
| AC8 | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| AC9 | I/O | I/O |
| AC10 | I/O | I/O |
| AC11 | I/O | I/O |
| AC12 | I/O | QCLKA |
| AC13 | I/O | I/O |
| AC14 | I/O | I/O |
| AC15 | I/O | I/O |
| AC16 | I/O | I/O |
| AC17 | I/O | I/O |
| AC18 | I/O | I/O |
| AC19 | I/O | I/O |
| AC20 | $V_{CCI}$ | $V_{CCI}$ |
| AC21 | I/O | I/O |
| AC22 | I/O | I/O |
| AC23 | NC* | I/O |
| AC24 | I/O | I/O |
| AC25 | NC* | I/O |
| AC26 | NC* | I/O |
| AD1 | I/O | I/O |
| AD2 | I/O | I/O |
| AD3 | GND | GND |
| AD4 | I/O | I/O |
| AD5 | I/O | I/O |
| AD6 | I/O | I/O |
| AD7 | I/O | I/O |
| AD8 | I/O | I/O |
| AD9 | $V_{CCI}$ | $V_{CCI}$ |
| AD10 | I/O | I/O |
| AD11 | I/O | I/O |
| AD12 | I/O | I/O |
| AD13 | $V_{CCI}$ | $V_{CCI}$ |
| AD14 | I/O | I/O |
| AD15 | I/O | I/O |
| AD16 | I/O | I/O |
| AD17 | $V_{CCI}$ | $V_{CCI}$ |

***Note:*** **These pins must be left floating on the A54SX32A device.*

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| K10 | GND | GND |
| K11 | GND | GND |
| K12 | GND | GND |
| K13 | GND | GND |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | GND | GND |
| K17 | GND | GND |
| K22 | I/O | I/O |
| K23 | I/O | I/O |
| K24 | NC* | NC |
| K25 | NC* | I/O |
| K26 | NC* | I/O |
| L1 | NC* | I/O |
| L2 | NC* | I/O |
| L3 | I/O | I/O |
| L4 | I/O | I/O |
| L5 | I/O | I/O |
| L10 | GND | GND |
| L11 | GND | GND |
| L12 | GND | GND |
| L13 | GND | GND |
| L14 | GND | GND |
| L15 | GND | GND |
| L16 | GND | GND |
| L17 | GND | GND |
| L22 | I/O | I/O |
| L23 | I/O | I/O |
| L24 | I/O | I/O |
| L25 | I/O | I/O |
| L26 | I/O | I/O |
| M1 | NC* | NC |
| M2 | I/O | I/O |
| M3 | I/O | I/O |
| M4 | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| M5 | I/O | I/O |
| M10 | GND | GND |
| M11 | GND | GND |
| M12 | GND | GND |
| M13 | GND | GND |
| M14 | GND | GND |
| M15 | GND | GND |
| M16 | GND | GND |
| M17 | GND | GND |
| M22 | I/O | I/O |
| M23 | I/O | I/O |
| M24 | I/O | I/O |
| M25 | NC* | I/O |
| M26 | NC* | I/O |
| N1 | I/O | I/O |
| N2 | $V_{CCI}$ | $V_{CCI}$ |
| N3 | I/O | I/O |
| N4 | I/O | I/O |
| N5 | I/O | I/O |
| N10 | GND | GND |
| N11 | GND | GND |
| N12 | GND | GND |
| N13 | GND | GND |
| N14 | GND | GND |
| N15 | GND | GND |
| N16 | GND | GND |
| N17 | GND | GND |
| N22 | $V_{CCA}$ | $V_{CCA}$ |
| N23 | I/O | I/O |
| N24 | I/O | I/O |
| N25 | I/O | I/O |
| N26 | NC* | NC |
| P1 | NC* | I/O |
| P2 | NC* | I/O |
| P3 | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| P4 | I/O | I/O |
| P5 | $V_{CCA}$ | $V_{CCA}$ |
| P10 | GND | GND |
| P11 | GND | GND |
| P12 | GND | GND |
| P13 | GND | GND |
| P14 | GND | GND |
| P15 | GND | GND |
| P16 | GND | GND |
| P17 | GND | GND |
| P22 | I/O | I/O |
| P23 | I/O | I/O |
| P24 | $V_{CCI}$ | $V_{CCI}$ |
| P25 | I/O | I/O |
| P26 | I/O | I/O |
| R1 | NC* | I/O |
| R2 | NC* | I/O |
| R3 | I/O | I/O |
| R4 | I/O | I/O |
| R5 | TRST, I/O | TRST, I/O |
| R10 | GND | GND |
| R11 | GND | GND |
| R12 | GND | GND |
| R13 | GND | GND |
| R14 | GND | GND |
| R15 | GND | GND |
| R16 | GND | GND |
| R17 | GND | GND |
| R22 | I/O | I/O |
| R23 | I/O | I/O |
| R24 | I/O | I/O |
| R25 | NC* | I/O |
| R26 | NC* | I/O |
| T1 | NC* | I/O |
| T2 | NC* | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*