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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-tq100

Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Speed Grade and Temperature Grade Matrix

	F	Std	-1	-2	-3
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

Notes:

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.

General Description

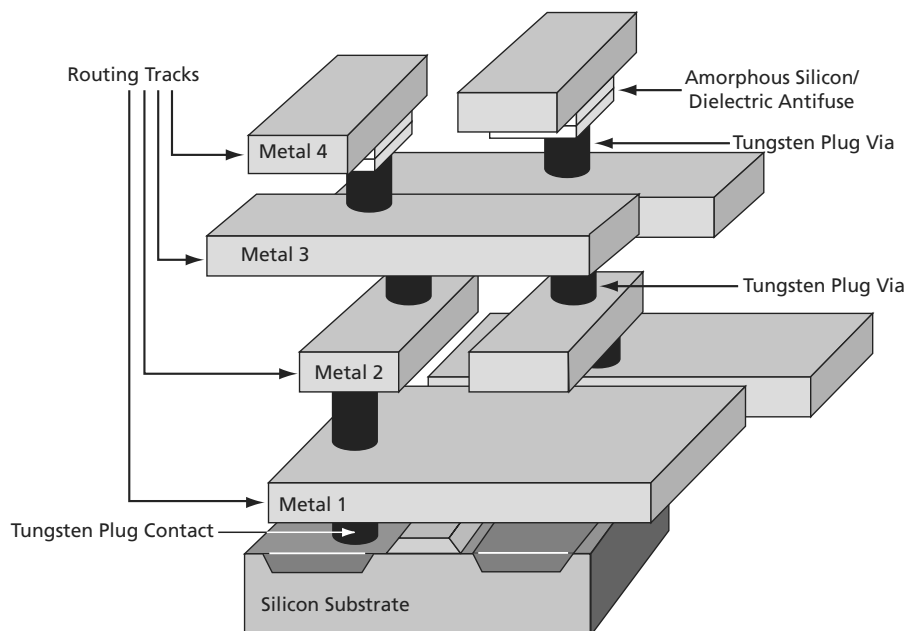
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices and Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • **SX-A Clock Resources**

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

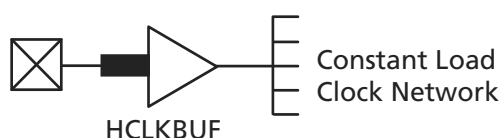


Figure 1-7 • **SX-A HCLK Clock Buffer**

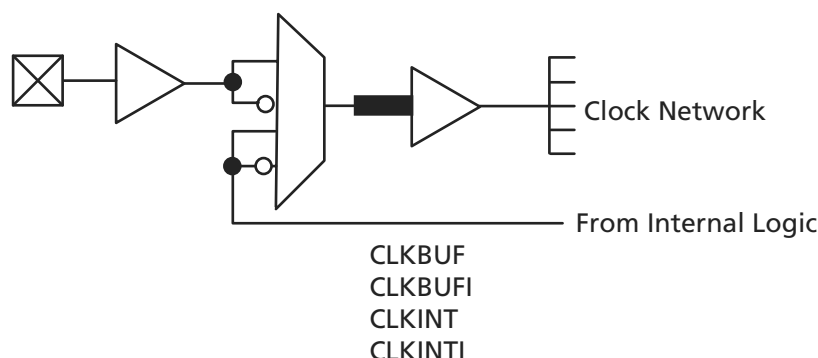


Figure 1-8 • **SX-A Routed Clock Buffer**

Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using $0.22\ \mu\text{m}$ / $0.25\ \mu\text{m}$ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of $25\ \Omega$ with capacitance of $1.0\ \text{fF}$ for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CC1} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CC1} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately $50\ \text{k}\Omega$ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 • JTAG Instruction Code

Instructions (IR4:IR0)	Binary Code
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HighZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-8 • JTAG Instruction Code

Device	Process	Revision	Bits 31-28	Bits 27-12
A54SX08A	0.22 μ	0	8, 9	40B4, 42B4
		1	A, B	40B4, 42B4
A54SX16A	0.22 μ	0	9	40B8, 42B8
		1	B	40B8, 42B8
	0.25 μ	1	B	22B8
A54SX32A	0.2 2 μ	0	9	40BD, 42BD
		1	B	40BD, 42BD
	0.25 μ	1	B	22BD
A54SX72A	0.22 μ	0	9	40B2, 42B2
		1	B	40B2, 42B2
	0.25 μ	1	B	22B2

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

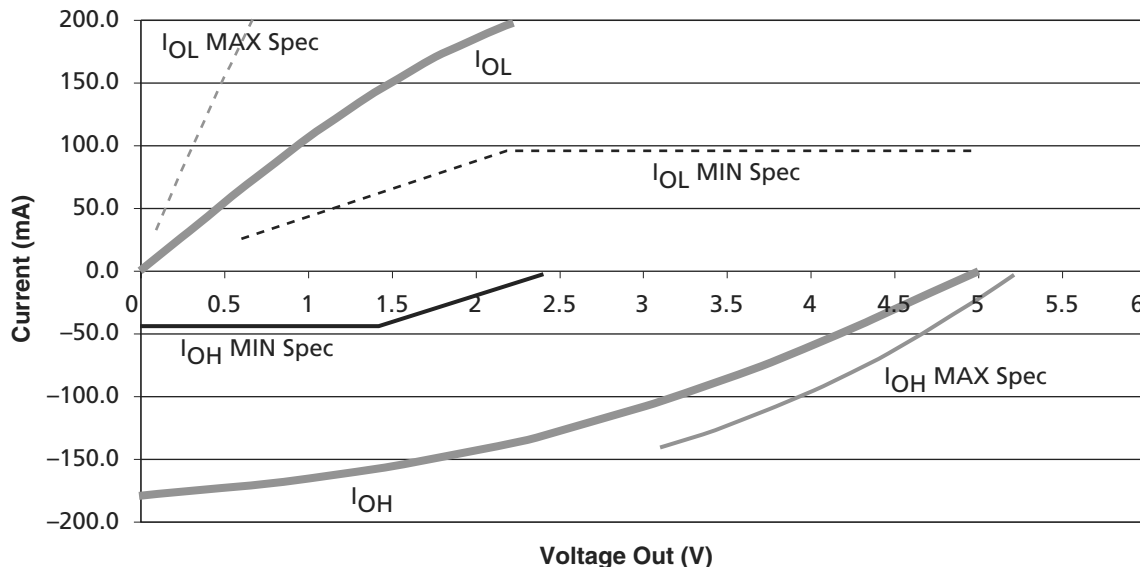


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CCI}$	–	V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CCI}$	-10	+10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$	–	V
V_{OL}	Output Low Voltage	$I_{OUT} = 1,500 \mu A$		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance ³		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Input Buffer Delays

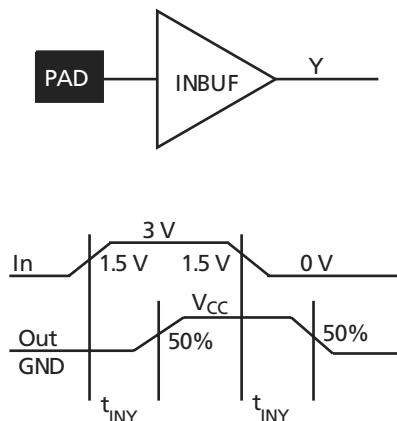


Figure 2-6 • Input Buffer Delays

C-Cell Delays

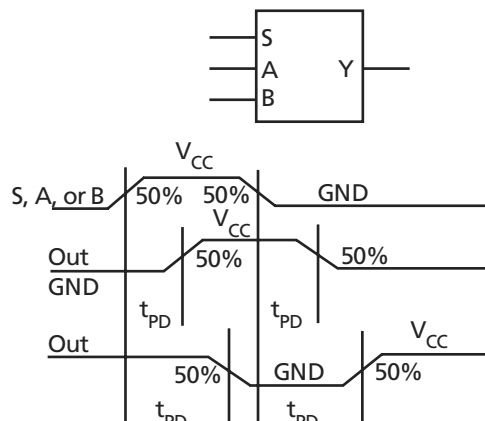


Figure 2-7 • C-Cell Delays

Cell Timing Characteristics

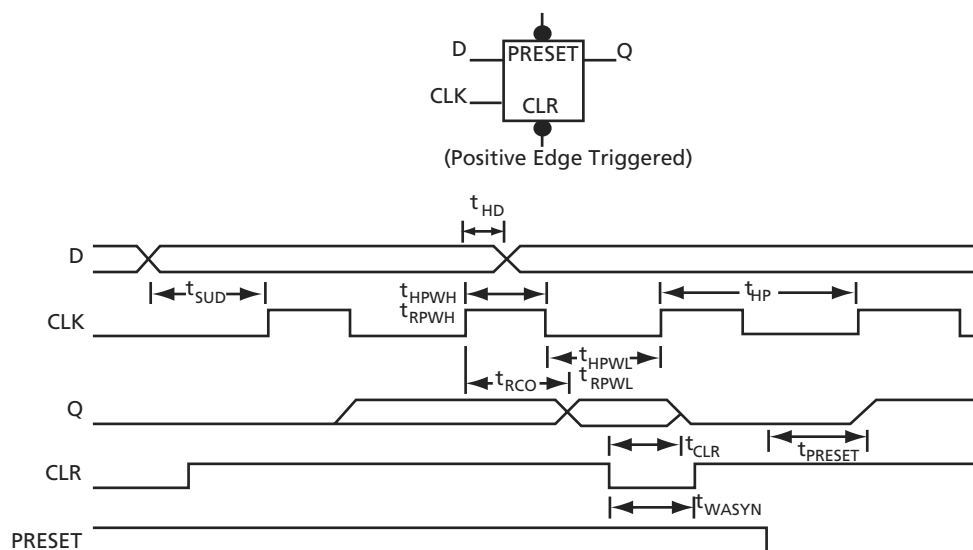


Figure 2-8 • Flip-Flops

Table 2-20 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH} ²	Delta Low to High	0.016		0.02		0.022		0.032		ns/pF
d _{THL} ²	Delta High to Low	0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.6		8.6		10.1		14.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH}	Delta Low to High	0.017		0.017		0.023		0.031		ns/pF
d _{THL}	Delta High to Low	0.029		0.031		0.037		0.051		ns/pF
d _{THLS}	Delta High to Low—low slew	0.046		0.057		0.066		0.089		ns/pF

Notes:

- Delays based on 50 pF loading.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-31 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-36 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		2.9		3.4		4.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.7		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.3		3.8		4.5		6.2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.0		4.7		6.6	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.8		2.1		2.4		2.8		3.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.8		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.6		3.0		3.3		3.9		5.5	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.2		5.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-40 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.3		2.7		3.0		3.6		5.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.0		3.6		5.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	3.2		3.7		4.2		5.0		6.9		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.7		4.2		4.9		6.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3		11.9		13.5		15.8		22.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2		3.7		4.2		5.0		6.9		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.7		4.2		4.9		6.9		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HLH|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Package Pin Assignments

208-Pin PQFP

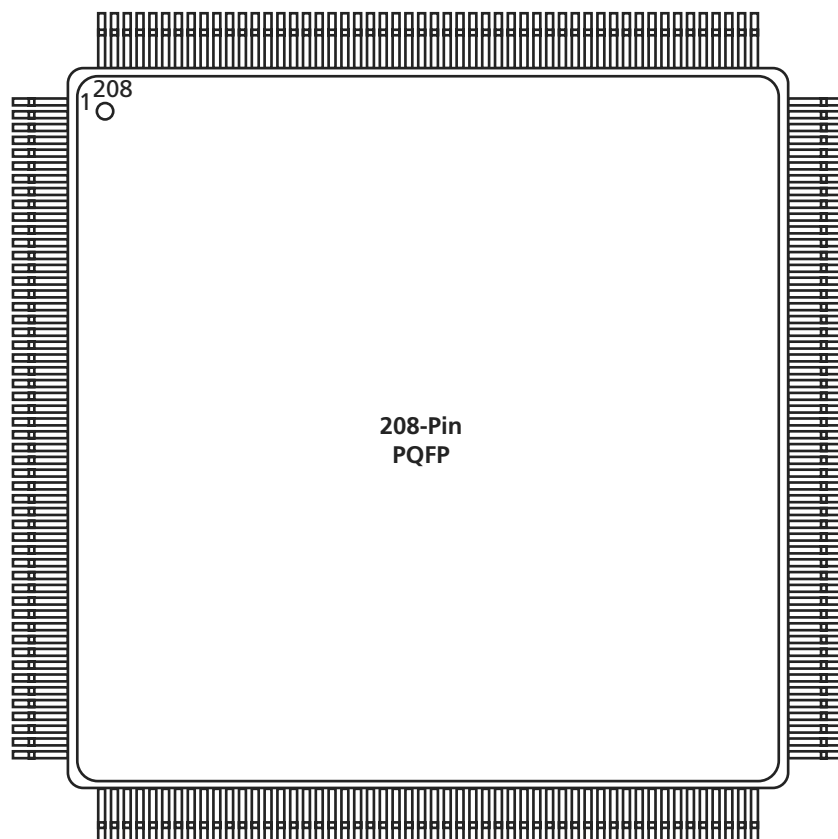


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V _{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

100-Pin TQFP

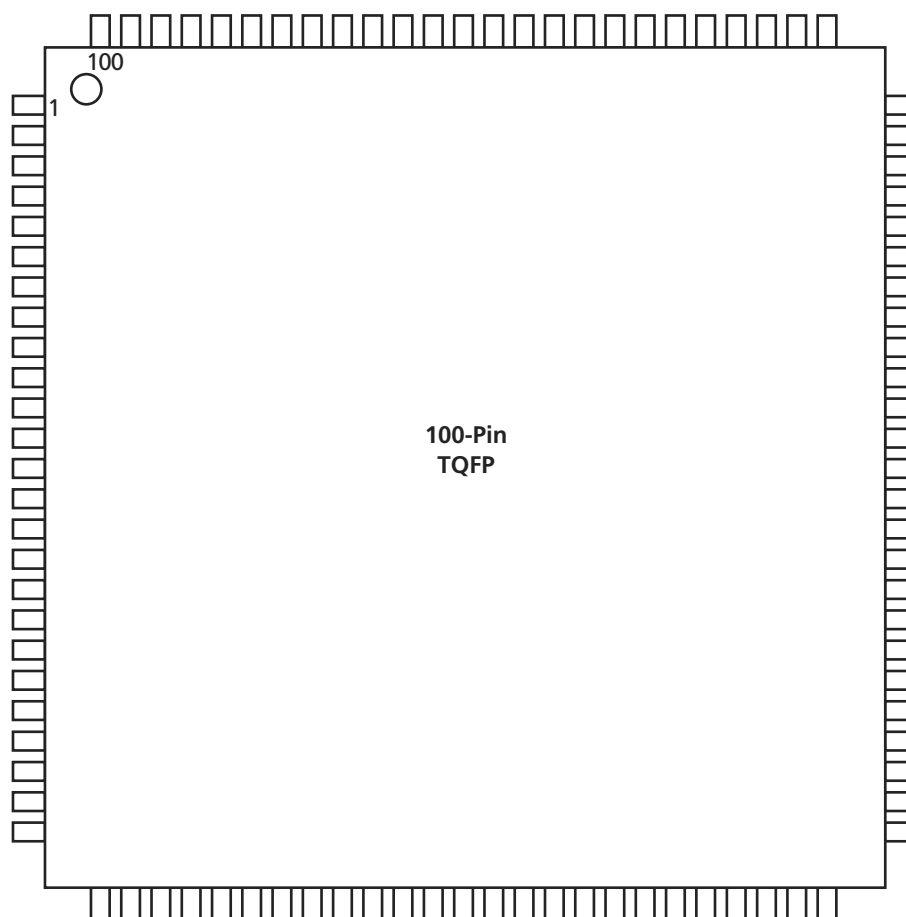


Figure 3-2 • 100-Pin TQFP

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP		176-Pin TQFP		176-Pin TQFP		176-Pin TQFP	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
1	GND	37	I/O	73	I/O	109	V _{CCA}
2	TDI, I/O	38	I/O	74	I/O	110	GND
3	I/O	39	I/O	75	I/O	111	I/O
4	I/O	40	I/O	76	I/O	112	I/O
5	I/O	41	I/O	77	I/O	113	I/O
6	I/O	42	I/O	78	I/O	114	I/O
7	I/O	43	I/O	79	I/O	115	I/O
8	I/O	44	GND	80	I/O	116	I/O
9	I/O	45	I/O	81	I/O	117	I/O
10	TMS	46	I/O	82	V _{CCI}	118	I/O
11	V _{CCI}	47	I/O	83	I/O	119	I/O
12	I/O	48	I/O	84	I/O	120	I/O
13	I/O	49	I/O	85	I/O	121	I/O
14	I/O	50	I/O	86	I/O	122	V _{CCA}
15	I/O	51	I/O	87	TDO, I/O	123	GND
16	I/O	52	V _{CCI}	88	I/O	124	V _{CCI}
17	I/O	53	I/O	89	GND	125	I/O
18	I/O	54	I/O	90	I/O	126	I/O
19	I/O	55	I/O	91	I/O	127	I/O
20	I/O	56	I/O	92	I/O	128	I/O
21	GND	57	I/O	93	I/O	129	I/O
22	V _{CCA}	58	I/O	94	I/O	130	I/O
23	GND	59	I/O	95	I/O	131	I/O
24	I/O	60	I/O	96	I/O	132	I/O
25	TRST, I/O	61	I/O	97	I/O	133	GND
26	I/O	62	I/O	98	V _{CCA}	134	I/O
27	I/O	63	I/O	99	V _{CCI}	135	I/O
28	I/O	64	PRB, I/O	100	I/O	136	I/O
29	I/O	65	GND	101	I/O	137	I/O
30	I/O	66	V _{CCA}	102	I/O	138	I/O
31	I/O	67	NC	103	I/O	139	I/O
32	V _{CCI}	68	I/O	104	I/O	140	V _{CCI}
33	V _{CCA}	69	HCLK	105	I/O	141	I/O
34	I/O	70	I/O	106	I/O	142	I/O
35	I/O	71	I/O	107	I/O	143	I/O
36	I/O	72	I/O	108	GND	144	I/O

329-Pin PBGA	
Pin Number	A545X32A Function
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V _{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V _{CCA}	V _{CCA}	V _{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

484-Pin FBGA

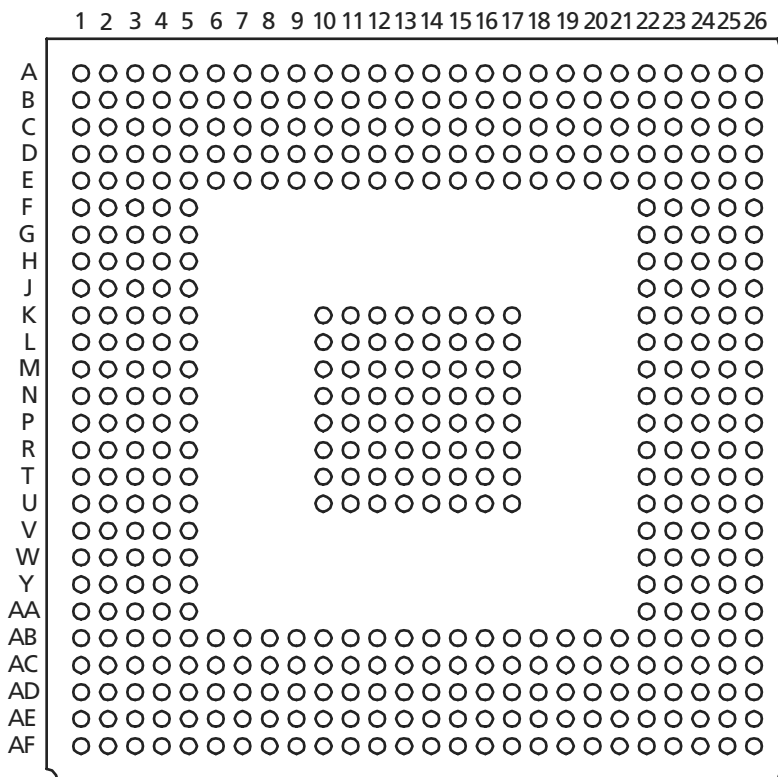


Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC
A2	NC*	NC
A3	NC*	I/O
A4	NC*	I/O
A5	NC*	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC*	I/O
A12	NC*	I/O
A13	I/O	I/O
A14	NC*	NC
A15	NC*	I/O
A16	NC*	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC*	I/O
A22	NC*	I/O
A23	NC*	I/O
A24	NC*	I/O
A25	NC*	NC
A26	NC*	NC
AA1	NC*	I/O
AA2	NC*	I/O
AA3	V _{CCA}	V _{CCA}
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AA26	NC*	I/O
AB1	NC*	NC
AB2	V _{CCI}	V _{CCI}
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC*	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V _{CCA}	V _{CCA}
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC*	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC*	I/O
AB26	NC*	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC*	I/O
AC5	V _{CCI}	V _{CCI}
AC6	I/O	I/O
AC7	V _{CCI}	V _{CCI}
AC8	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V _{CCI}	V _{CCI}
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC*	I/O
AC24	I/O	I/O
AC25	NC*	I/O
AC26	NC*	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V _{CCI}	V _{CCI}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V _{CCI}	V _{CCI}
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V _{CCI}	V _{CCI}

Note: *These pins must be left floating on the A54SX32A device.