Microchip Technology - A54SX32A-TQ144 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-tq144

Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 μ / 0.25 μ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).

Figure 1-11 • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Electrical Specifications

Table 2-5 • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

Symbol	**Parameter**		**Commercial**		**Industrial**		**Units**
			Min.	**Max.**	**Min.**	**Max.**	
V_{OH}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	0.9 V_{CCI}		0.9 V_{CCI}		V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –8 mA)	2.4		2.4		V
V_{OL}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12 mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Table 2-6 • **2.5 V LVCMOS2 Electrical Specifications**

Symbol	**Parameter**		**Commercial**		**Industrial**		**Units**
			Min.	**Max.**	**Min.**	**Max.**	
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –100 µA)	2.1		2.1		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	2.0		2.0		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} =–-2 mA)	1.7		1.7		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 100 µA)		0.2		0.2	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \leq V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \geq V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

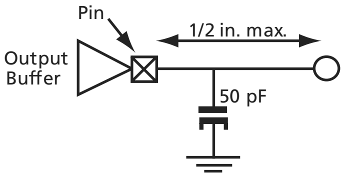
Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Table 2-8 • **AC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ [1]	–44	–	mA
		$1.4 \leq V_{OUT} < 2.4$ [1, 2]	$(-44 + (V_{OUT} - 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ [3]	–	–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ [1]	95	–	mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ [1, 3]	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ [3]	–	206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



Where:

C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF

C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of CLKA/B in pF

C_{EQHV} = Variable capacitance of HCLK in pF

C_{EQHF} = Fixed capacitance of HCLK in pF

C_{L} = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average CLKA rate in MHz

f_{q2} = Average CLKB rate in MHz

f_{s1} = Average HCLK rate in MHz

m = Number of logic modules switching at fm

n = Number of input buffers switching at fn

p = Number of output buffers switching at fp

q_1 = Number of clock loads on CLKA

q_2 = Number of clock loads on CLKB

r_1 = Fixed capacitance due to CLKA

r_2 = Fixed capacitance due to CLKB

s_1 = Number of clock loads on HCLK

x = Number of I/Os at logic low

y = Number of I/Os at logic high

Table 2-11 • **CEQ Values for SX-A Devices**

	A54SX08A	**A54SX16A**	**A54SX32A**	**A54SX72A**
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

θ_{JA} = Junction-to-air thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_C = Ambient temperature
P = total power dissipated by the device

Table 2-12 • **Package Thermal Characteristics**

Package Type	**Pin Count**	θ_{JC}	θ_{JA} **Still Air**	θ_{JA} **1.0 m/s 200 ft./min.**	θ_{JA} **2.5 m/s 500 ft./min.**	**Units**
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

1. *The A54SX08A PQ208 has no heat spreader.*
2. *The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.*

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

θ_{JA} = 17.1°C/W is taken from Table 2-12 on page 2-11

T_A = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°\text{C} - 125°\text{C}}{17.1°\text{C/W}} = 1.46\ \text{W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

T_J = 110°C

T_A = 70°C

From the datasheet:

θ_{JA} = 18.0°C/W

θ_{JC} = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°\text{C} - 70°\text{C}}{18.0°\text{C/W}} = 2.22\ \text{W}$$

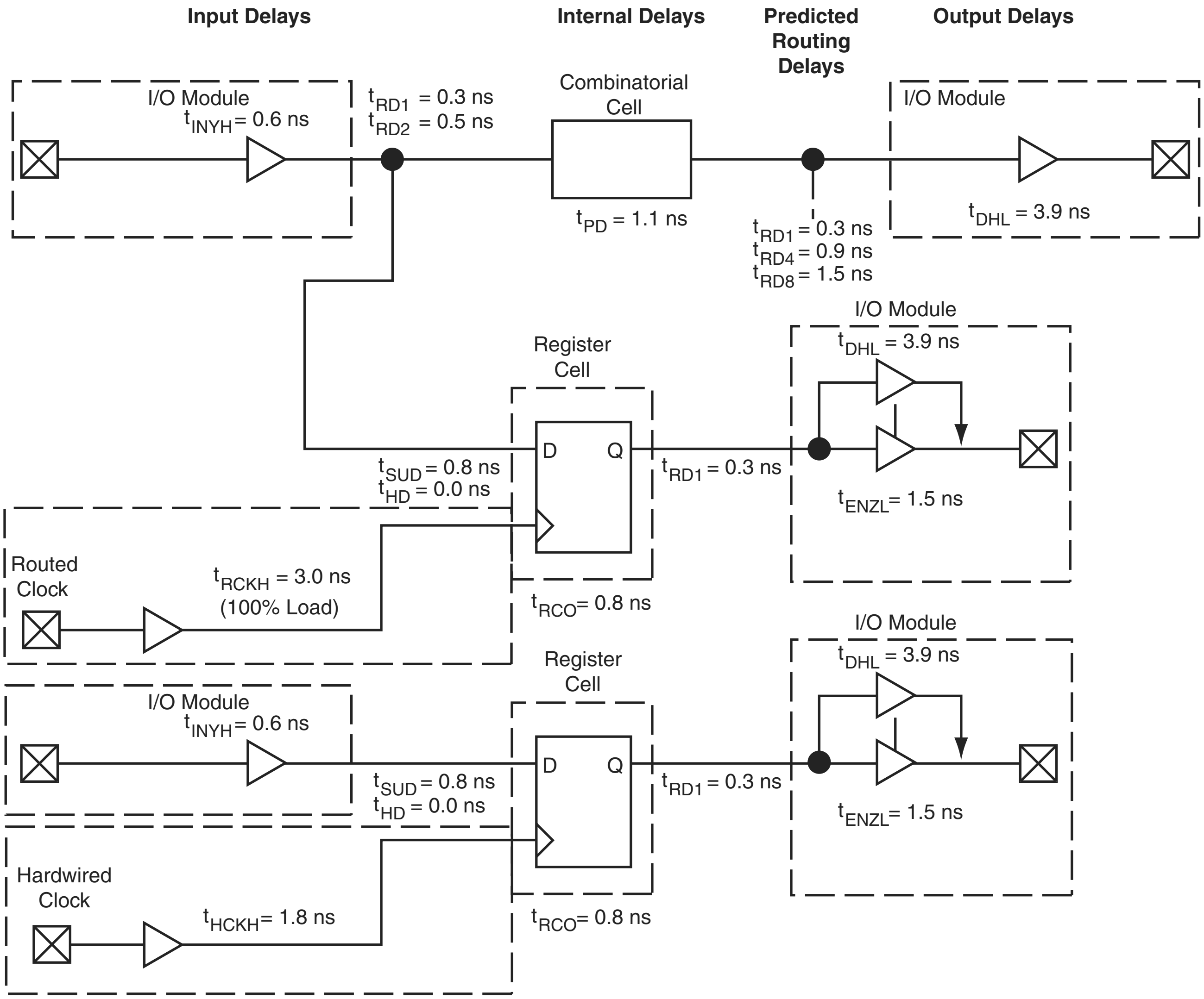
EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°\text{C} - 70°\text{C}}{3.00\ \text{W}} = 13.33°\text{C/W}$$

EQ 2-13

SX-A Timing Model



Note: **Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route.*

Figure 2-3 • **SX-A Timing Model**

Sample Path Calculations

Hardwired Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH}$
= 0.6 + 0.3 + 0.8 - 1.8 = – 0.1 ns

Clock-to-Out (Pad-to-Pad) = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 ns

Routed Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH}$
= 0.6 + 0.3 + 0.8 - 3.0 = –1.3 ns

Clock-to-Out (Pad-to-Pad) = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 ns

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.25 V)**

V_{CCA}	Junction Temperature (T_J)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-15 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-18 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	**Description**	**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		**Units**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
2.5 V LVCMOS Output Module Timing[1,2]										
t_{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[3]	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-24 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed* Min.	–3 Speed* Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-25 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing [2, 3]												
t_{DLH}	Data-to-Pad Low to High		3.4		3.9		4.5		5.2		7.3	ns
t_{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		11.6		13.4		15.2		17.9		25.0	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		3.9		4.5		5.2		7.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}[4]	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[4]	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[4]	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-30 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-37 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

		–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t_{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t_{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V_{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V_{CCI}	V_{CCI}
AD24	NC*	I/O
AD25	NC*	I/O
AD26	NC*	I/O
AE1	NC*	NC
AE2	I/O	I/O
AE3	NC*	I/O
AE4	NC*	I/O
AE5	NC*	I/O
AE6	NC*	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	NC*	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	NC*	I/O
AE16	NC*	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	NC*	I/O
AE22	NC*	I/O
AE23	NC*	I/O
AE24	NC*	I/O
AE25	NC*	NC
AE26	NC*	NC
AF1	NC*	NC
AF2	NC*	NC
AF3	NC	I/O
AF4	NC*	I/O
AF5	NC*	I/O
AF6	NC*	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	NC*	I/O
AF12	NC*	NC
AF13	HCLK	HCLK
AF14	I/O	QCLKB
AF15	NC*	I/O
AF16	NC*	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	NC*	I/O
AF21	NC*	I/O
AF22	NC*	I/O
AF23	NC*	I/O
AF24	NC*	I/O
AF25	NC*	NC
AF26	NC*	NC
B1	NC*	NC
B2	NC*	NC
B3	NC*	I/O
B4	NC*	I/O
B5	NC*	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	NC*	I/O
B12	NC*	I/O
B13	V_{CCI}	V_{CCI}
B14	CLKA	CLKA
B15	NC*	I/O
B16	NC*	I/O
B17	I/O	I/O
B18	V_{CCI}	V_{CCI}
B19	I/O	I/O
B20	I/O	I/O
B21	NC*	I/O
B22	NC*	I/O
B23	NC*	I/O
B24	NC*	I/O
B25	I/O	I/O
B26	NC*	NC
C1	NC*	I/O
C2	NC*	I/O
C3	NC*	I/O
C4	NC*	I/O
C5	I/O	I/O
C6	V_{CCI}	V_{CCI}
C7	I/O	I/O
C8	I/O	I/O
C9	V_{CCI}	V_{CCI}
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	PRA, I/O	PRA, I/O
C14	I/O	I/O
C15	I/O	QCLKD
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O

Note: **These pins must be left floating on the A54SX32A device.*

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
C19	I/O	I/O
C20	V_{CCI}	V_{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V_{CCI}	V_{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V_{CCI}	V_{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V_{CCA}	V_{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V_{CCI}	V_{CCI}
E26	GND	GND
F1	V_{CCI}	V_{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V_{CCA}	V_{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V_{CCI}	V_{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V_{CCI}	V_{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V_{CCA}	V_{CCA}

Note: **These pins must be left floating on the A54SX32A device.*