Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 113 |
| Number of Gates | 48000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-tq144a |

## Temperature Grade Offering

| Package | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---|---|---|---|---|
| PQ208 | C,I,A,M | C,I,A,M | C,I,A,M | C,I,A,M |
| TQ100 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ176 | | | C,I,M | |
| BG329 | | | C,I,M | |
| FG144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| FG256 | | C,I,A,M | C,I,A,M | C,I,A,M |
| FG484 | | | C,I,M | C,I,A,M |
| CQ208 | | | C,M,B | C,M,B |
| CQ256 | | | C,M,B | C,M,B |

***Notes:***

1. *C = Commercial*
2. *I = Industrial*
3. *A = Automotive*
4. *M = Military*
5. *B = MIL-STD-883 Class B*
6. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
7. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

## Speed Grade and Temperature Grade Matrix

| | F | Std | –1 | –2 | –3 |
|---|---|---|---|---|---|
| Commercial | ✓ | ✓ | ✓ | ✓ | Discontinued |
| Industrial | | ✓ | ✓ | ✓ | Discontinued |
| Automotive | | ✓ | | | |
| Military | | ✓ | ✓ | | |
| MIL-STD-883B | | ✓ | ✓ | | |

***Notes:***

1. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
2. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Contact your Actel Sales representative for more information on availability.

# Table of Contents

**General Description**

Introduction . . . . . . . . . . 1-1
SX-A Family Architecture . . . . . . . . . . 1-1
Other Architectural Features . . . . . . . . . . 1-7
Programming . . . . . . . . . . 1-13
Related Documents . . . . . . . . . . 1-14
Pin Description . . . . . . . . . . 1-15

**Detailed Specifications**

Operating Conditions . . . . . . . . . . 2-1
Typical SX-A Standby Current . . . . . . . . . . 2-1
Electrical Specifications . . . . . . . . . . 2-2
PCI Compliance for the SX-A Family . . . . . . . . . . 2-3
Thermal Characteristics . . . . . . . . . . 2-11
SX-A Timing Model . . . . . . . . . . 2-14
Sample Path Calculations . . . . . . . . . . 2-14
Output Buffer Delays . . . . . . . . . . 2-15
AC Test Loads . . . . . . . . . . 2-15
Input Buffer Delays . . . . . . . . . . 2-16
C-Cell Delays . . . . . . . . . . 2-16
Cell Timing Characteristics . . . . . . . . . . 2-16
Timing Characteristics . . . . . . . . . . 2-17
Temperature and Voltage Derating Factors . . . . . . . . . . 2-17
Timing Characteristics . . . . . . . . . . 2-18

**Package Pin Assignments**

208-Pin PQFP . . . . . . . . . . 3-1
100-Pin TQFP . . . . . . . . . . 3-5
144-Pin TQFP . . . . . . . . . . 3-8
176-Pin TQFP . . . . . . . . . . 3-11
329-Pin PBGA . . . . . . . . . . 3-14
144-Pin FBGA . . . . . . . . . . 3-18
256-Pin FBGA . . . . . . . . . . 3-21
484-Pin FBGA . . . . . . . . . . 3-26

**Datasheet Information**

List of Changes . . . . . . . . . . 4-1
Datasheet Categories . . . . . . . . . . 4-3
International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR) . . . . . . . . . . 4-3

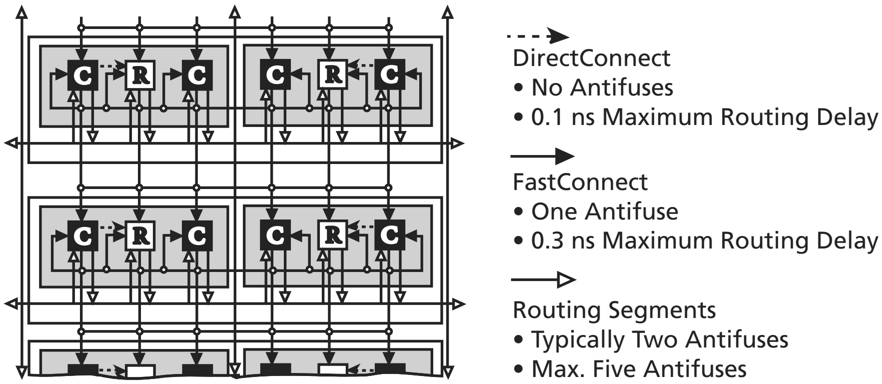



*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

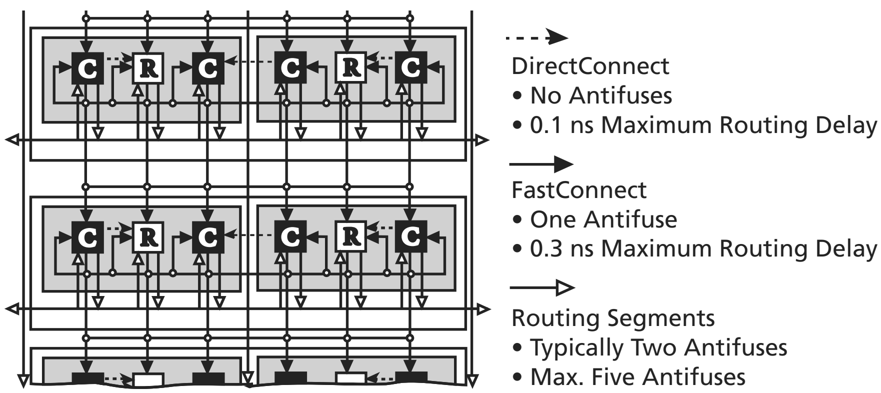



*Figure 1-6* • **DirectConnect and FastConnect for Type 2 SuperClusters**

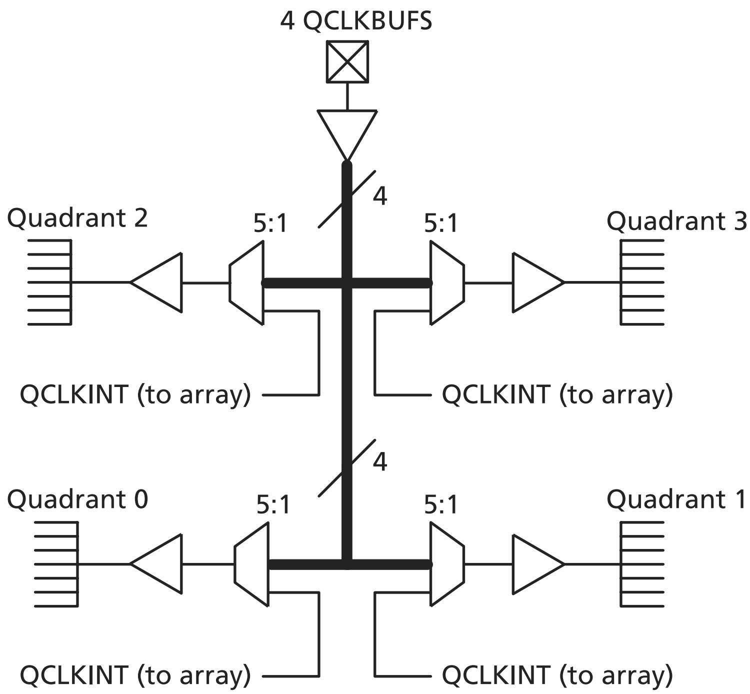



*Figure 1-9* • **SX-A QCLK Architecture**

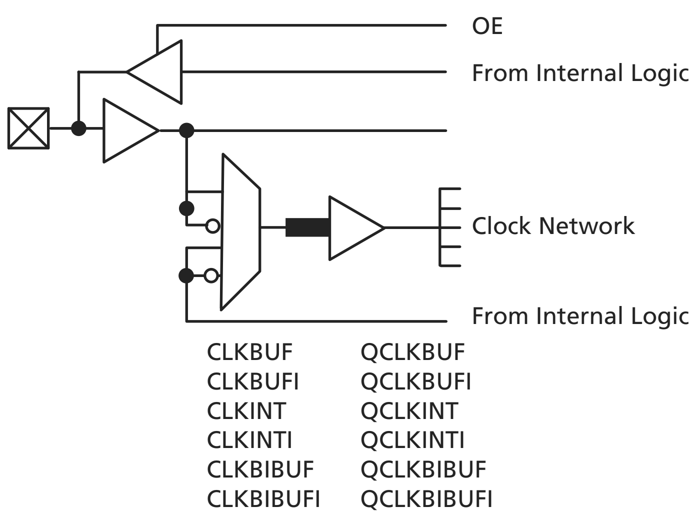



*Figure 1-10* • **A54SX72A Routed Clock and QCLK Buffer**

## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

### Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

*Figure 1-12* • **Device Selection Wizard**

*Table 1-5* • **Reserve Pin Definitions**

| Pin | Function |
|---|---|
| Reserve JTAG | Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS) |
| Reserve JTAG Test Reset | Regular I/O or JTAG reset with an internal pull-up |
| Reserve Probe | Keeps pins from being used or regular I/O |

### Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to $V_{CCI}$ should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

*Table 1-6* • **Boundary-Scan Pin Configurations and Functions**

| Mode | Designer "Reserve JTAG" Selection | TAP Controller State |
|---|---|---|
| Dedicated (JTAG) | Checked | Any |
| Flexible (User I/O) | Unchecked | Test-Logic-Reset |
| Flexible (JTAG) | Unchecked | Any EXCEPT Test-Logic-Reset |

### TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

# Pin Description

**CLKA/B, I/O** **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

**QCLKA/B/C/D, I/O** **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

**GND** **Ground**

Low supply voltage.

**HCLK** **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

**I/O** **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

**NC** **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

**PRA/B, I/O** **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK, I/O** **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI, I/O** **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO, I/O** **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

**TMS** **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**TRST, I/O** **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

**$V_{CCI}$** **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All $V_{CCI}$ power pins in the device should be connected.

**$V_{CCA}$** **Supply Voltage**

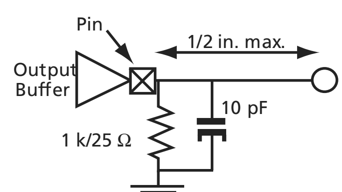
Supply voltage for array. See Table 2-2 on page 2-1. All $V_{CCA}$ power pins in the device should be connected.

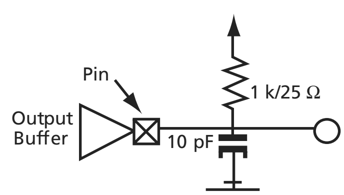
*Table 2-10* • **AC Specifications (3.3 V PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \le 0.3V_{CCI}$ [1] | $-12V_{CCI}$ | – | mA |
| | | $0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1] | $(-17.1(V_{CCI} - V_{OUT}))$ | – | mA |
| | | $0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2] | – | EQ 2-3 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}$ [2] | – | $-32V_{CCI}$ | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1] | $16V_{CCI}$ | – | mA |
| | | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1] | $(26.7V_{OUT})$ | – | mA |
| | | $0.18V_{CCI} > V_{OUT} > 0$ [1, 2] | – | EQ 2-4 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}$ [2] | – | $38V_{CCI}$ | mA |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \le -1$ | $-25 + (V_{IN} + 1)/0.015$ | – | mA |
| $I_{CH}$ | High Clamp Current | $V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$ | $25 + (V_{IN} - V_{CCI} - 1)/0.015$ | – | mA |
| $slew_R$ | Output Rise Slew Rate | $0.2V_{CCI}$ - $0.6V_{CCI}$ load [3] | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate | $0.6V_{CCI}$ - $0.2V_{CCI}$ load [3] | 1 | 4 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*



## Input Buffer Delays

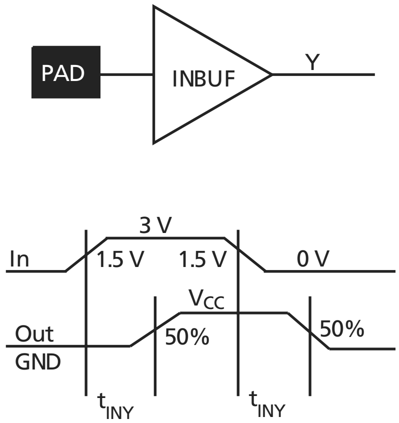



*Figure 2-6* • **Input Buffer Delays**

## C-Cell Delays

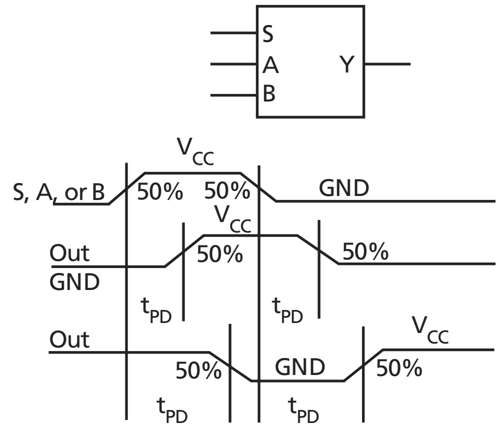



*Figure 2-7* • **C-Cell Delays**

## Cell Timing Characteristics

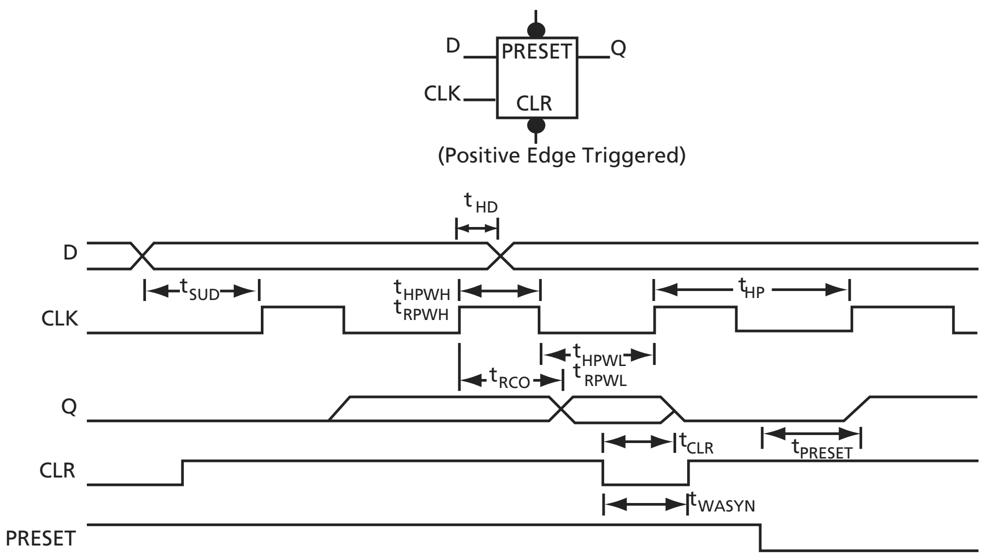



*Figure 2-8* • **Flip-Flops**

*Table 2-14* • **A54SX08A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-15* • **A54SX08A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-20* • **A54SX08A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **5 V PCI Output Module Timing[1]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$[2] | Delta Low to High | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[2] | Delta High to Low | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[3]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$ | Delta High to Low—low slew | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *Delays based on 50 pF loading.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
3. *Delays based on 35 pF loading.*

*Table 2-21* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] Min. | –3 Speed[1] Max. | –2 Speed Min. | –2 Speed Max. | –1 Speed Min. | –1 Speed Max. | Std. Speed Min. | Std. Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.6 | | 1.9 | | 2.7 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-24* • **A54SX16A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ =4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.2 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.7 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-28* • **A54SX32A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$ , $t_{RCO} + t_{RD1} + t_{PDn}$ , or $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance.   Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-34* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] Min. | –3 Speed[1] Max. | –2 Speed Min. | –2 Speed Max. | –1 Speed Min. | –1 Speed Max. | Std. Speed Min. | Std. Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **5 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.1 | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.1 | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 1.9 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.5 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 6.6 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.9 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1 * V_{CCI} – 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

# 144-Pin TQFP

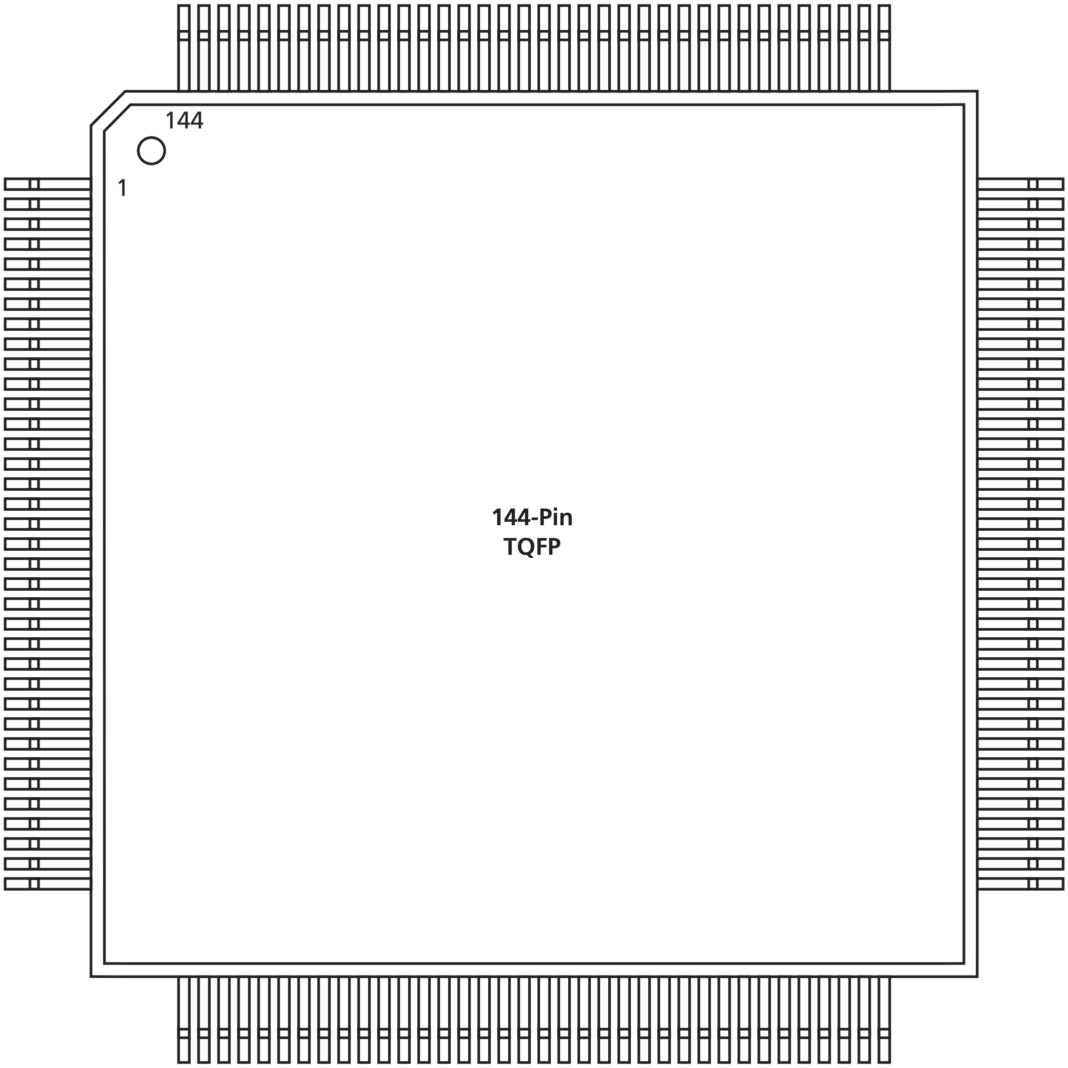



*Figure 3-3* • **144-Pin TQFP (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 484-Pin FBGA

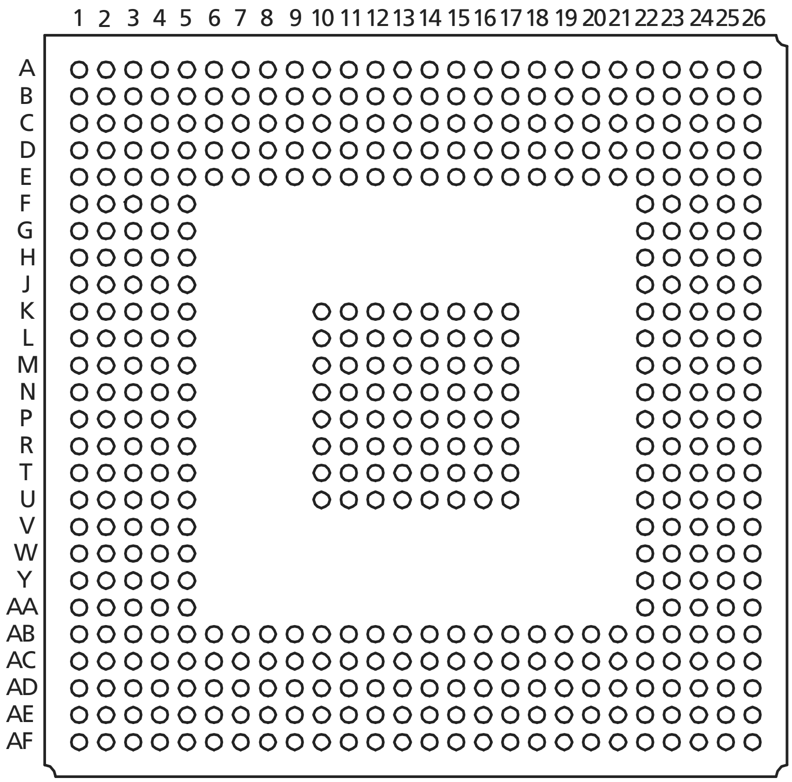



*Figure 3-8* • **484-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| AD18 | I/O | I/O |
| AD19 | I/O | I/O |
| AD20 | I/O | I/O |
| AD21 | I/O | I/O |
| AD22 | I/O | I/O |
| AD23 | $V_{CCI}$ | $V_{CCI}$ |
| AD24 | NC* | I/O |
| AD25 | NC* | I/O |
| AD26 | NC* | I/O |
| AE1 | NC* | NC |
| AE2 | I/O | I/O |
| AE3 | NC* | I/O |
| AE4 | NC* | I/O |
| AE5 | NC* | I/O |
| AE6 | NC* | I/O |
| AE7 | I/O | I/O |
| AE8 | I/O | I/O |
| AE9 | I/O | I/O |
| AE10 | I/O | I/O |
| AE11 | NC* | I/O |
| AE12 | I/O | I/O |
| AE13 | I/O | I/O |
| AE14 | I/O | I/O |
| AE15 | NC* | I/O |
| AE16 | NC* | I/O |
| AE17 | I/O | I/O |
| AE18 | I/O | I/O |
| AE19 | I/O | I/O |
| AE20 | I/O | I/O |
| AE21 | NC* | I/O |
| AE22 | NC* | I/O |
| AE23 | NC* | I/O |
| AE24 | NC* | I/O |
| AE25 | NC* | NC |
| AE26 | NC* | NC |
| AF1 | NC* | NC |
| AF2 | NC* | NC |
| AF3 | NC | I/O |
| AF4 | NC* | I/O |
| AF5 | NC* | I/O |
| AF6 | NC* | I/O |
| AF7 | I/O | I/O |
| AF8 | I/O | I/O |
| AF9 | I/O | I/O |
| AF10 | I/O | I/O |
| AF11 | NC* | I/O |
| AF12 | NC* | NC |
| AF13 | HCLK | HCLK |
| AF14 | I/O | QCLKB |
| AF15 | NC* | I/O |
| AF16 | NC* | I/O |
| AF17 | I/O | I/O |
| AF18 | I/O | I/O |
| AF19 | I/O | I/O |
| AF20 | NC* | I/O |
| AF21 | NC* | I/O |
| AF22 | NC* | I/O |
| AF23 | NC* | I/O |
| AF24 | NC* | I/O |
| AF25 | NC* | NC |
| AF26 | NC* | NC |
| B1 | NC* | NC |
| B2 | NC* | NC |
| B3 | NC* | I/O |
| B4 | NC* | I/O |
| B5 | NC* | I/O |
| B6 | I/O | I/O |
| B7 | I/O | I/O |
| B8 | I/O | I/O |
| B9 | I/O | I/O |
| B10 | I/O | I/O |
| B11 | NC* | I/O |
| B12 | NC* | I/O |
| B13 | $V_{CCI}$ | $V_{CCI}$ |
| B14 | CLKA | CLKA |
| B15 | NC* | I/O |
| B16 | NC* | I/O |
| B17 | I/O | I/O |
| B18 | $V_{CCI}$ | $V_{CCI}$ |
| B19 | I/O | I/O |
| B20 | I/O | I/O |
| B21 | NC* | I/O |
| B22 | NC* | I/O |
| B23 | NC* | I/O |
| B24 | NC* | I/O |
| B25 | I/O | I/O |
| B26 | NC* | NC |
| C1 | NC* | I/O |
| C2 | NC* | I/O |
| C3 | NC* | I/O |
| C4 | NC* | I/O |
| C5 | I/O | I/O |
| C6 | $V_{CCI}$ | $V_{CCI}$ |
| C7 | I/O | I/O |
| C8 | I/O | I/O |
| C9 | $V_{CCI}$ | $V_{CCI}$ |
| C10 | I/O | I/O |
| C11 | I/O | I/O |
| C12 | I/O | I/O |
| C13 | PRA, I/O | PRA, I/O |
| C14 | I/O | I/O |
| C15 | I/O | QCLKD |
| C16 | I/O | I/O |
| C17 | I/O | I/O |
| C18 | I/O | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| T3 | I/O | I/O |
| T4 | I/O | I/O |
| T5 | I/O | I/O |
| T10 | GND | GND |
| T11 | GND | GND |
| T12 | GND | GND |
| T13 | GND | GND |
| T14 | GND | GND |
| T15 | GND | GND |
| T16 | GND | GND |
| T17 | GND | GND |
| T22 | I/O | I/O |
| T23 | I/O | I/O |
| T24 | I/O | I/O |
| T25 | NC* | I/O |
| T26 | NC* | I/O |
| U1 | I/O | I/O |
| U2 | $V_{CCI}$ | $V_{CCI}$ |
| U3 | I/O | I/O |
| U4 | I/O | I/O |
| U5 | I/O | I/O |
| U10 | GND | GND |
| U11 | GND | GND |
| U12 | GND | GND |
| U13 | GND | GND |
| U14 | GND | GND |
| U15 | GND | GND |
| U16 | GND | GND |
| U17 | GND | GND |
| U22 | I/O | I/O |
| U23 | I/O | I/O |
| U24 | I/O | I/O |
| U25 | $V_{CCI}$ | $V_{CCI}$ |
| U26 | I/O | I/O |
| V1 | NC* | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| Pin Number | A54SX32A Function | A54SX72A Function |
| V2 | NC* | I/O |
| V3 | I/O | I/O |
| V4 | I/O | I/O |
| V5 | I/O | I/O |
| V22 | $V_{CCA}$ | $V_{CCA}$ |
| V23 | I/O | I/O |
| V24 | I/O | I/O |
| V25 | NC* | I/O |
| V26 | NC* | I/O |
| W1 | I/O | I/O |
| W2 | I/O | I/O |
| W3 | I/O | I/O |
| W4 | I/O | I/O |
| W5 | I/O | I/O |
| W22 | I/O | I/O |
| W23 | $V_{CCA}$ | $V_{CCA}$ |
| W24 | I/O | I/O |
| W25 | NC* | I/O |
| W26 | NC* | I/O |
| Y1 | NC* | I/O |
| Y2 | NC* | I/O |
| Y3 | I/O | I/O |
| Y4 | I/O | I/O |
| Y5 | NC* | I/O |
| Y22 | I/O | I/O |
| Y23 | I/O | I/O |
| Y24 | $V_{CCI}$ | $V_{CCI}$ |
| Y25 | I/O | I/O |
| Y26 | I/O | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v5.2 (June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1 February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| | Table 2-11 was updated. | 2-9 |