



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-tqg144a

General Description

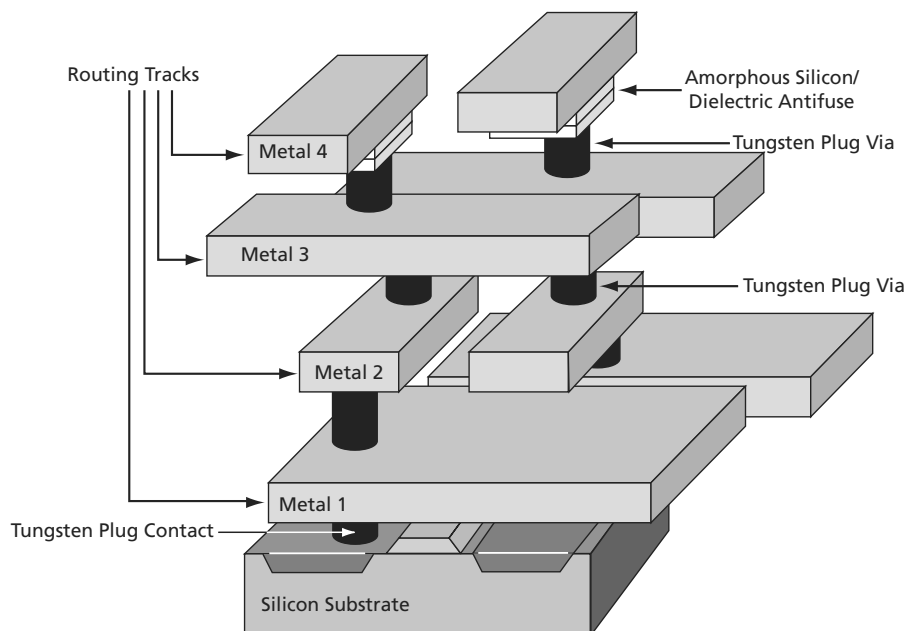
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • I/O Features

Function	Description
Input Buffer Threshold Selections	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) - I/O on an unpowered device does not sink current - Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μ s	0.025 V/ μ s	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μ s	μ s	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 • JTAG Instruction Code

Instructions (IR4:IR0)	Binary Code
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HighZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-8 • JTAG Instruction Code

Device	Process	Revision	Bits 31-28	Bits 27-12
A54SX08A	0.22 μ	0	8, 9	40B4, 42B4
		1	A, B	40B4, 42B4
A54SX16A	0.22 μ	0	9	40B8, 42B8
		1	B	40B8, 42B8
	0.25 μ	1	B	22B8
A54SX32A	0.2 2 μ	0	9	40BD, 42BD
		1	B	40BD, 42BD
	0.25 μ	1	B	22BD
A54SX72A	0.22 μ	0	9	40B2, 42B2
		1	B	40B2, 42B2
	0.25 μ	1	B	22B2

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

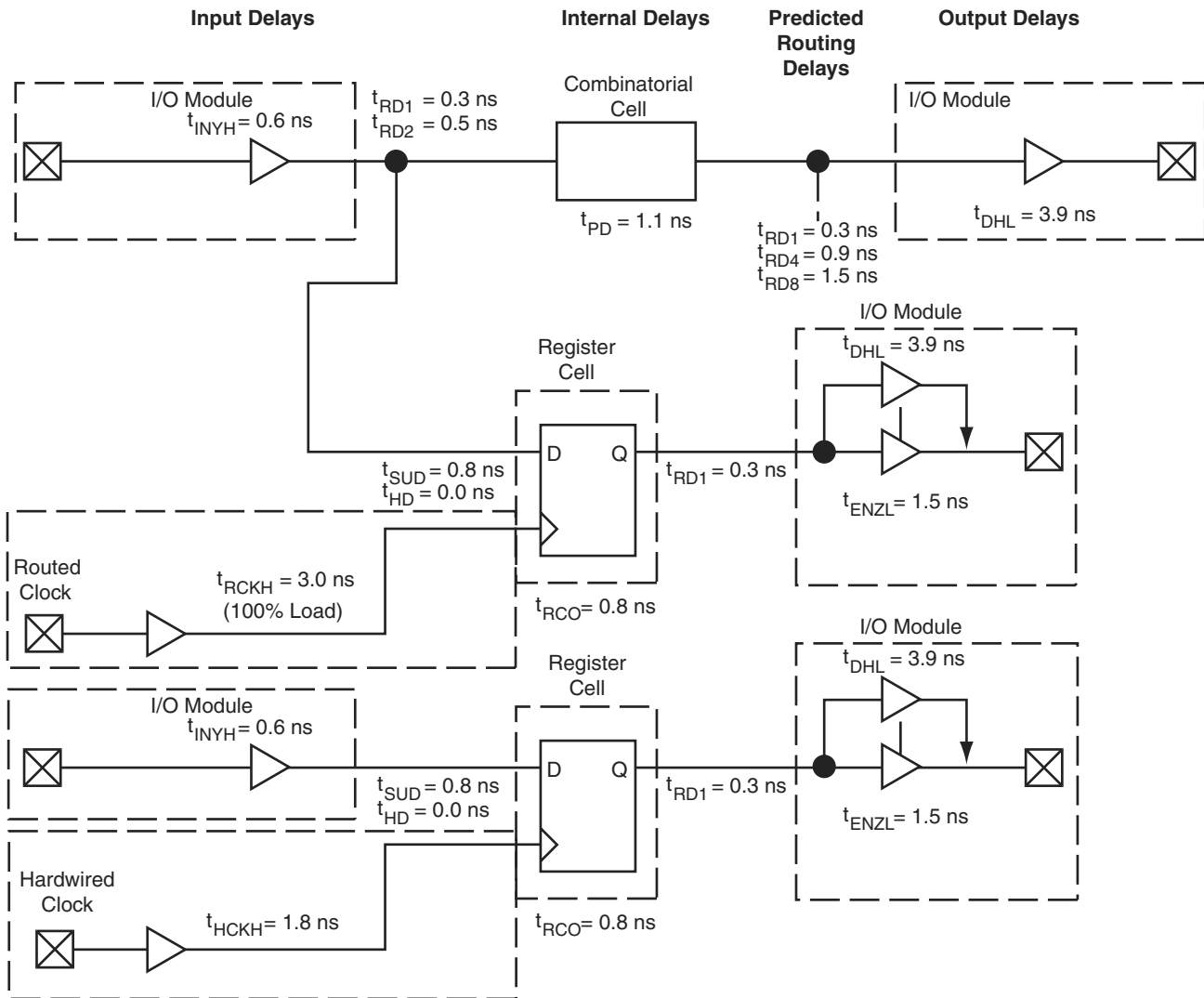
Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

SX-A Timing Model



Note: *Values shown for A54SX72A, -2, worst-case commercial conditions at 5 V PCI with standard place-and-route.

Figure 2-3 • SX-A Timing Model

Sample Path Calculations

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH} \\ &= 0.6 + 0.3 + 0.8 - 1.8 = -0.1 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 \text{ ns} \end{aligned}$$

Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH} \\ &= 0.6 + 0.3 + 0.8 - 3.0 = -1.3 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 \text{ ns} \end{aligned}$$

Output Buffer Delays

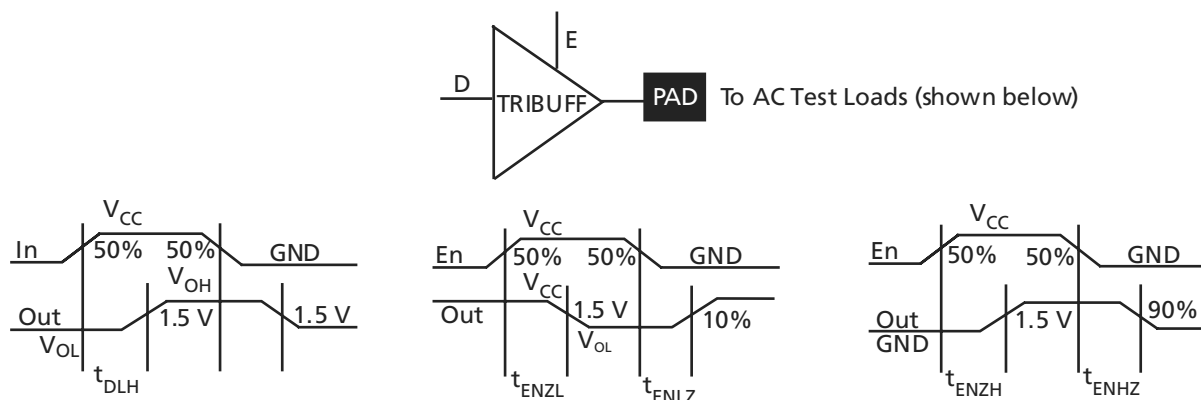


Figure 2-4 • Output Buffer Delays

AC Test Loads

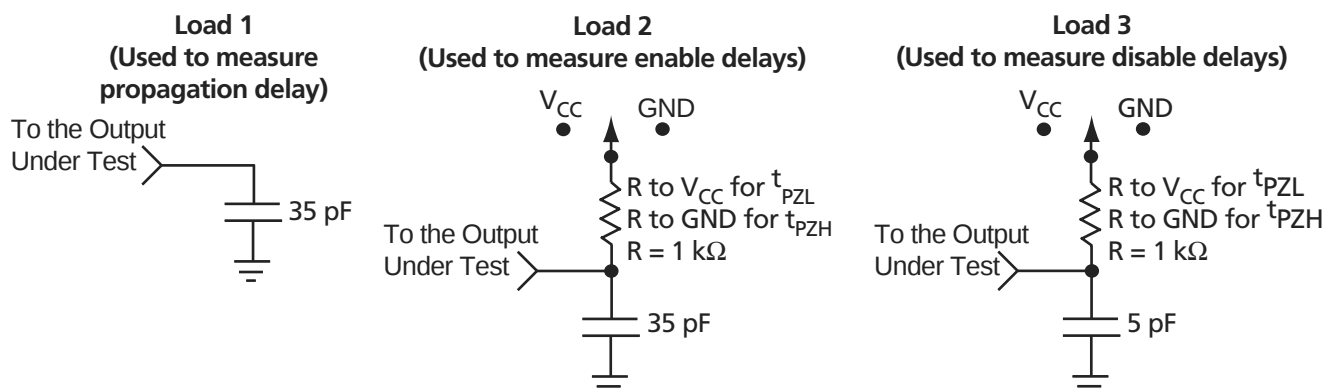


Figure 2-5 • AC Test Loads

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{1,2}										
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-19 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.2		2.4		2.9		4.0		ns
t _{DHL}	Data-to-Pad High to Low	2.3		2.6		3.1		4.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.4		2.9		4.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.3		2.6		3.1		4.3		ns
d _{TLH} ²	Delta Low to High	0.03		0.03		0.04		0.045		ns/pF
d _{THL} ²	Delta High to Low	0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	3.0		3.4		4.0		5.6		ns
t _{DHL}	Data-to-Pad High to Low	3.0		3.3		3.9		5.5		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.4		11.8		13.8		19.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3		3.4		4		5.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3		3.3		3.9		5.5		ns
d _{TLH} ²	Delta Low to High	0.03		0.03		0.04		0.045		ns/pF
d _{THL} ²	Delta High to Low	0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ²	Delta High to Low—low slew	0.053		0.067		0.073		0.107		ns/pF

Notes:

- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-22 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-23 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)	1.2		1.4		1.6		1.8		2.8		ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)	1.0		1.1		1.3		1.5		2.2		ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew	0.3		0.3		0.4		0.4		0.6		ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency	357		294		263		227		167		MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)	1.0		1.2		1.3		1.5		2.1		ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)	1.1		1.3		1.4		1.7		2.3		ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.7		ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.8		ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (50% Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (100% Load)	1.0		1.1		1.3		1.5		2.1		ns

Note: *All –3 speed grades have been discontinued.

Table 2-24 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-36 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V _{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V _{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V _{CCI}	V _{CCI}	V _{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V _{CCI}	V _{CCI}	V _{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V _{CCA}	V _{CCA}	V _{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V _{CCA}	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}	V _{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V _{CCA}	V _{CCA}	V _{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V _{CCA}	V _{CCA}	V _{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D1	I/O	I/O	I/O
D2	V _{CCI}	V _{CCI}	V _{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V _{CCI}	V _{CCI}	V _{CCI}
E7	V _{CCI}	V _{CCI}	V _{CCI}
E8	V _{CCI}	V _{CCI}	V _{CCI}
E9	V _{CCA}	V _{CCA}	V _{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC *	I/O
T26	NC *	I/O
U1	I/O	I/O
U2	V _{CCI}	V _{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V _{CCI}	V _{CCI}
U26	I/O	I/O
V1	NC *	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
V2	NC *	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V _{CCA}	V _{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC *	I/O
V26	NC *	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V _{CCA}	V _{CCA}
W24	I/O	I/O
W25	NC *	I/O
W26	NC *	I/O
Y1	NC *	I/O
Y2	NC *	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC *	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V _{CCI}	V _{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9