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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	
Total RAM Bits	
Number of I/O	203
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-1fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters



Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications.

Function	Description
Input Buffer Threshold Selections	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	 "Hot-Swap" Capability (3.3 V PCI is not hot swappable) I/O on an unpowered device does not sink current Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V _{CCA} and V _{CCI} can be powered in any order

Table 1-2 • I/O Features

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μs	0.025 V/ μs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μs	μs	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2



Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6	٠	Boundary-Scan Pin Configurations an	d
		Functions	

Mode	Designer "Reserve JTAG" Selection	TAP Controller State	
Dedicated (JTAG)	Checked	Any	
Flexible (User I/O)	Unchecked	Test-Logic-Reset	
Flexible (JTAG)	Unchecked	Any EXCEPT Test- Logic-Reset	

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function			
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)			
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up			
Reserve Probe	Keeps pins from being used or regular I/O			

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.



Figure 1-13 • Probe Setup

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices http://www.actel.com/documents/GlobalClk_AN.pdf Using A54SX72A and RT54SX72S Quadrant Clocks http://www.actel.com/documents/QCLK_AN.pdf Implementation of Security in Actel Antifuse FPGAs http://www.actel.com/documents/Antifuse_Security_AN.pdf Actel eX, SX-A, and RTSX-S I/Os http://www.actel.com/documents/AntifuseIO_AN.pdf Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications http://www.actel.com/documents/HotSwapColdSparing_AN.pdf Programming Antifuse Devices http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs http://www.actel.com/documents/HRSXA_DS.pdf SX-A Automotive Family FPGAs http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V _{CCI}	DC Supply Voltage for I/Os	-0.3 to +6.0	V
V _{CCA}	DC Supply Voltage for Arrays	-0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
V _O	Output Voltage	–0.5 to + V _{CCI} + 0.5	V
T _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
2.5 V Power Supply Range (V _{CCA} and V _{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V _{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V _{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with $V_{CCA} = 2.5 V$

Product	V _{CCI} = 2.5 V	V _{CCI} = 3.3 V	V _{CCI} = 5 V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

V _{CCA}	V _{CCI} *	Maximum Input Tolerance	Maximum Output Drive
2. 5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

Note: *3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

Electrical Specifications

Table 2-5 • 3.3 V LVTTL and 5 V TTL Electrical Specifications

			Comm	ercial	Industrial		
Symbol	Parameter		Min.	Max.	Min.	Max.	Units
V _{OH}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	$(I_{OH} = -1 \text{ mA})$	0.9 V _{CCI}		0.9 V _{CCI}		V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OH} = -8 mA)	2.4		2.4		V
V _{OL}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 1 mA)		0.4		0.4	V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 12 mA)		0.4		0.4	V
V _{IL}	Input Low Voltage			0.8		0.8	V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current		-10	10	-10	10	μΑ
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

			Comn	nercial	Indu	strial	
Symbol	Parameter		Min.	Max.	Min.	Max.	Units
V _{OH}	$V_{DD} = MIN,$	$(I_{OH} = -100 \ \mu A)$	2.1		2.1		V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	$V_{DD} = MIN,$ $V_{I} = V_{UI} \text{ or } V_{U}$	$(I_{OH} = -1 \text{ mA})$	2.0		2.0		V
		(l - 2mA)	17		17		V
	$V_{DD} = V_{IH}$ or V_{IL}	(I _{OH} =2 IIIA)	1.7		1.7		v
V _{OL}	$V_{DD} = MIN,$	(I _{OL} = 100 μA)		0.2		0.2	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	$V_{DD} = MIN,$	(I _{OL} = 1 mA)		0.4		0.4	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$	-					
	$V_{DD} = MIN,$	(I _{OL} = 2 mA)		0.7		0.7	V
	$V_{I} = V_{IH} \text{ or } V_{IL}$						
V _{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
$I_{\rm IL}/I_{\rm IH}$	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		-10	10	-10	10	μΑ
I _{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		-10	10	-10	10	μΑ
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.

Table 2-14 A545X08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCA} = 2.25 V$, $V_{CCI} = 3.0 V$, $T_J = 70^{\circ}$ C)

		-2 Spe	ed	-1 S	peed	Std. S	Speed	-F S	peed	
Parameter	Description	Min. N	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t _{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Modul	e Predicted Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t _{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-17 • A54SX08A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _{CCI} =	= 4.75 V, T _J = 70°C)
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		-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lardwired) Array Clock Networks									
t _{НСКН}	Input Low to High (Pad to R-cell Input)		1.2		1.3		1.5		2.3	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.2		1.4		2.0	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Arra	y Clock Networks									
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.3		1.5		2.1	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.9	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPVVL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		1.0		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-22 A54SX16A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V,	V _{CCI} = 2.25 V,	T _J = 70°C)
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		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Networ	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Arr	ay Clock Networks			-		-				-		
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-29 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _c	_{CCI} = 2.25 V, T _J = 70°C)
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		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Netwo	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Arr	ay Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-37 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions	5 V _{CCA} = 2.25 V, V _{CCI} = 3.0 V, T _J = 70	°C)
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		–3 Speed* –2 Speed		–1 Speed		Std. Speed		–F Speed				
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Netwo	rks										1
t _{нскн}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPVVL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Arra	ay Clock Networks											
t _{rckh}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t _{rckl}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{rckl}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{rckl}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant A	rray Clock Networks											
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t _{qchkl}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: *All –3 speed grades have been discontinued.

	2	08-Pin PQF	Р		208-Pin PQFP							
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function	Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function			
141	NC	I/O	I/O	I/O	176	NC	I/O	I/O	I/O			
142	I/O	I/O	I/O	I/O	177	I/O	I/O	I/O	I/O			
143	NC	I/O	I/O	I/O	178	I/O	I/O	I/O	QCLKD			
144	I/O	I/O	I/O	I/O	179	I/O	I/O	I/O	I/O			
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}	180	CLKA	CLKA	CLKA	CLKA			
146	GND	GND	GND	GND	181	CLKB	CLKB	CLKB	CLKB			
147	I/O	I/O	I/O	I/O	182	NC	NC	NC	NC			
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}	183	GND	GND	GND	GND			
149	I/O	I/O	I/O	I/O	184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}			
150	I/O	I/O	I/O	I/O	185	GND	GND	GND	GND			
151	I/O	I/O	I/O	I/O	186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O			
152	I/O	I/O	I/O	I/O	187	I/O	I/O	I/O	V _{CCI}			
153	I/O	I/O	I/O	I/O	188	I/O	I/O	I/O	I/O			
154	I/O	I/O	I/O	I/O	189	NC	I/O	I/O	I/O			
155	NC	I/O	I/O	I/O	190	I/O	I/O	I/O	QCLKC			
156	NC	I/O	I/O	I/O	191	I/O	I/O	I/O	I/O			
157	GND	GND	GND	GND	192	NC	I/O	I/O	I/O			
158	I/O	I/O	I/O	I/O	193	I/O	I/O	I/O	I/O			
159	I/O	I/O	I/O	I/O	194	I/O	I/O	I/O	I/O			
160	I/O	I/O	I/O	I/O	195	NC	I/O	I/O	I/O			
161	I/O	I/O	I/O	I/O	196	I/O	I/O	I/O	I/O			
162	I/O	I/O	I/O	I/O	197	I/O	I/O	I/O	I/O			
163	I/O	I/O	I/O	I/O	198	NC	I/O	I/O	I/O			
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}	199	I/O	I/O	I/O	I/O			
165	I/O	I/O	I/O	I/O	200	I/O	I/O	I/O	I/O			
166	I/O	I/O	I/O	I/O	201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}			
167	NC	I/O	I/O	I/O	202	NC	I/O	I/O	I/O			
168	I/O	I/O	I/O	I/O	203	NC	I/O	I/O	I/O			
169	I/O	I/O	I/O	I/O	204	I/O	I/O	I/O	I/O			
170	NC	I/O	I/O	I/O	205	NC	I/O	I/O	I/O			
171	I/O	I/O	I/O	I/O	206	I/O	I/O	I/O	I/O			
172	I/O	I/O	I/O	I/O	207	I/O	I/O	I/O	I/O			
173	NC	I/O	I/O	I/O	208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O			
174	I/O	I/O	I/O	I/O		-			-			
175	I/O	I/O	I/O	I/O								



176-Pin TQFP							
Pin Number	A54SX32A Function						
145	I/O						
146	I/O						
147	I/O						
148	I/O						
149	I/O						
150	I/O						
151	I/O						
152	CLKA						
153	CLKB						
154	NC						
155	GND						
156	V _{CCA}						
157	PRA, I/O						
158	I/O						
159	I/O						
160	I/O						
161	I/O						
162	I/O						
163	I/O						
164	I/O						
165	I/O						
166	I/O						
167	I/O						
168	I/O						
169	V _{CCI}						
170	I/O						
171	I/O						
172	I/O						
173	I/O						
174	I/O						
175	I/O						
176	TCK, I/O						

329-Pin PBGA

		12	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Α	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{0}$
В	C	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
С	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D		$\frac{1}{2}$	0	0	0	0	Ο	0	0	Ο	Ο	0	0	Ο	0	0	0	0	Ο	0	0	0	0
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L	C	00	0	0						0	0	0	0	0						0	Ο	Ο	0
M		$\sum_{i=1}^{i}$	0	0						Õ	Õ	Õ	Õ	Õ						Õ	Õ	Õ	0
N P		$\frac{1}{2}$		0								0								0	0	\bigcirc	\mathbf{O}
R		$\frac{1}{2}$	$\overline{0}$	õ						0	0	0	0	0						0	õ	õ	0
т	C	00	Õ	Õ																Õ	Õ	Õ	Õ
U	C	00	0	0																0	0	0	0
V	C	00	0	0																0	0	0	0
W		$\frac{1}{2}$	0	0	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	0	Õ	0	0
Y A A) 0	\mathbf{O}	0	0	0	0	0	0	0	0	0 O	O	O	0	0	0	0	0	0	0	0	0
AB		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $								0	0		0									0
AC	$\left(\right)$	$\frac{1}{2}$	$\overline{0}$	0	0	0	õ	õ	0	0	õ	õ	õ	õ	0	0	0	0	0	0	õ	õ	õ
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Figure 3-5 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA



Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

	Actel
SX-A Fa	amily FPGAs

484-Pin FBGA								
Pin Number	A54SX32A Function	A54SX72A Function						
T3	I/O	I/O						
T4	I/O	I/O						
T5	I/O	I/O						
T10	GND	GND						
T11	GND	GND						
T12	GND	GND						
T13	GND	GND						
T14	GND	GND						
T15	GND	GND						
T16	GND	GND						
T17	GND	GND						
T22	I/O	I/O						
T23	I/O	I/O						
T24	I/O	I/O						
T25	NC*	I/O						
T26	NC*	I/O						
U1	I/O	I/O						
U2	V _{CCI}	V _{CCI}						
U3	I/O	I/O						
U4	I/O	I/O						
U5	I/O	I/O						
U10	GND	GND						
U11	GND	GND						
U12	GND	GND						
U13	GND	GND						
U14	GND	GND						
U15	GND	GND						
U16	GND	GND						
U17	GND	GND						
U22	I/O	I/O						
U23	I/O	I/O						
U24	I/O	I/O						
U25	V _{CCI}	V _{CCI}						
U26	I/O	I/O						
V1	NC*	I/O						

484-Pin FBGA										
Pin Number	A54SX32A Function	A54SX72A Function								
V2	NC*	I/O								
V3	I/O	I/O								
V4	I/O	I/O								
V5	I/O	I/O								
V22	V _{CCA}	V _{CCA}								
V23	I/O	I/O								
V24	I/O	I/O								
V25	NC*	I/O								
V26	NC*	I/O								
W1	I/O	I/O								
W2	I/O	I/O								
W3	I/O	I/O								
W4	I/O	I/O								
W5	I/O	I/O								
W22	I/O	I/O								
W23	V _{CCA}	V _{CCA}								
W24	I/O	I/O								
W25	NC*	I/O								
W26	NC*	I/O								
Y1	NC*	I/O								
Y2	NC*	I/O								
Y3	I/O	I/O								
Y4	I/O	I/O								
Y5	NC*	I/O								
Y22	I/O	I/O								
Y23	I/O	I/O								
Y24	V _{CCI}	V _{CCI}								
Y25	I/O	I/O								
Y26	I/O	1/0								

Note: *These pins must be left floating on the A54SX32A device.

Previous Version	Changes in Current Version (v5.3)	Page					
v4.0	Table 2-12 was updated.						
(continued)	The was updated.						
	The "Sample Path Calculations" were updated.	2-14					
	Table 2-13 was updated.						
	Table 2-13 was updated.	2-17					
	All timing tables were updated.	2-18 to 2-52					
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.						
	The "Ordering Information" section was updated.	1-ii					
	The "Temperature Grade Offering" section was updated.	1-iii					
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1					
	The ""Clock Resources" section" was updated	1-5					
	The Table 1-1 • SX-A Clock Resources is new.	1-5					
	The "User Security" section is new.	1-7					
	The "I/O Modules" section was updated.						
	The Table 1-2 • I/O Features was updated.						
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8					
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new	1-8					
	The Figure 1-12 • Device Selection Wizard is new.	1-9					
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9					
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11					
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12					
	The "Design Considerations" section was updated.	1-12					
	The Figure 1-13 • Probe Setup was updated.	1-12					
	The Design Environment was updated.	1-13					
	The Figure 1-13 • Design Flow is new.	1-11					
	The "Absolute Maximum Ratings*" section was updated.	1-12					
	The "Recommended Operating Conditions" section was updated.	1-12					
	The "Electrical Specifications" section was updated.	1-12					
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.						
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.						
	The "Pin Description" section was updated.	1-15					
v2.0.1	The "Design Environment" section has been updated.	1-13					
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8					
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23					



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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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