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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	360
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (27X27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-1fgg484m

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • I/O Features

Function	Description
Input Buffer Threshold Selections	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	5 V: PCI, TTL 3.3 V: PCI, LVTTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) - I/O on an unpowered device does not sink current - Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μ s	0.025 V/ μ s	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μ s	μ s	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage for I/Os	−0.3 to +6.0	V
V_{CCA}	DC Supply Voltage for Arrays	−0.3 to +3.0	V
V_I	Input Voltage	−0.5 to +5.75	V
V_O	Output Voltage	−0.5 to + V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	−40 to +85	°C
2.5 V Power Supply Range (V_{CCA} and V_{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V_{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V_{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with $V_{CCA} = 2.5$ V

Product	$V_{CCI} = 2.5$ V	$V_{CCI} = 3.3$ V	$V_{CCI} = 5$ V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

V_{CCA}	V_{CCI}^*	Maximum Input Tolerance	Maximum Output Drive
2.5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

Note: *3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	5.75	V
V _{IL}	Input Low Voltage		–0.5	0.8	V
I _{IH}	Input High Leakage Current ¹	V _{IN} = 2.7	–	70	μA
I _{IL}	Input Low Leakage Current ¹	V _{IN} = 0.5	–	–70	μA
V _{OH}	Output High Voltage	I _{OUT} = –2 mA	2.4	–	V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA	–	0.55	V
C _{IN}	Input Pin Capacitance ³		–	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 2-8 • AC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ ¹	–44	–	mA
		$1.4 \leq V_{OUT} < 2.4$ ^{1, 2}	$(-44 + (V_{OUT} - 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ ^{1, 3}	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ ³	–	–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ ¹	95	–	mA
		$2.2 > V_{OUT} > 0.55$ ¹	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ ^{1, 3}	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ ³	–	206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Notes:

1. Refer to the *VII* curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

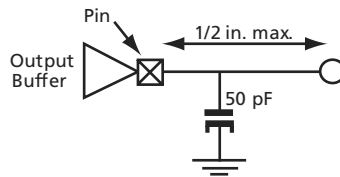


Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

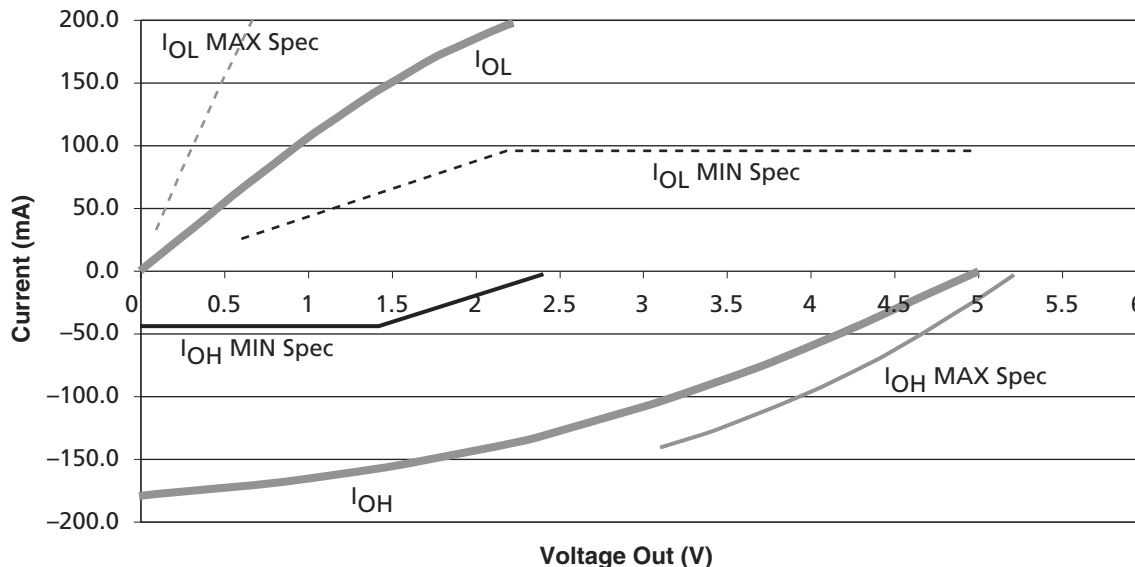


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CCI}$	–	V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CCI}$	-10	+10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$	–	V
V_{OL}	Output Low Voltage	$I_{OUT} = 1,500 \mu A$		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance ³		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 2-20 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH} ²	Delta Low to High	0.016		0.02		0.022		0.032		ns/pF
d _{THL} ²	Delta High to Low	0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.6		8.6		10.1		14.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH}	Delta Low to High	0.017		0.017		0.023		0.031		ns/pF
d _{THL}	Delta High to Low	0.029		0.031		0.037		0.051		ns/pF
d _{THLS}	Delta High to Low—low slew	0.046		0.057		0.066		0.089		ns/pF

Notes:

- Delays based on 50 pF loading.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-22 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-31 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-36 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Table 2-37 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-40 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.3		2.7		3.0		3.6		5.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.0		3.6		5.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	3.2		3.7		4.2		5.0		6.9		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.7		4.2		4.9		6.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3		11.9		13.5		15.8		22.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2		3.7		4.2		5.0		6.9		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.7		4.2		4.9		6.9		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HLH|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Package Pin Assignments

208-Pin PQFP

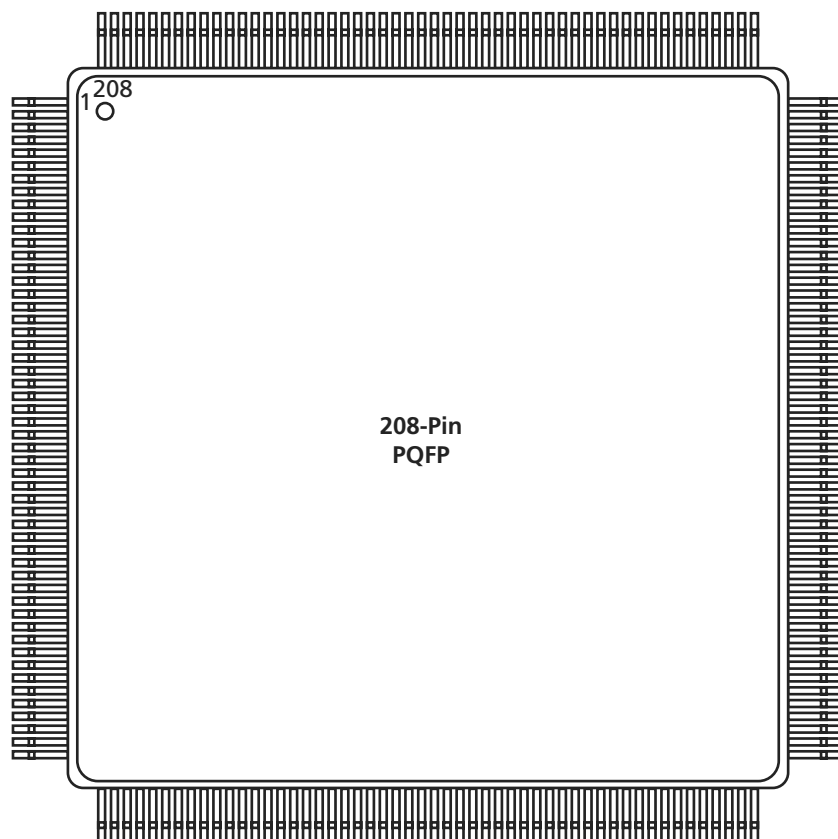


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V _{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V _{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O

176-Pin TQFP

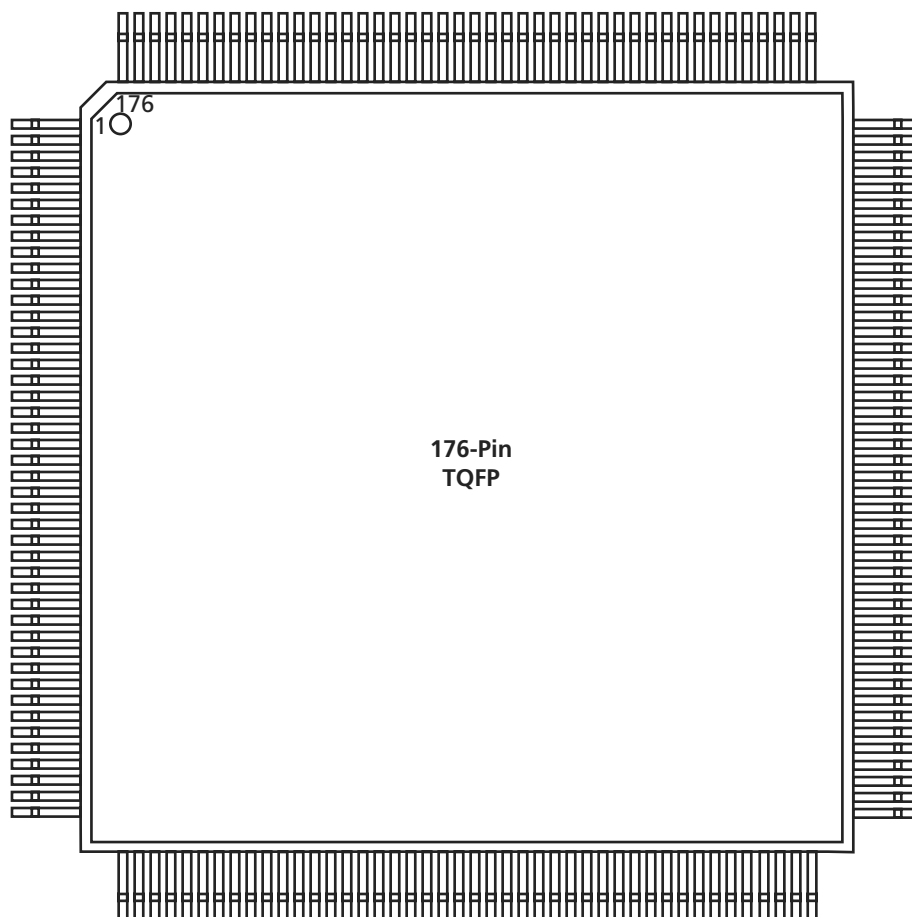


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA	
Pin Number	A545X32A Function
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V _{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

144-Pin FBGA

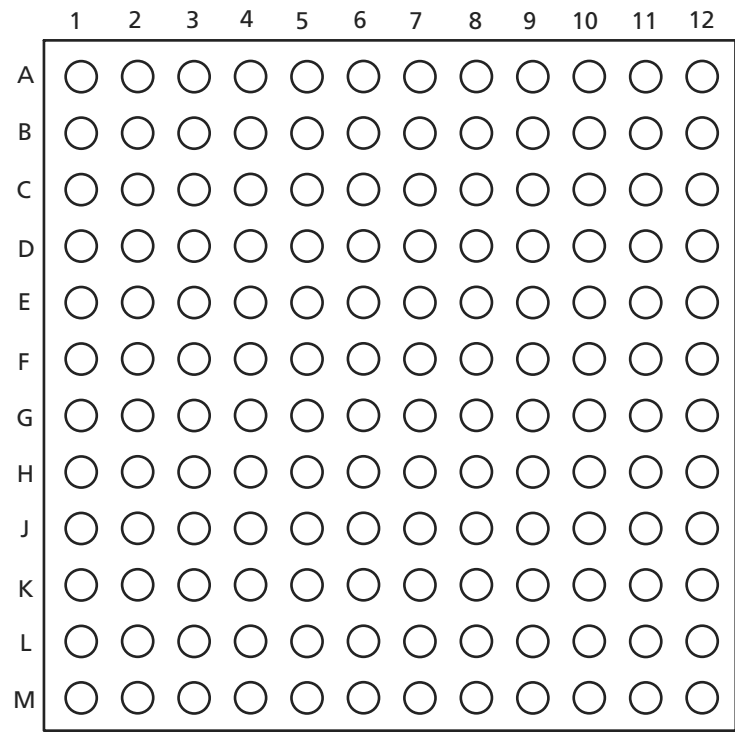


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V _{CCA}	V _{CCA}	V _{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC
A2	NC*	NC
A3	NC*	I/O
A4	NC*	I/O
A5	NC*	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC*	I/O
A12	NC*	I/O
A13	I/O	I/O
A14	NC*	NC
A15	NC*	I/O
A16	NC*	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC*	I/O
A22	NC*	I/O
A23	NC*	I/O
A24	NC*	I/O
A25	NC*	NC
A26	NC*	NC
AA1	NC*	I/O
AA2	NC*	I/O
AA3	V _{CCA}	V _{CCA}
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AA26	NC*	I/O
AB1	NC*	NC
AB2	V _{CCI}	V _{CCI}
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC*	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V _{CCA}	V _{CCA}
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC*	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC*	I/O
AB26	NC*	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC*	I/O
AC5	V _{CCI}	V _{CCI}
AC6	I/O	I/O
AC7	V _{CCI}	V _{CCI}
AC8	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V _{CCI}	V _{CCI}
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC*	I/O
AC24	I/O	I/O
AC25	NC*	I/O
AC26	NC*	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V _{CCI}	V _{CCI}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V _{CCI}	V _{CCI}
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V _{CCI}	V _{CCI}

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V _{CCI}	V _{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V _{CCI}	V _{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V _{CCI}	V _{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V _{CCA}	V _{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V _{CCI}	V _{CCI}
E26	GND	GND
F1	V _{CCI}	V _{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V _{CCA}	V _{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V _{CCI}	V _{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V _{CCI}	V _{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V _{CCA}	V _{CCA}

Note: *These pins must be left floating on the A54SX32A device.

Previous Version	Changes in Current Version (v5.3)	Page
v4.0 (continued)	Table 2-12 was updated.	2-11
	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The "Clock Resources" section was updated.	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new.	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23