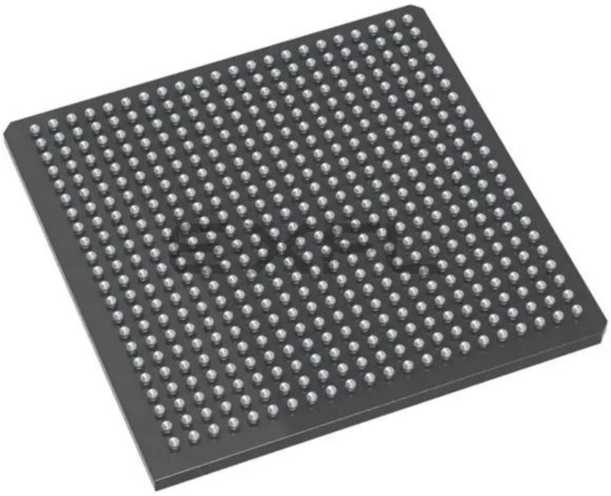
Microchip Technology - A54SX72A-2FG484I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	360
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (27X27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-2fg484i

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

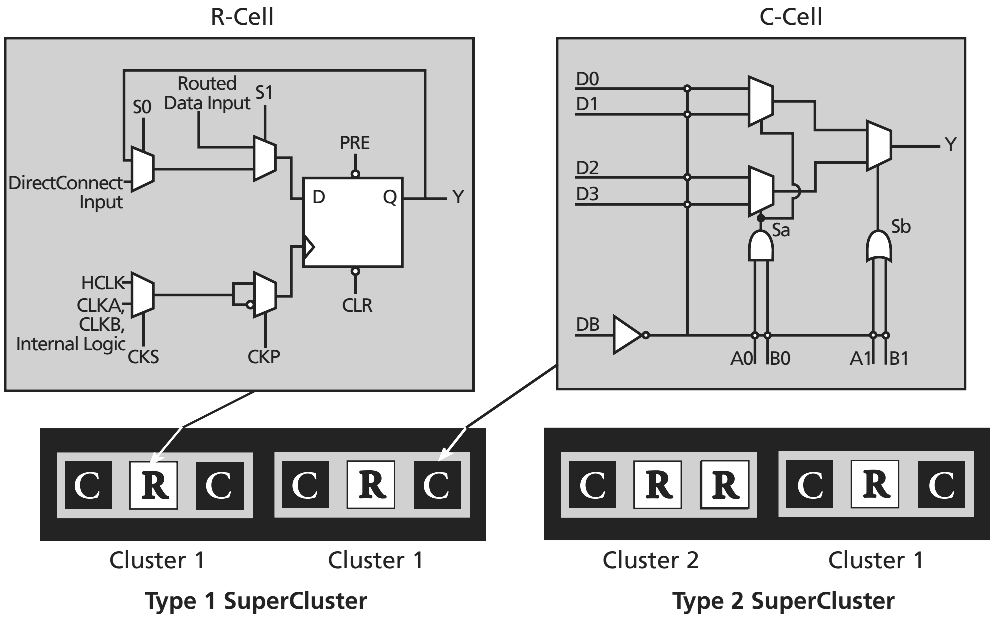


Figure 1-4 • **Cluster Organization**

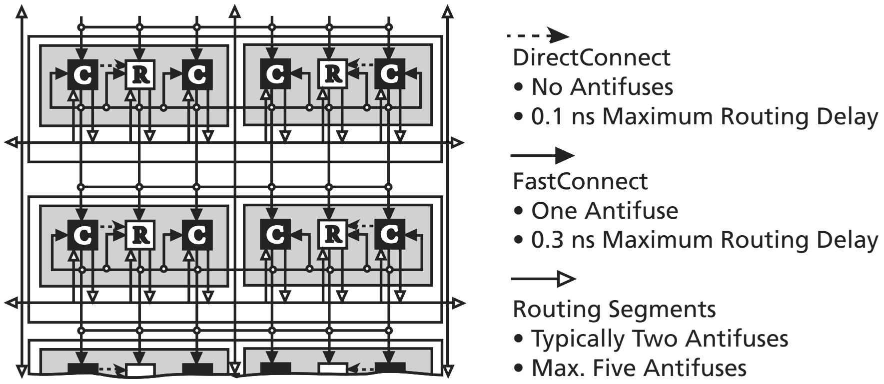


Figure 1-5 • **DirectConnect and FastConnect for Type 1 SuperClusters**

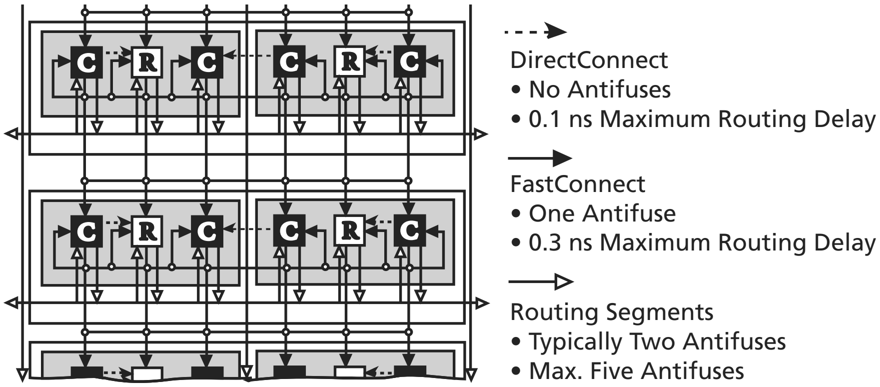


Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

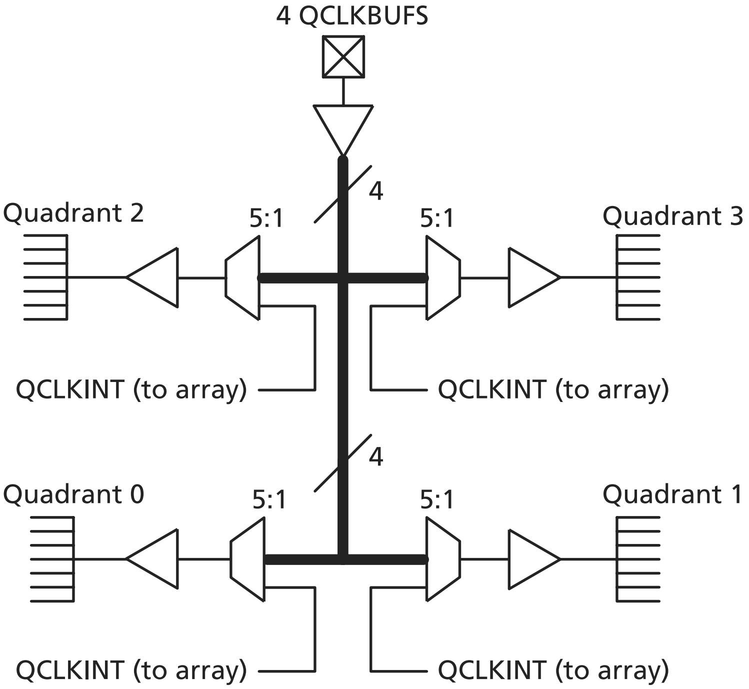


Figure 1-9 • **SX-A QCLK Architecture**

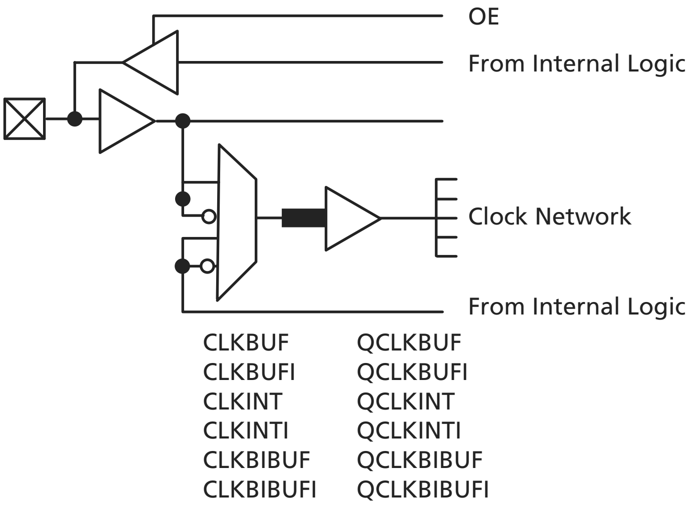


Figure 1-10 • **A54SX72A Routed Clock and QCLK Buffer**

Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 μ / 0.25 μ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).

Figure 1-11 • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the “logic reset” state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

Electrical Specifications

Table 2-5 • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	0.9 V_{CCI}		0.9 V_{CCI}		V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –8 mA)	2.4		2.4		V
V_{OL}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12 mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Table 2-6 • **2.5 V LVCMOS2 Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –100 µA)	2.1		2.1		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	2.0		2.0		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} =–-2 mA)	1.7		1.7		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 100 µA)		0.2		0.2	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \leq V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \geq V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Where:

C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of CLKA/B in pF
C_{EQHV} = Variable capacitance of HCLK in pF
C_{EQHF} = Fixed capacitance of HCLK in pF
$C_{L =}$ Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average CLKA rate in MHz
f_{q2} = Average CLKB rate in MHz
f_{s1} = Average HCLK rate in MHz
m = Number of logic modules switching at fm
n = Number of input buffers switching at fn
p = Number of output buffers switching at fp
q_1 = Number of clock loads on CLKA
q_2 = Number of clock loads on CLKB
r_1 = Fixed capacitance due to CLKA
r_2 = Fixed capacitance due to CLKB
$s_{1 =}$ Number of clock loads on HCLK
x = Number of I/Os at logic low
y = Number of I/Os at logic high

Table 2-11 • **CEQ Values for SX-A Devices**

	A54SX08A	**A54SX16A**	**A54SX32A**	**A54SX72A**
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Table 2-15 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

		–2 Speed		**–1 Speed**		**Std. Speed**		**–F Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-17 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	**Description**	**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		**Units**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.3		1.5		2.3	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.2		1.4		2.0	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.3		1.5		2.1	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.9	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		1.0		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-19 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[1]										
t_{DLH}	Data-to-Pad Low to High		2.2		2.4		2.9		4.0	ns
t_{DHL}	Data-to-Pad High to Low		2.3		2.6		3.1		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.4		2.9		4.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.3		2.6		3.1		4.3	ns
d_{TLH}[2]	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[2]	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad Low to High		3.0		3.4		4.0		5.6	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		10.4		11.8		13.8		19.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3		3.4		4		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3		3.3		3.9		5.5	ns
d_{TLH}[2]	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[2]	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[2]	Delta High to Low—low slew		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25 Ω resistance.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} - 0.9*V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} *is the load capacitance driven by the I/O in pF*
   $d_{T[LH|HL|HLS]}$ *is the worst case delta value from the datasheet in ns/pF.*
3. *Delays based on 35 pF loading.*

Table 2-21 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[2]												
t_{PD}	Internal Array Module		0.9		1.0		1.2		1.4		1.9	ns
Predicted Routing Delays[3]												
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t_{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.6		1.9		2.7		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Minimum Pulse Width	1.4		1.7		1.9		2.2		3.0		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		0.9		1.0		1.1		1.6	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		0.9		1.1		1.2		1.4		2.0	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-24 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-25 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing [2, 3]												
t_{DLH}	Data-to-Pad Low to High		3.4		3.9		4.5		5.2		7.3	ns
t_{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		11.6		13.4		15.2		17.9		25.0	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		3.9		4.5		5.2		7.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}[4]	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[4]	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[4]	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-28 • **A54SX32A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		–3 Speed[1]		**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.9		1.1		1.2		1.4		1.9	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-30 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-33 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	**Description**	**–3 Speed[1]**		**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		**Units**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.4		2.9		4.0	ns
t_{DHL}	Data-to-Pad High to Low		2.0		2.3		2.6		3.1		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.4		2.9		4.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.0		2.3		2.6		3.1		4.3	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.6		3.0		3.4		4.0		5.6	ns
t_{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		9.0		10.4		11.8		13.8		19.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.6		3.0		3.4		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-36 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

		–3 Speed*		**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		2.9		3.4		4.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.7		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.3		3.8		4.5		6.2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.0		4.7		6.6	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.8		2.1		2.4		2.8		3.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.8		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.6		3.0		3.3		3.9		5.5	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.2		5.9	ns

Note: **All –3 speed grades have been discontinued.*

Package Pin Assignments

208-Pin PQFP

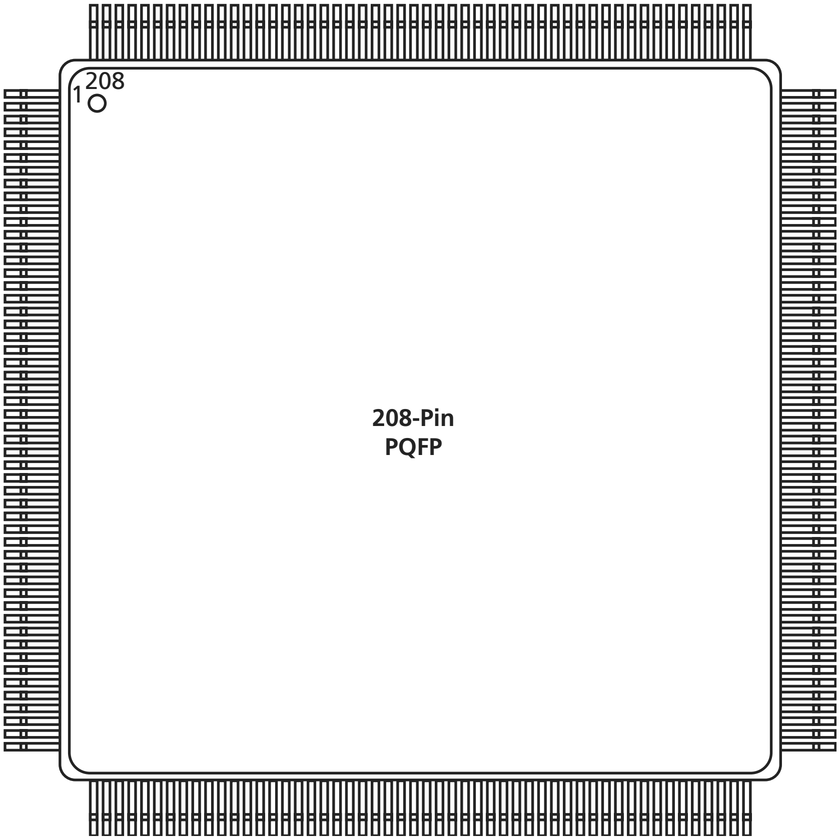


Figure 3-1 • **208-Pin PQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

329-Pin PBGA

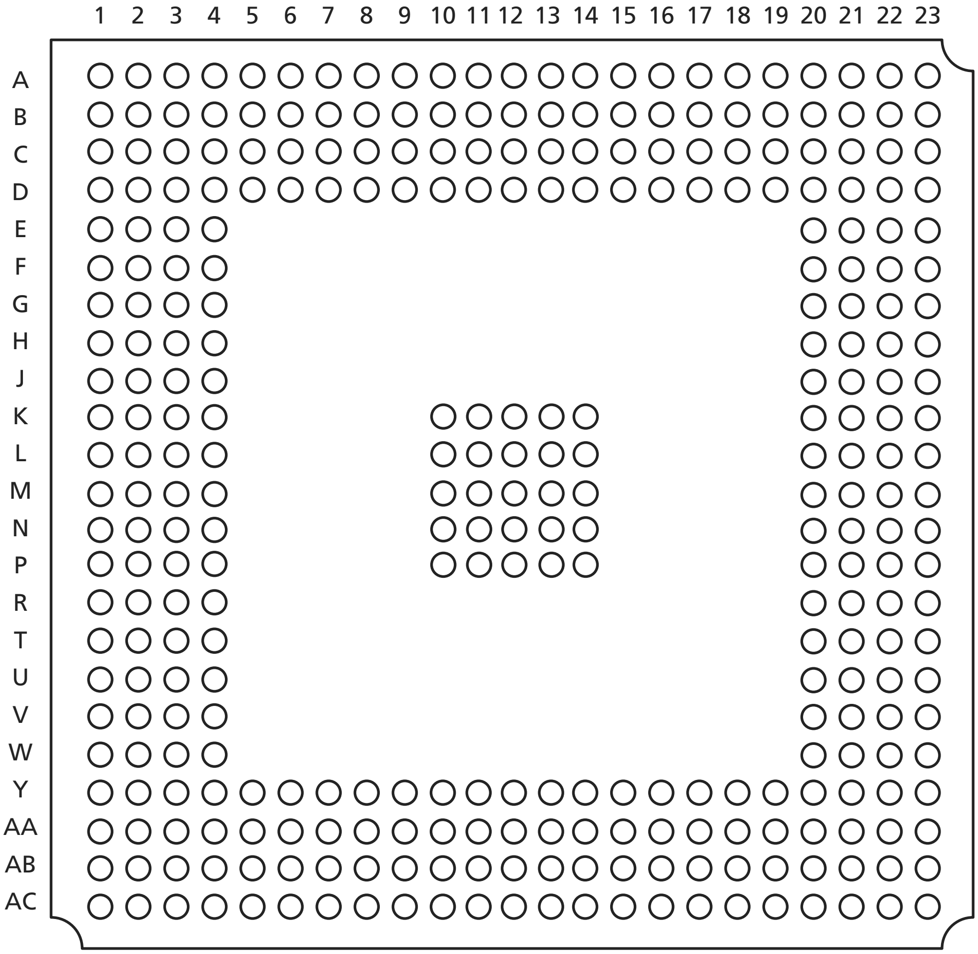


Figure 3-5 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.