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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	360
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (27X27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-2fgg484

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Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High. When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

JTAG Mode	TRST ¹	Security Fuse Programmed	PRA, PRB ²	TDI, TCK, TDO ²
Dedicated	cated Low No		User I/O ³	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O ³	User I/O ³
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.

2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.



Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero[®] Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is design management environment. seamlessly а integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Svnplify[®] for Actel from Synplicity[®], ViewDraw[®] for Actel from Mentor Graphics[®], ModelSim[®] HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD[™], and Designer software from Actel. Refer to the Libero IDE flow diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

- 1. Load the .AFM file
- 2. Select the device to be programmed
- 3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

Electrical Specifications

Table 2-5 • 3.3 V LVTTL and 5 V TTL Electrical Specifications

			Comm	ercial	Indus		
Symbol	Parameter		Min.	Max.	Min.	Max.	Units
V _{OH}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	$(I_{OH} = -1 \text{ mA})$	0.9 V _{CCI}		0.9 V _{CCI}		V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OH} = -8 mA)	2.4		2.4		V
V _{OL}	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 1 mA)		0.4		0.4	V
	$V_{CCI} = Minimum$ $V_I = V_{IH} \text{ or } V_{IL}$	(I _{OL} = 12 mA)		0.4		0.4	V
V _{IL}	Input Low Voltage			0.8		0.8	V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current		-10	10	-10	10	μΑ
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

				Commercial		Industrial		
Symbol	Parameter		Min.	Max.	Min.	Max.	Units	
V _{OH}	$V_{DD} = MIN,$	$(I_{OH} = -100 \ \mu A)$	2.1		2.1		V	
	$V_{I} = V_{IH} \text{ or } V_{IL}$							
	$V_{DD} = MIN,$ $V_{I} = V_{UI} \text{ or } V_{U}$	$(I_{OH} = -1 \text{ mA})$	2.0		2.0		V	
		(l - 2mA)	17		17		V	
	$V_{DD} = V_{IH}$ or V_{IL}	(I _{OH} =2 IIIA)	1.7		1.7		v	
V _{OL}	$V_{DD} = MIN,$	(I _{OL} = 100 μA)		0.2		0.2	V	
	$V_{I} = V_{IH} \text{ or } V_{IL}$							
	$V_{DD} = MIN,$	(I _{OL} = 1 mA)		0.4		0.4	V	
	$V_{I} = V_{IH} \text{ or } V_{IL}$	-						
	$V_{DD} = MIN,$	(I _{OL} = 2 mA)		0.7		0.7	V	
	$V_{I} = V_{IH} \text{ or } V_{IL}$							
V _{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V	
V _{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	5.75	1.7	5.75	V	
$I_{\rm IL}/I_{\rm IH}$	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μΑ	
I _{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		-10	10	-10	10	μΑ	
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns	
C _{IO}	I/O Capacitance			10		10	pF	
I _{CC}	Standby Current			10		20	mA	
IV Curve*	Can be derived from the IBIS model on the web.							

Note: *The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.



PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	5.75	V
V _{IL}	Input Low Voltage		-0.5	0.8	V
I _{IH}	Input High Leakage Current ¹	V _{IN} = 2.7	-	70	μΑ
IIL	Input Low Leakage Current ¹	V _{IN} = 0.5	-	-70	μΑ
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4	-	V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA	-	0.55	V
C _{IN}	Input Pin Capacitance ³		-	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.

2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.

3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH(AC)}	Switching Current High	$0 < V_{OUT} \le 1.4^{-1}$	-44	_	mA
		$1.4 \le V_{OUT} < 2.4^{-1, 2}$	(-44 + (V _{OUT} - 1.4)/0.024)	-	mA
		3.1 < V _{OUT} < V _{CCI} ^{1, 3}	-	EQ 2-1 on page 2-5	_
	(Test Point)	V _{OUT} = 3.1 ³	-	-142	mA
I _{OL(AC)}	Switching Current Low	$V_{OUT} \ge 2.2^{-1}$	95	_	mA
		2.2 > V _{OUT} > 0.55 ¹	(V _{OUT} /0.023)	-	mA
		0.71 > V _{OUT} > 0 ^{1, 3}	-	EQ 2-2 on page 2-5	-
	(Test Point)	V _{OUT} = 0.71 ³	-	206	mA
I _{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	-25 + (V _{IN} + 1)/0.015	-	mA
slew _R	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
slew _F	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Table 2-8 • AC Specifications (5 V PCI Operation)

Notes:

1. Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.

2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.

3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.

4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.



Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}$$
C/W is taken from Table 2-12 on page 2-11

 $T_A = 125$ °C is the maximum limit of ambient (from the datasheet)

Max. Allowed Power =
$$\frac{\text{Max Junction Temp - Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_{J} = 110^{\circ}C$$

 $T_{A} = 70^{\circ}C$

From the datasheet:

 $\theta_{JA} = 18.0^{\circ}C/W$ $\theta_{JC} = 3.2^{\circ}C/W$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{Max Junction Temp - Max. Ambient Temp}{P} = \frac{110^{\circ}C - 70^{\circ}C}{3.00 W} = 13.33^{\circ}C/W$$

EQ 2-13

SX-A Timing Model



Note: *Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route. Figure 2-3 • SX-A Timing Model

Sample Path Calculations

Hardwired Clock

External Setup	=	(t _{INYH} + t _{RD1} + t _{SUD}) – t _{HCKH}
	=	0.6 + 0.3 + 0.8 - 1.8 = - 0.1 ns
Clock-to-Out (Pad-to-Pad)	=	t _{HCKH} + t _{RCO} + t _{RD1} + t _{DHL}
	=	1.8 + 0.8 + 0.3 + 3.9 = 6.8 ns

Routed Clock

External Setup	$= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{RC}$	СКН
	= 0.6 + 0.3 + 0.8 - 3.0 = -1.	3 ns
Clock-to-Out (Pad-to-Pad	$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DH}$	L
	= 3.0 + 0.8 + 0.3 + 3.9 = 8.0) ns

Table 2-15 • A54SX08A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _C	_{CI} = 2.25 V, T _J = 70°C)
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		-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lardwired) Array Clock Networks			8				8		
t _{НСКН}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Arra	y Clock Networks									
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-19 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 Speed -1 Speed		Std. S	Speed	–F S	peed			
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Ou	tput Module Timing ¹									
t _{DLH}	Data-to-Pad Low to High		2.2		2.4		2.9		4.0	ns
t _{DHL}	Data-to-Pad High to Low		2.3		2.6		3.1		4.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.7		1.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.2		2.4		2.9		4.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.8		3.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.3		2.6		3.1		4.3	ns
d_{TLH}^2	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL O	Dutput Module Timing ³							-		
t _{DLH}	Data-to-Pad Low to High		3.0		3.4		4.0		5.6	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.3		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		10.4		11.8		13.8		19.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.6		2.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		18.9		21.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H		3		3.4		4		5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.3		3.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3		3.3		3.9		5.5	ns
d_{TLH}^{2}	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}^2	Delta High to Low—low slew		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. Delays based on 10 pF loading and 25 Ω resistance.

2. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate $[V/ns] = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

3. Delays based on 35 pF loading.

Table 2-25 A54SX16A Timing Characteristics

		-3 Speed	1 -	2 Speed	–1 Sp	beed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min. Ma	c. Mi	n. Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2, 3}										
t _{DLH}	Data-to-Pad Low to High	3.4		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad High to Low	2.6		3.0		3.3		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	11.	5	13.4		15.2		17.9		25.0	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.	3	13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.4		3.9		4.5		5.2		7.3	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}^{4}	Delta Low to High	0.03	1	0.037		0.043		0.051		0.071	ns/pF
${\sf d_{THL}}^4$	Delta High to Low	0.0	7	0.017		0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.05	7	0.06		0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL]HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-31 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _{CCI} :	= 4.75 V, T _J = 70°C)
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		-3 Sp	peed*	-2 S	peed	-1 S	peed	Std.	Speed	-F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Netwo	rks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Arr	ay Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 V$, $V_{CCI} = 4.75 V$, $T_J = 70^{\circ}$ C)

		-3 Speed*		-2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{qcksw}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{qcksw}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.



100-TQFP											
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function								
71	I/O	I/O	I/O								
72	I/O	I/O	I/O								
73	I/O	I/O	I/O								
74	I/O	I/O	I/O								
75	I/O	I/O	I/O								
76	I/O	I/O	I/O								
77	I/O	I/O	I/O								
78	I/O	I/O	I/O								
79	I/O	I/O	I/O								
80	I/O	I/O	I/O								
81	I/O	I/O	I/O								
82	V _{CCI}	V _{CCI}	V _{CCI}								
83	I/O	I/O	I/O								
84	I/O	I/O	I/O								
85	I/O	I/O	I/O								
86	I/O	I/O	I/O								
87	CLKA	CLKA	CLKA								
88	CLKB	CLKB	CLKB								
89	NC	NC	NC								
90	V _{CCA}	V _{CCA}	V _{CCA}								
91	GND	GND	GND								
92	PRA, I/O	PRA, I/O	PRA, I/O								
93	I/O	I/O	I/O								
94	I/O	I/O	I/O								
95	I/O	I/O	I/O								
96	I/O	I/O	I/O								
97	I/O	I/O	I/O								
98	I/O	I/O	I/O								
99	I/O	I/O	I/O								
100	TCK, I/O	TCK, I/O	TCK, I/O								



176-Pin TQFP



Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

176-P	in TQFP	176-P	in TQFP	176-P	in TQFP	176-Pin TQFP				
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function			
1	GND	37	I/O	73	I/O	109	V _{CCA}			
2	TDI, I/O	38	I/O	74	I/O	110	GND			
3	I/O	39	I/O	75	I/O	111	I/O			
4	I/O	40	I/O	76	I/O	112	I/O			
5	I/O	41	I/O	77	I/O	113	I/O			
6	I/O	42	I/O	78	I/O	114	I/O			
7	I/O	43	I/O	79	I/O	115	I/O			
8	I/O	44	GND	80	I/O	116	I/O			
9	I/O	45	I/O	81	I/O	117	I/O			
10	TMS	46	I/O	82	V _{CCI}	118	I/O			
11	V _{CCI}	47	I/O	83	I/O	119	I/O			
12	I/O	48	I/O	84	I/O	120	I/O			
13	I/O	49	I/O	85	I/O	121	I/O			
14	I/O	50	I/O	86	I/O	122	V _{CCA}			
15	I/O	51	I/O	87	TDO, I/O	123	GND			
16	I/O	52	V _{CCI}	88	I/O	124	V _{CCI}			
17	I/O	53	I/O	89	GND	125	I/O			
18	I/O	54	I/O	90	I/O	126	I/O			
19	I/O	55	I/O	91	I/O	127	I/O			
20	I/O	56	I/O	92	I/O	128	I/O			
21	GND	57	I/O	93	I/O	129	I/O			
22	V _{CCA}	58	I/O	94	I/O	130	I/O			
23	GND	59	I/O	95	I/O	131	I/O			
24	I/O	60	I/O	96	I/O	132	I/O			
25	TRST, I/O	61	I/O	97	I/O	133	GND			
26	I/O	62	I/O	98	V _{CCA}	134	I/O			
27	I/O	63	I/O	99	V _{CCI}	135	I/O			
28	I/O	64	PRB, I/O	100	I/O	136	I/O			
29	I/O	65	GND	101	I/O	137	I/O			
30	I/O	66	V _{CCA}	102	I/O	138	I/O			
31	I/O	67	NC	103	I/O	139	I/O			
32	V _{CCI}	68	I/O	104	I/O	140	V _{CCI}			
33	V _{CCA}	69	HCLK	105	I/O	141	I/O			
34	I/O	70	I/O	106	I/O	142	I/O			
35	I/O	71	I/O	107	I/O	143	I/O			
36	I/O	72	I/O	108	GND	144	I/O			



176-Pi	n TQFP
Pin Number	A54SX32A Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V _{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V _{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

144-Pin FBGA



Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

484-Pin FBGA

	1	2	3	4	5	6	/	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	252	6
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K L	00	000	00	00	00					000	00	00	000	00	00	000	00					00	00	0		2
M N	00	00	00	00	00					00	00	00	00	00	00	000	00					00	0	0		2
P R	00	00	00	00	00					00	00	00	00	00	00	000	00					00	0	0)
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w	000	000	000	000	000																	000	000	000)
AA AR	000	000	000	000	000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000	000	000		
AC AD	000	õõ	õ	00	000	000	000	000	000	000	000	000	õ	00	õ	õ	000	õ	õ	õ	000	õ	õ	000		$\hat{\mathbf{b}}$
AE AF	000	000	000	000	000	000	000	000	000	0 0	000	000	000	000	000	000	000	000	000	000	000	000	ŏ o	000		5
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Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

	Actel	
SX-A Fa	amily FPGAs	

484-Pin FBGA										
Pin Number	A54SX32A Function	A54SX72A Function								
T3	I/O	I/O								
T4	I/O	I/O								
T5	I/O	I/O								
T10	GND	GND								
T11	GND	GND								
T12	GND	GND								
T13	GND	GND								
T14	GND	GND								
T15	GND	GND								
T16	GND	GND								
T17	GND	GND								
T22	I/O	I/O								
T23	I/O	I/O								
T24	I/O	I/O								
T25	NC*	I/O								
T26	NC*	I/O								
U1	I/O	I/O								
U2	V _{CCI}	V _{CCI}								
U3	I/O	I/O								
U4	I/O	I/O								
U5	I/O	I/O								
U10	GND	GND								
U11	GND	GND								
U12	GND	GND								
U13	GND	GND								
U14	GND	GND								
U15	GND	GND								
U16	GND	GND								
U17	GND	GND								
U22	I/O	I/O								
U23	I/O	I/O								
U24	I/O	I/O								
U25	V _{CCI}	V _{CCI}								
U26	I/O	I/O								
V1	NC*	I/O								

484-Pin FBGA											
Pin Number	Pin A54SX32A Number Function										
V2	NC*	I/O									
V3	I/O	I/O									
V4	I/O	I/O									
V5	I/O	I/O									
V22	V _{CCA}	V _{CCA}									
V23	I/O	I/O									
V24	I/O	I/O									
V25	NC*	I/O									
V26	NC*	I/O									
W1	I/O	I/O									
W2	I/O	I/O									
W3	I/O	I/O									
W4	I/O	I/O									
W5	I/O	I/O									
W22	I/O	I/O									
W23	V _{CCA}	V _{CCA}									
W24	I/O	I/O									
W25	NC*	I/O									
W26	NC*	I/O									
Y1	NC*	I/O									
Y2	NC*	I/O									
Y3	I/O	I/O									
Y4	I/O	I/O									
Y5	NC*	I/O									
Y22	I/O	I/O									
Y23	I/O	I/O									
Y24	V _{CCI}	V _{CCI}									
Y25	I/O	I/O									
Y26	I/O	I/O									

Note: *These pins must be left floating on the A54SX32A device.



Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	-3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1	RoHS information was added to the "Ordering Information".	ii
February 2005	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the -3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9