



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	171
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-2pq208

Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Speed Grade and Temperature Grade Matrix

	F	Std	-1	-2	-3
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

Notes:

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.

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Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000

different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

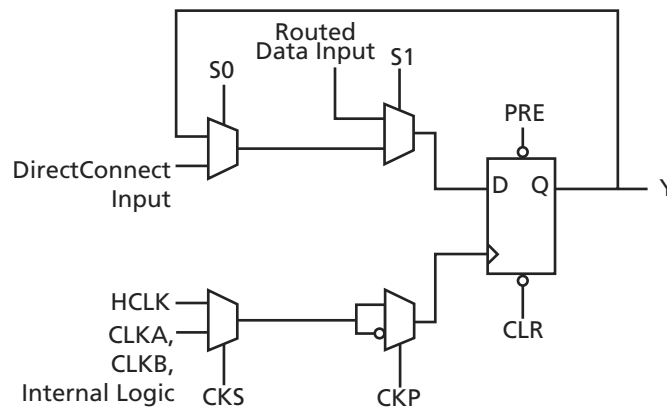


Figure 1-2 • R-Cell

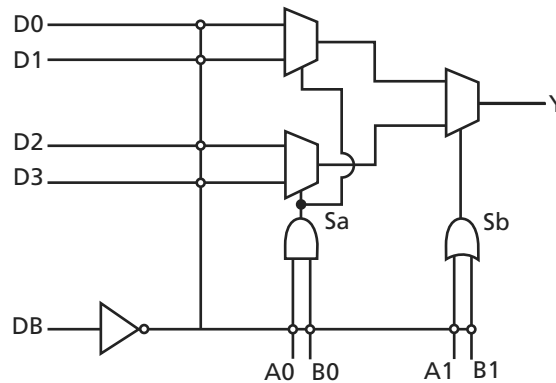


Figure 1-3 • C-Cell

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CC} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices

http://www.actel.com/documents/GlobalClk_AN.pdf

Using A54SX72A and RT54SX72S Quadrant Clocks

http://www.actel.com/documents/QCLK_AN.pdf

Implementation of Security in Actel Antifuse FPGAs

http://www.actel.com/documents/Antifuse_Security_AN.pdf

Actel eX, SX-A, and RTSX-S I/Os

http://www.actel.com/documents/AntifuseIO_AN.pdf

Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

http://www.actel.com/documents/HotSwapColdSparing_AN.pdf

Programming Antifuse Devices

http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs

http://www.actel.com/documents/HR SXA_DS.pdf

SX-A Automotive Family FPGAs

http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide

http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Table 2-17 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.3		1.5		2.3	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.2		1.4		2.0	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.3		1.5		2.1	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.9	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		1.0		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-23 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)	1.2		1.4		1.6		1.8		2.8		ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)	1.0		1.1		1.3		1.5		2.2		ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew	0.3		0.3		0.4		0.4		0.6		ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency	357		294		263		227		167		MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)	1.0		1.2		1.3		1.5		2.1		ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)	1.1		1.3		1.4		1.7		2.3		ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.7		ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.8		ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (50% Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (100% Load)	1.0		1.1		1.3		1.5		2.1		ns

Note: *All –3 speed grades have been discontinued.

Table 2-26 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.0		2.3		2.6		3.1		4.3		ns
t _{DHL}	Data-to-Pad High to Low	2.2		2.5		2.8		3.3		4.6		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.0		2.3		2.6		3.1		4.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.2		2.5		2.8		3.3		4.6		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.8		3.2		3.6		4.3		6.0		ns
t _{DHL}	Data-to-Pad High to Low	2.7		3.1		3.5		4.1		5.7		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	9.5		10.9		12.4		14.6		20.4		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.8		3.2		3.6		4.3		6.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.7		3.1		3.5		4.1		5.7		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-28 • A54SX32A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.9		1.1		1.2		1.4		1.9	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays³												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-35 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	1.0		1.1		1.3		1.5		2.0		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.7		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.6		0.7		1		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.7		0.8		0.9		1.3		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.9		1		1.1		1.5		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.5		1.7		2.1		2.9		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2.2		2.5		3		4.2		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.7		0.8		0.9		1.1		1.5		ns
t _{CLR}	Asynchronous Clear-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.8		1.0		1.4		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.3		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	0.8		1.0		1.1		1.3		1.7		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.6		0.7		0.7		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.0		1.4		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.7		0.7		0.8		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	1.0		1.2		1.3		1.5		2.1		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-37 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-40 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.3		2.7		3.0		3.6		5.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.0		3.6		5.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	3.2		3.7		4.2		5.0		6.9		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.7		4.2		4.9		6.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3		11.9		13.5		15.8		22.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2		3.7		4.2		5.0		6.9		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.7		4.2		4.9		6.9		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HLH|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t _{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d _{TLH} ³	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t _{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d _{TLH} ³	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Package Pin Assignments

208-Pin PQFP

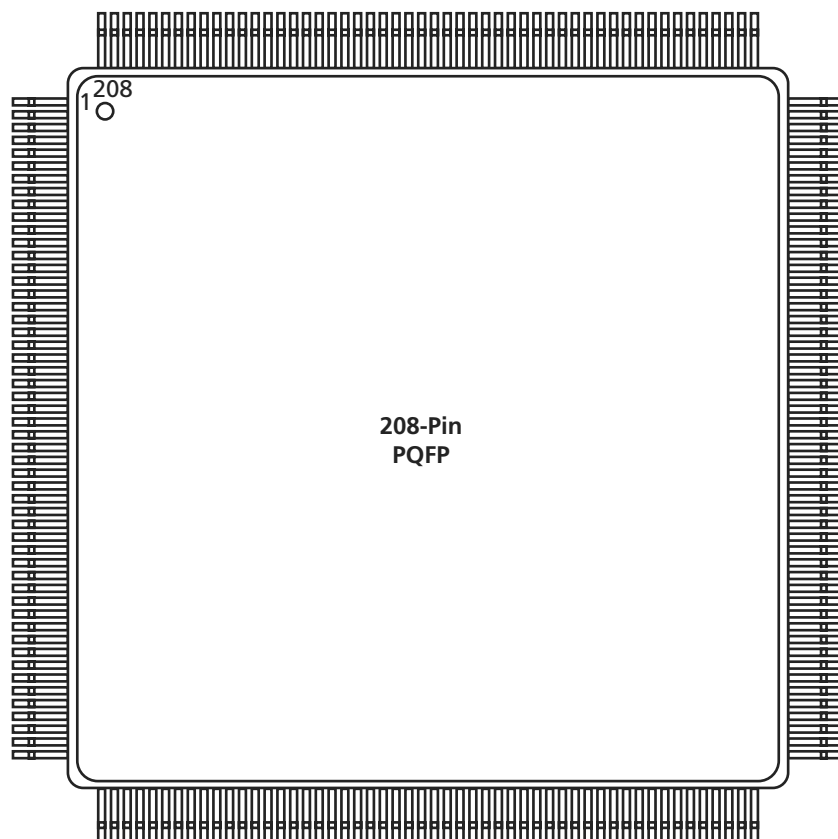


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V _{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

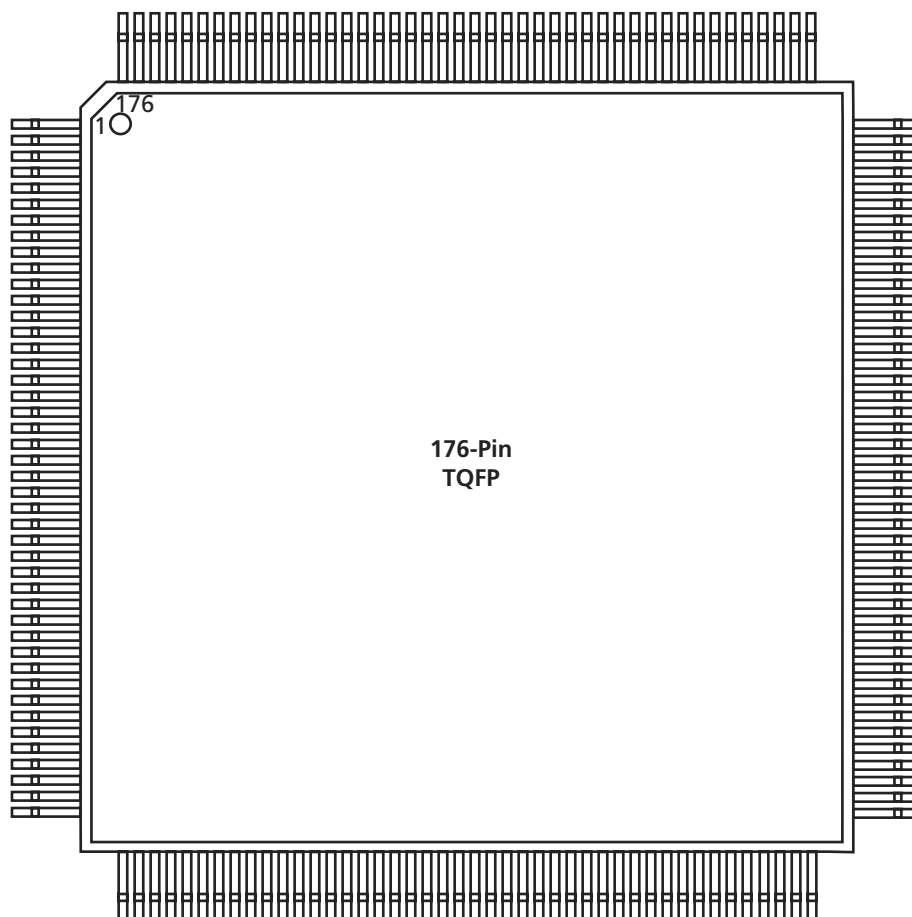


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

176-Pin TQFP	
Pin Number	A54SX32A Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V _{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V _{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V _{CCA}	V _{CCA}	V _{CCA}
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND
C4	I/O	I/O	I/O
C5	NC	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O
E7	I/O	I/O	QCLKC
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V _{CCI}	V _{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V _{CCI}	V _{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V _{CCI}	V _{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V _{CCA}	V _{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V _{CCI}	V _{CCI}
E26	GND	GND
F1	V _{CCI}	V _{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V _{CCA}	V _{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V _{CCI}	V _{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V _{CCI}	V _{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V _{CCA}	V _{CCA}

Note: *These pins must be left floating on the A54SX32A device.