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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	171
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-cq208

General Description

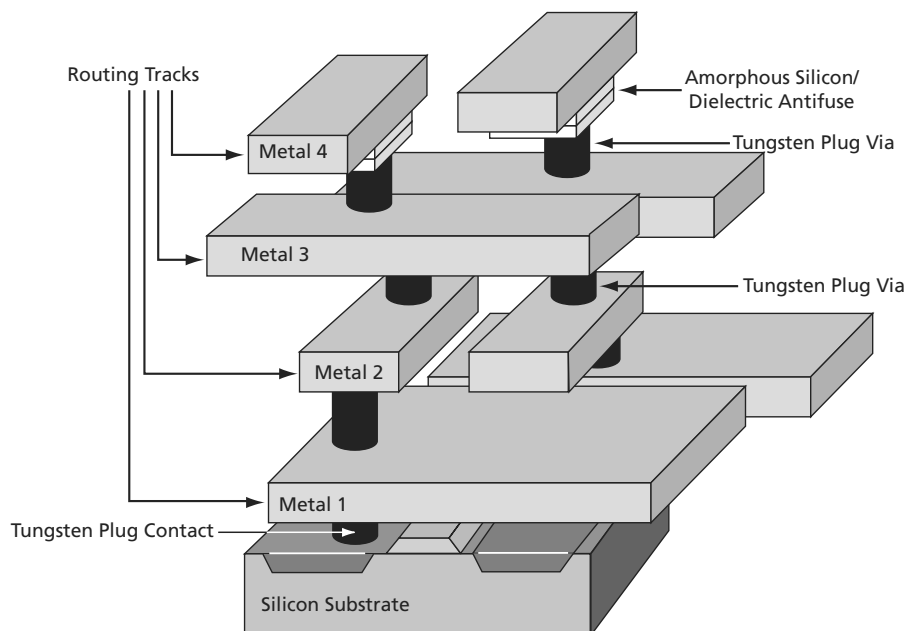
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

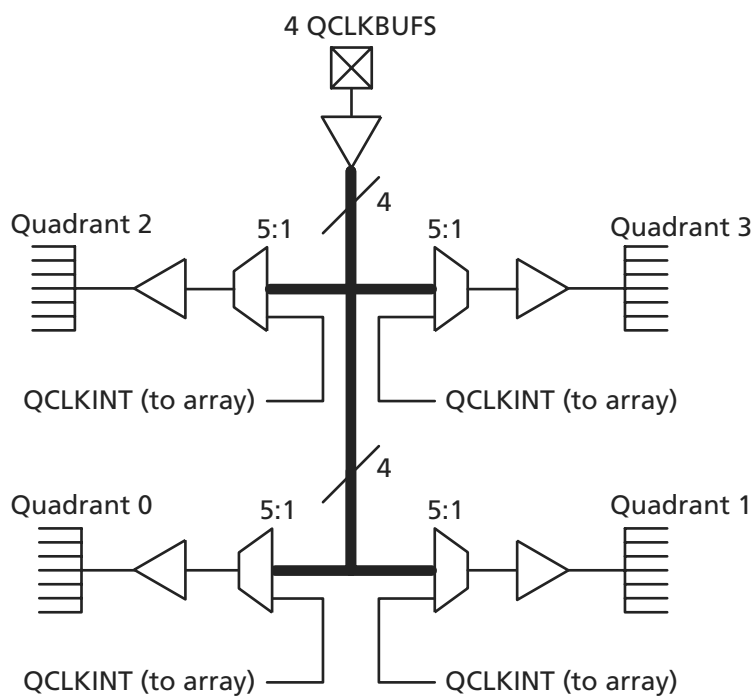


Figure 1-9 • SX-A QCLK Architecture

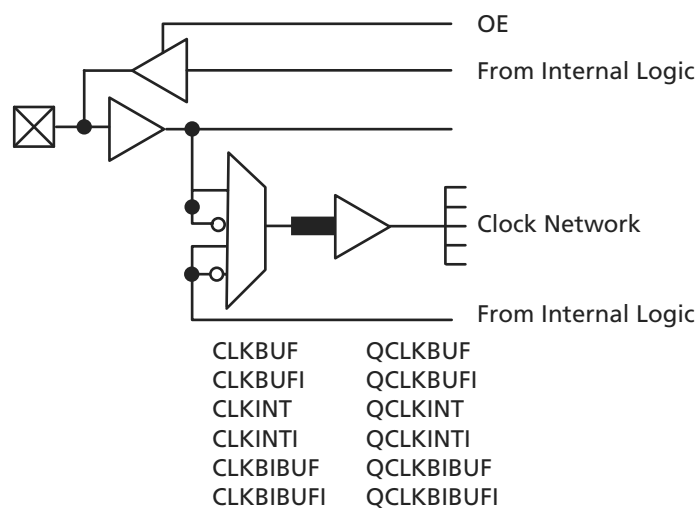


Figure 1-10 • A54SX72A Routed Clock and QCLK Buffer

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CC} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

JTAG Mode	TRST ¹	Security Fuse Programmed	PRA, PRB ²	TDI, TCK, TDO ²
Dedicated	Low	No	User I/O ³	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O ³	User I/O ³
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CC1} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CC1} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	5.75	V
V _{IL}	Input Low Voltage		–0.5	0.8	V
I _{IH}	Input High Leakage Current ¹	V _{IN} = 2.7	–	70	μA
I _{IL}	Input Low Leakage Current ¹	V _{IN} = 0.5	–	–70	μA
V _{OH}	Output High Voltage	I _{OUT} = –2 mA	2.4	–	V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA	–	0.55	V
C _{IN}	Input Pin Capacitance ³		–	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

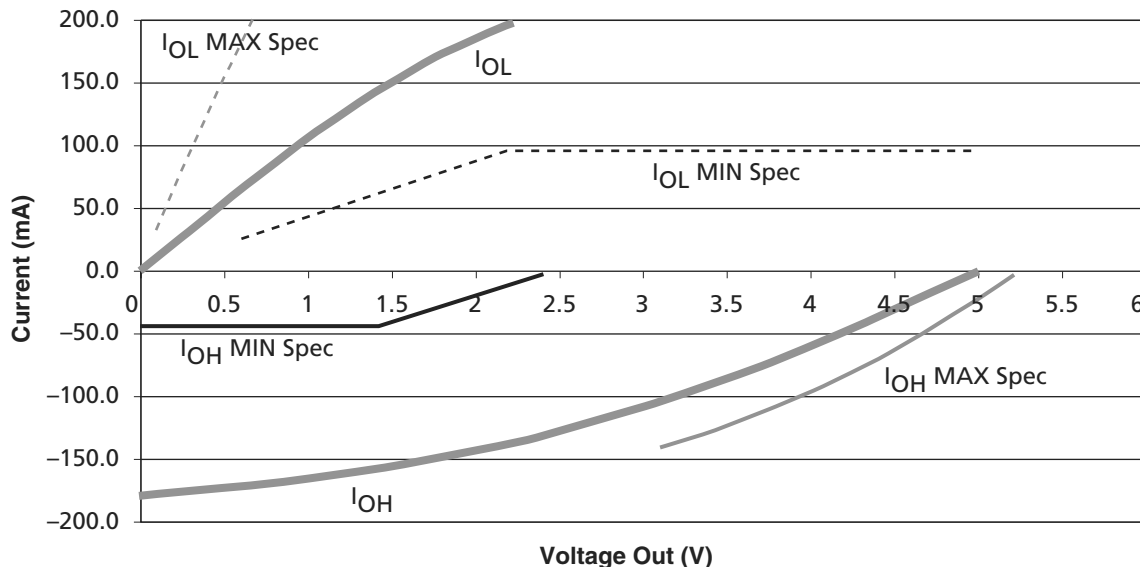


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CCI}$	–	V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CCI}$	-10	+10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$	–	V
V_{OL}	Output Low Voltage	$I_{OUT} = 1,500 \mu A$		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance ³		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

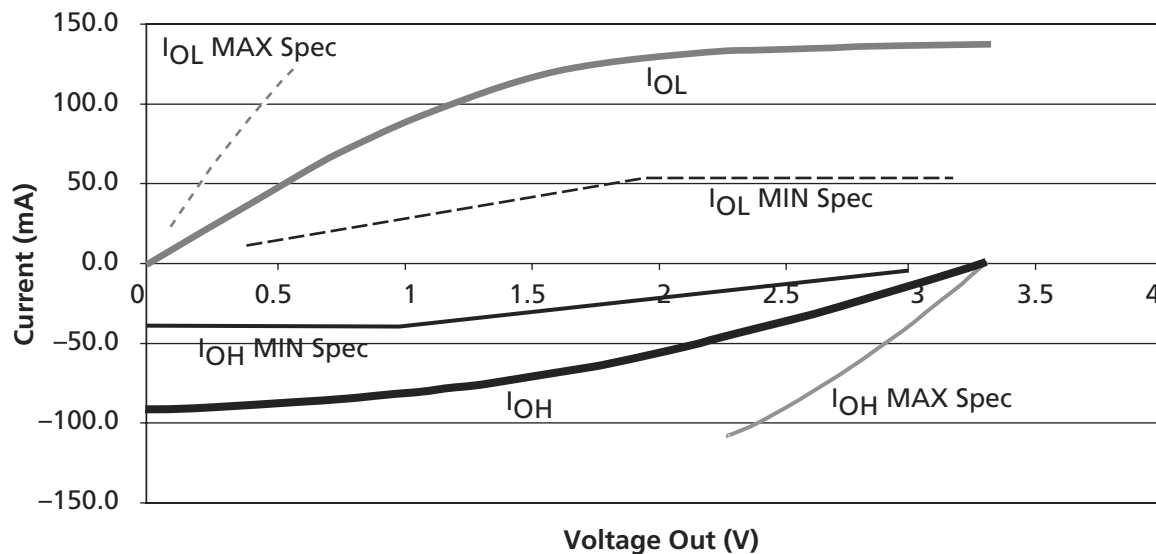


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Table 2-32 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{2,3}												
t _{DLH}	Data-to-Pad Low to High	3.3		3.8		4.2		5.0		7.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	11.1		12.8		14.5		17.0		23.8		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8		3.2		3.7		5.2		ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8		13.7		15.5		18.2		25.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.3		3.8		4.2		5.0		7.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5		2.8		3.3		4.7		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ⁴	Delta Low to High	0.031		0.037		0.043		0.051		0.071		ns/pF
d _{THL} ⁴	Delta High to Low	0.017		0.017		0.023		0.023		0.037		ns/pF
d _{THLS} ⁴	Delta High to Low—low slew	0.057		0.06		0.071		0.086		0.117		ns/pF

Note:

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-37 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Package Pin Assignments

208-Pin PQFP

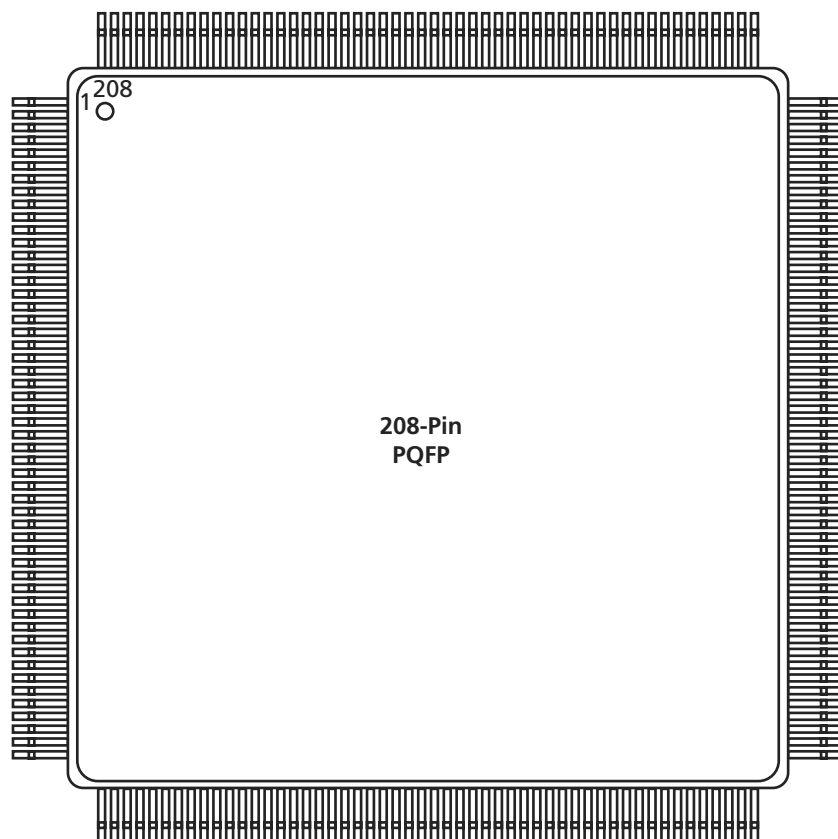


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V _{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V _{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V _{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP		176-Pin TQFP		176-Pin TQFP		176-Pin TQFP	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
1	GND	37	I/O	73	I/O	109	V _{CCA}
2	TDI, I/O	38	I/O	74	I/O	110	GND
3	I/O	39	I/O	75	I/O	111	I/O
4	I/O	40	I/O	76	I/O	112	I/O
5	I/O	41	I/O	77	I/O	113	I/O
6	I/O	42	I/O	78	I/O	114	I/O
7	I/O	43	I/O	79	I/O	115	I/O
8	I/O	44	GND	80	I/O	116	I/O
9	I/O	45	I/O	81	I/O	117	I/O
10	TMS	46	I/O	82	V _{CCI}	118	I/O
11	V _{CCI}	47	I/O	83	I/O	119	I/O
12	I/O	48	I/O	84	I/O	120	I/O
13	I/O	49	I/O	85	I/O	121	I/O
14	I/O	50	I/O	86	I/O	122	V _{CCA}
15	I/O	51	I/O	87	TDO, I/O	123	GND
16	I/O	52	V _{CCI}	88	I/O	124	V _{CCI}
17	I/O	53	I/O	89	GND	125	I/O
18	I/O	54	I/O	90	I/O	126	I/O
19	I/O	55	I/O	91	I/O	127	I/O
20	I/O	56	I/O	92	I/O	128	I/O
21	GND	57	I/O	93	I/O	129	I/O
22	V _{CCA}	58	I/O	94	I/O	130	I/O
23	GND	59	I/O	95	I/O	131	I/O
24	I/O	60	I/O	96	I/O	132	I/O
25	TRST, I/O	61	I/O	97	I/O	133	GND
26	I/O	62	I/O	98	V _{CCA}	134	I/O
27	I/O	63	I/O	99	V _{CCI}	135	I/O
28	I/O	64	PRB, I/O	100	I/O	136	I/O
29	I/O	65	GND	101	I/O	137	I/O
30	I/O	66	V _{CCA}	102	I/O	138	I/O
31	I/O	67	NC	103	I/O	139	I/O
32	V _{CCI}	68	I/O	104	I/O	140	V _{CCI}
33	V _{CCA}	69	HCLK	105	I/O	141	I/O
34	I/O	70	I/O	106	I/O	142	I/O
35	I/O	71	I/O	107	I/O	143	I/O
36	I/O	72	I/O	108	GND	144	I/O

176-Pin TQFP	
Pin Number	A54SX32A Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V _{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V _{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

329-Pin PBGA	
Pin Number	A54SX32A Function
D11	V _{CCA}
D12	NC
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V _{CCI}
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V _{CCA}
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	NC
L10	GND
L11	GND
L12	GND
L13	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
L14	GND
L20	NC
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V _{CCA}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V _{CCA}
M21	I/O
M22	I/O
M23	V _{CCI}
N1	I/O
N2	TRST, I/O
N3	I/O
N4	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V _{CCA}
U4	I/O
U20	I/O
U21	V _{CCA}
U22	I/O
U23	I/O
V1	V _{CCI}
V2	I/O
V3	I/O
V4	I/O
V20	I/O
V21	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V _{CCA}	V _{CCA}	V _{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D1	I/O	I/O	I/O
D2	V _{CCI}	V _{CCI}	V _{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V _{CCI}	V _{CCI}	V _{CCI}
E7	V _{CCI}	V _{CCI}	V _{CCI}
E8	V _{CCI}	V _{CCI}	V _{CCI}
E9	V _{CCA}	V _{CCA}	V _{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
K5	I/O	I/O	I/O
K6	V _{CCI}	V _{CCI}	V _{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V _{CCI}	V _{CCI}	V _{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V _{CCI}	V _{CCI}	V _{CCI}
L8	V _{CCI}	V _{CCI}	V _{CCI}
L9	V _{CCI}	V _{CCI}	V _{CCI}
L10	V _{CCI}	V _{CCI}	V _{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V _{CCA}	V _{CCA}	V _{CCA}
P14	I/O	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC *	NC
K25	NC *	I/O
K26	NC *	I/O
L1	NC *	I/O
L2	NC *	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC *	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC *	I/O
M26	NC *	I/O
N1	I/O	I/O
N2	V _{CCI}	V _{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V _{CCA}	V _{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC *	NC
P1	NC *	I/O
P2	NC *	I/O
P3	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
P4	I/O	I/O
P5	V _{CCA}	V _{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V _{CCI}	V _{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC *	I/O
R2	NC *	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	NC *	I/O
R26	NC *	I/O
T1	NC *	I/O
T2	NC *	I/O

Note: *These pins must be left floating on the A54SX32A device.