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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 6036 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 203 |
| Number of Gates | 108000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-ffgg256 |

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 2-14*

where:

$\theta_{CS}$ = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

## Input Buffer Delays

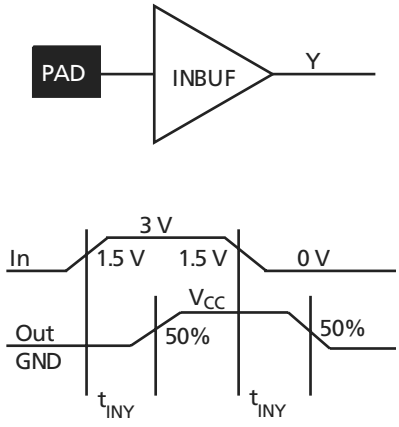


*Figure 2-6* • **Input Buffer Delays**

## C-Cell Delays

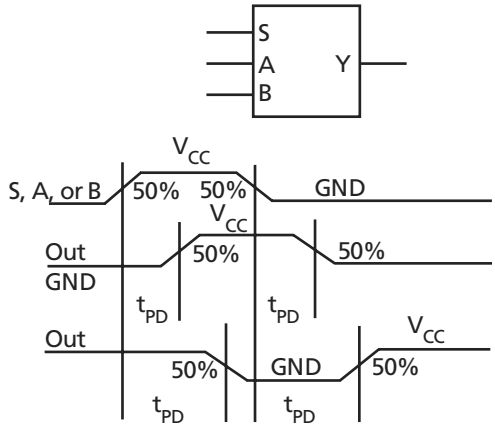


*Figure 2-7* • **C-Cell Delays**

## Cell Timing Characteristics

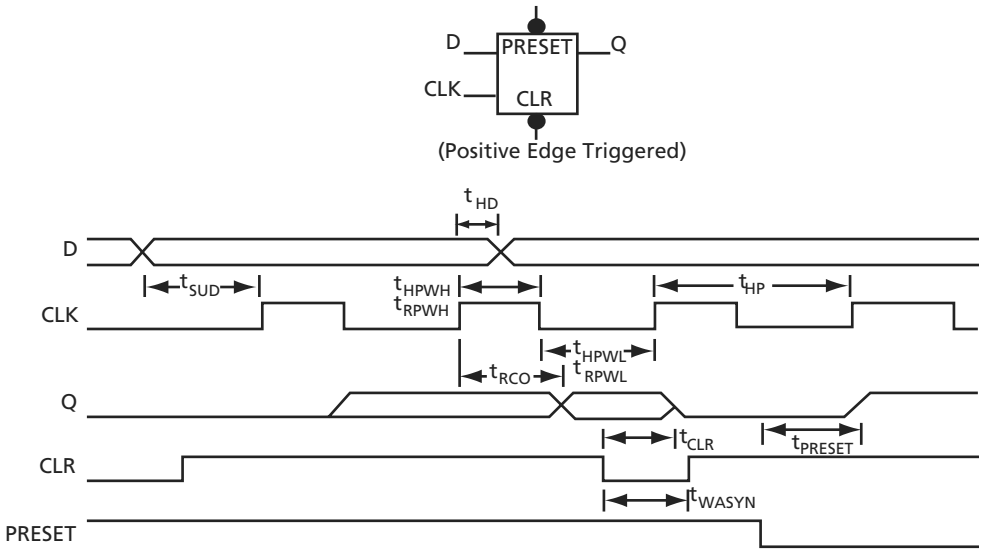


*Figure 2-8* • **Flip-Flops**

# Timing Characteristics

*Table 2-14* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |

***Notes:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-17* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.5 | | 2.3 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 1.0 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-26* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **3.3 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 9.5 | | 10.9 | | 12.4 | | 14.6 | | 20.4 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-28* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.8 | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-31* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.7 | | 1.9 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.5 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.2 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-35* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.0 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-36* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| $t_{HP}$ | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.7 | | 4.3 | | 6.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.9 | | 3.3 | | 3.8 | | 4.5 | | 6.2 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.1 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| **Quadrant Array Clock Networks** | | | | | | | | | | | | |
| $t_{QCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{QCHKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{QCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{QCHKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O | I/O |
| 73 | NC | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | QCLKA |
| 75 | NC | I/O | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O | PRB,I/O |
| 77 | GND | GND | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND | GND | GND |
| 80 | NC | NC | NC | NC |
| 81 | I/O | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O | $V_{CCI}$ |
| 84 | I/O | I/O | I/O | QCLKB |
| 85 | NC | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O | I/O |
| 88 | NC | I/O | I/O | I/O |
| 89 | I/O | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O | I/O |
| 91 | NC | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O | I/O |
| 94 | NC | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O | I/O |
| 97 | NC | I/O | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O | I/O |
| 105 | GND | GND | GND | GND |

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 106 | NC | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O | I/O |
| 108 | NC | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | NC | I/O | I/O | GND |
| 117 | I/O | I/O | I/O | $V_{CCA}$ |
| 118 | I/O | I/O | I/O | I/O |
| 119 | NC | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O | I/O |
| 122 | NC | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O | I/O |
| 125 | NC | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O | I/O |
| 129 | GND | GND | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND | GND | GND |
| 132 | NC | NC | NC | I/O |
| 133 | I/O | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O | I/O |
| 135 | NC | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O | I/O |
| 138 | NC | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O | I/O |

# 100-Pin TQFP

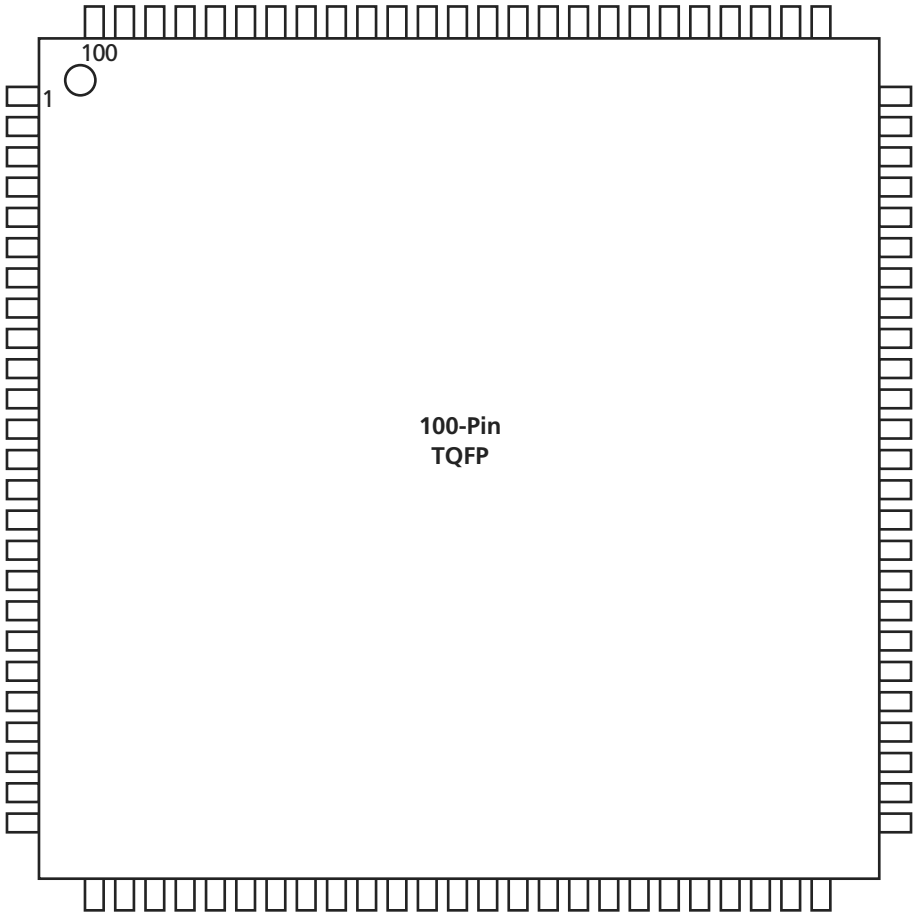


*Figure 3-2* • **100-Pin TQFP**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | NC | NC | NC |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | TRST, I/O | TRST, I/O | TRST, I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |
| 37 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | NC | NC | NC |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |

| 176-Pin TQFP | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | I/O |
| 149 | I/O |
| 150 | I/O |
| 151 | I/O |
| 152 | CLKA |
| 153 | CLKB |
| 154 | NC |
| 155 | GND |
| 156 | $V_{CCA}$ |
| 157 | PRA, I/O |
| 158 | I/O |
| 159 | I/O |
| 160 | I/O |
| 161 | I/O |
| 162 | I/O |
| 163 | I/O |
| 164 | I/O |
| 165 | I/O |
| 166 | I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | $V_{CCI}$ |
| 170 | I/O |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | TCK, I/O |

# 329-Pin PBGA

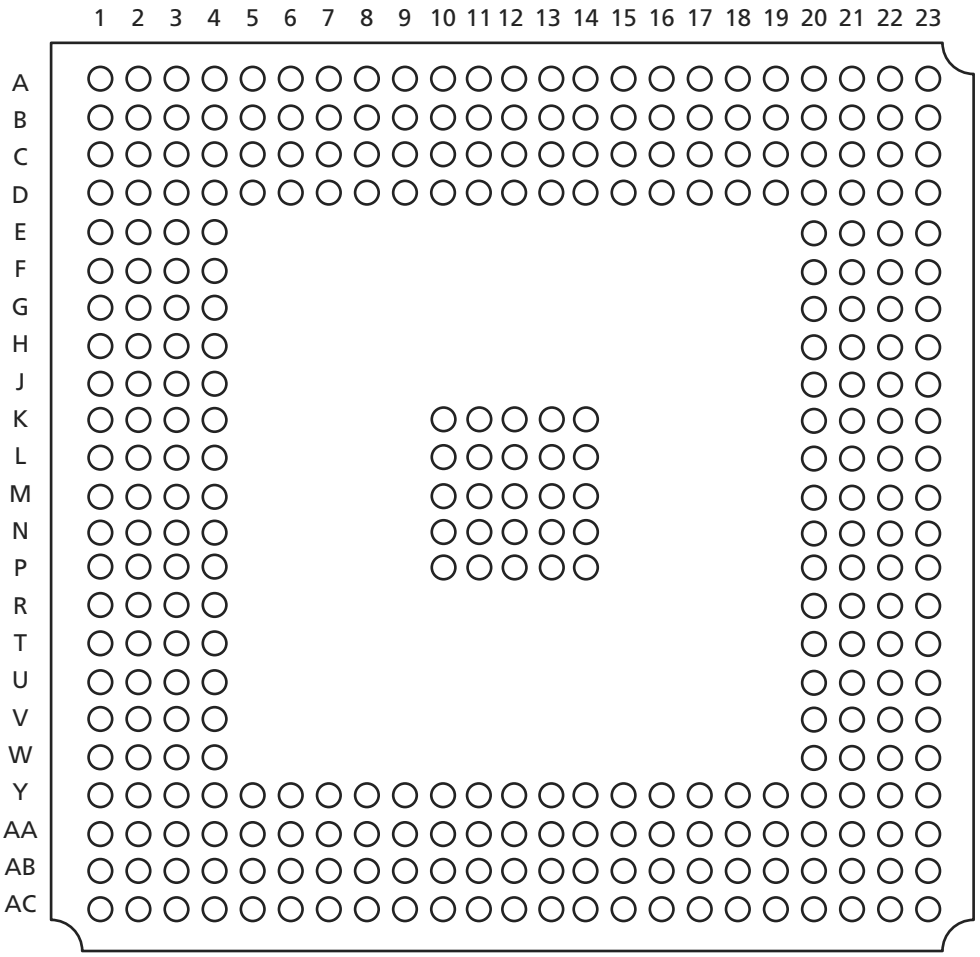


*Figure 3-5* • **329-Pin PBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 144-Pin FBGA

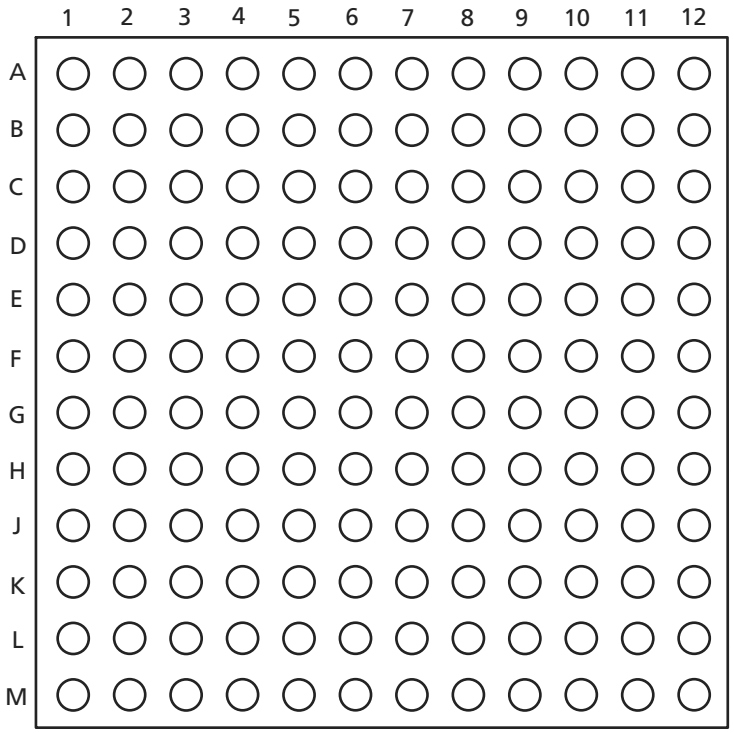


*Figure 3-6* • **144-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 256-Pin FBGA

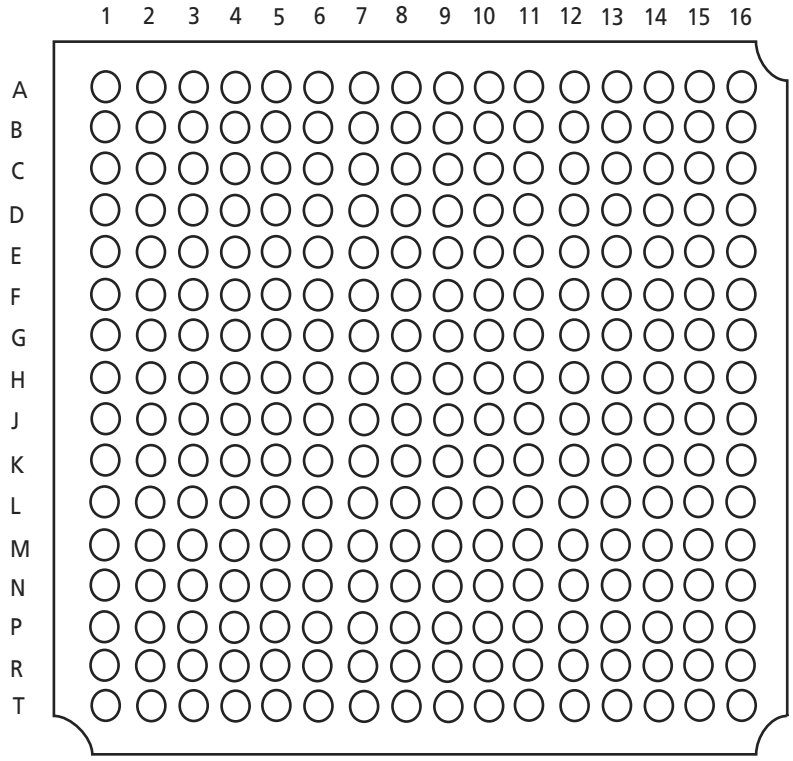


*Figure 3-7* • **256-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| K5 | I/O | I/O | I/O |
| K6 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K7 | GND | GND | GND |
| K8 | GND | GND | GND |
| K9 | GND | GND | GND |
| K10 | GND | GND | GND |
| K11 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K12 | I/O | I/O | I/O |
| K13 | I/O | I/O | I/O |
| K14 | I/O | I/O | I/O |
| K15 | NC | I/O | I/O |
| K16 | I/O | I/O | I/O |
| L1 | I/O | I/O | I/O |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L9 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| L13 | I/O | I/O | I/O |
| L14 | I/O | I/O | I/O |
| L15 | I/O | I/O | I/O |
| L16 | NC | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | I/O | I/O | QCLKA |
| M8 | PRB, I/O | PRB, I/O | PRB, I/O |
| M9 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| M10 | I/O | I/O | I/O |
| M11 | I/O | I/O | I/O |
| M12 | NC | I/O | I/O |
| M13 | I/O | I/O | I/O |
| M14 | NC | I/O | I/O |
| M15 | I/O | I/O | I/O |
| M16 | I/O | I/O | I/O |
| N1 | I/O | I/O | I/O |
| N2 | I/O | I/O | I/O |
| N3 | I/O | I/O | I/O |
| N4 | I/O | I/O | I/O |
| N5 | I/O | I/O | I/O |
| N6 | I/O | I/O | I/O |
| N7 | I/O | I/O | I/O |
| N8 | I/O | I/O | I/O |
| N9 | I/O | I/O | I/O |
| N10 | I/O | I/O | I/O |
| N11 | I/O | I/O | I/O |
| N12 | I/O | I/O | I/O |
| N13 | I/O | I/O | I/O |
| N14 | I/O | I/O | I/O |
| N15 | I/O | I/O | I/O |
| N16 | I/O | I/O | I/O |
| P1 | I/O | I/O | I/O |
| P2 | GND | GND | GND |
| P3 | I/O | I/O | I/O |
| P4 | I/O | I/O | I/O |
| P5 | NC | I/O | I/O |
| P6 | I/O | I/O | I/O |
| P7 | I/O | I/O | I/O |
| P8 | I/O | I/O | I/O |
| P9 | I/O | I/O | I/O |
| P10 | NC | I/O | I/O |
| P11 | I/O | I/O | I/O |
| P12 | I/O | I/O | I/O |
| P13 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| P14 | I/O | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| T3 | I/O | I/O |
| T4 | I/O | I/O |
| T5 | I/O | I/O |
| T10 | GND | GND |
| T11 | GND | GND |
| T12 | GND | GND |
| T13 | GND | GND |
| T14 | GND | GND |
| T15 | GND | GND |
| T16 | GND | GND |
| T17 | GND | GND |
| T22 | I/O | I/O |
| T23 | I/O | I/O |
| T24 | I/O | I/O |
| T25 | NC* | I/O |
| T26 | NC* | I/O |
| U1 | I/O | I/O |
| U2 | $V_{CCI}$ | $V_{CCI}$ |
| U3 | I/O | I/O |
| U4 | I/O | I/O |
| U5 | I/O | I/O |
| U10 | GND | GND |
| U11 | GND | GND |
| U12 | GND | GND |
| U13 | GND | GND |
| U14 | GND | GND |
| U15 | GND | GND |
| U16 | GND | GND |
| U17 | GND | GND |
| U22 | I/O | I/O |
| U23 | I/O | I/O |
| U24 | I/O | I/O |
| U25 | $V_{CCI}$ | $V_{CCI}$ |
| U26 | I/O | I/O |
| V1 | NC* | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| V2 | NC* | I/O |
| V3 | I/O | I/O |
| V4 | I/O | I/O |
| V5 | I/O | I/O |
| V22 | $V_{CCA}$ | $V_{CCA}$ |
| V23 | I/O | I/O |
| V24 | I/O | I/O |
| V25 | NC* | I/O |
| V26 | NC* | I/O |
| W1 | I/O | I/O |
| W2 | I/O | I/O |
| W3 | I/O | I/O |
| W4 | I/O | I/O |
| W5 | I/O | I/O |
| W22 | I/O | I/O |
| W23 | $V_{CCA}$ | $V_{CCA}$ |
| W24 | I/O | I/O |
| W25 | NC* | I/O |
| W26 | NC* | I/O |
| Y1 | NC* | I/O |
| Y2 | NC* | I/O |
| Y3 | I/O | I/O |
| Y4 | I/O | I/O |
| Y5 | NC* | I/O |
| Y22 | I/O | I/O |
| Y23 | I/O | I/O |
| Y24 | $V_{CCI}$ | $V_{CCI}$ |
| Y25 | I/O | I/O |
| Y26 | I/O | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v5.2 (June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1 February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| | Table 2-11 was updated. | 2-9 |