

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	203
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-fgg256a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. C = Commercial

- 2. I = Industrial
- 3. A = Automotive
- 4. M = Military
- 5. B = MIL-STD-883 Class B

6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.

7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Speed Grade and Temperature Grade Matrix

	F	Std	-1	-2	-3
Commercial	1	1	1	1	Discontinued
Industrial		1	1	1	Discontinued
Automotive		1			
Military		1	1		
MIL-STD-883B		1	1		

Notes:

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.

2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.



General Description

Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements



Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters



Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters



Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • SX-A Clock Resources

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4



Figure 1-7 • SX-A HCLK Clock Buffer



Figure 1-8 • SX-A Routed Clock Buffer

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer builtin programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any userdefined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.



Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

 $I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CCI} > V_{OUT} > 3.1V$ $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for 0V < V_{OUT} < 0.71V

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V _{IH}	Input High Voltage		0.5V _{CCI}	V _{CCI} + 0.5	V
V _{IL}	Input Low Voltage		-0.5	0.3V _{CCI}	V
I _{IPU}	Input Pull-up Voltage ¹		0.7V _{CCI}	-	V
IIL	Input Leakage Current ²	0 < V _{IN} < V _{CCI}	-10	+10	μΑ
V _{OH}	Output High Voltage	I _{OUT} = -500 μA	0.9V _{CCI}	-	V
V _{OL}	Output Low Voltage	I _{OUT} = 1,500 μA		0.1V _{CCI}	V
C _{IN}	Input Pin Capacitance ³		-	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

EQ 2-1

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.

2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.

3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Timing Characteristics

Table 2-14 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 S	peed	-1 Speed		Std. Speed		-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	igation Delays ¹									
t _{PD}	Internal Array Module		0.9		1.1		1.2		1.7	ns
Predicted Ro	outing Delays ²			4						
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns
R-Cell Timin	g									<u></u>
t _{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.7		0.9		1.2	ns
t _{sud}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays			1						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.8		0.9		1.0		1.4	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.0		1.2		1.4		1.9	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.3	ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.1		1.3		1.8	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-14 A545X08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCA} = 2.25 V$, $V_{CCI} = 3.0 V$, $T_J = 70^{\circ}$ C)

		-2 Speed		-1 Speed		Std. Speed		-F Speed		
Parameter	Description	Min. N	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t _{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Modul	e Predicted Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t _{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-15 • A54SX08A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _C	_{CI} = 2.25 V, T _J = 70°C)
----------------------------------	---	--

		-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
Dedicated (H	lardwired) Array Clock Networks			8				8			
t _{НСКН}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns	
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns	
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns	
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns	
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns	
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns	
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz	
Routed Array Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns	
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns	
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns	
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns	
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns	
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns	
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns	
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns	
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns	
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns	
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns	

Table 2-16 A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions	V _{CCA} = 2.25 V, V _{CC}	₁ = 3.0 V, T _J = 70°C)
-----------------------------------	--	--

		-2 S	peed	-1 S	peed	Std.	Speed	-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lardwired) Array Clock Networks									
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.3		1.5		1.7		2.6	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.1		1.3		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPVVL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.5		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Arra	y Clock Networks									
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		1.9	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.2		1.3		1.6		2.2	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPVVL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.8		0.9		1.1		1.5	ns

Table 2-19 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 Speed -1 Speed Ste		Std. S	Speed	–F S	peed			
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Ou	tput Module Timing ¹									
t _{DLH}	Data-to-Pad Low to High		2.2		2.4		2.9		4.0	ns
t _{DHL}	Data-to-Pad High to Low		2.3		2.6		3.1		4.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.7		1.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.2		2.4		2.9		4.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.8		3.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.3		2.6		3.1		4.3	ns
d_{TLH}^2	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL O	Dutput Module Timing ³							-		
t _{DLH}	Data-to-Pad Low to High		3.0		3.4		4.0		5.6	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.3		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		10.4		11.8		13.8		19.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.6		2.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		18.9		21.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H		3		3.4		4		5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.3		3.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3		3.3		3.9		5.5	ns
d_{TLH}^{2}	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}^2	Delta High to Low—low slew		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. Delays based on 10 pF loading and 25 Ω resistance.

2. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate $[V/ns] = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

3. Delays based on 35 pF loading.

Table 2-28 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-3 Sp	beed ¹	-2 S	peed	–1 Speed		Std. Speed		–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module		0.8		0.9		1.1		1.2		1.7	ns
Predicted R	outing Delays ³											
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays					-						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.2		1.3		1.5		1.8		2.5	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.6		0.7		0.8		0.9		1.3	ns
t _{INYH}	lnput Data Pad to Y High 3.3 V LVTTL		0.8		0.9		1.0		1.2		1.6	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.4		1.6		1.8		2.2		3.0	ns

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-29 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _c	_{CCI} = 2.25 V, T _J = 70°C)
----------------------------------	---	---

		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	peed –F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Netwo	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Arr	ay Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-37 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_{J} =	: 70°C)
--	---------

		-3 Sp	beed*	-2 S	peed	-1 Speed		Std. Speed		-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-39 A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 2.3 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

		-3 Speed ¹ -2 Speed ·		-1 Speed	Std. 9	Speed	-F Speed			
Parameter	Description	Min. Ma	. Mir	. Max.	Min. Max	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2, 3}									
t _{DLH}	Data-to-Pad Low to High	3.9		4.5	5.1		6.0		8.4	ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.6	4.1		4.8		6.7	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12.	,	14.6	16.5		19.4		27.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8	3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.	3	13.7	15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.9		4.5	5.1		6.0		8.4	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5	2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.6	4.1		4.8		6.7	ns
d_{TLH}^{4}	Delta Low to High	0.03	1	0.037	0.043		0.051		0.071	ns/pF
${\sf d_{THL}}^4$	Delta High to Low	0.01	7	0.017	0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.05	7	0.06	0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-40 A54SX72A Timing Characteristics

(Worst-Case Commercial	Conditions $V_{CCA} = 2.25$	$V_{V_{CCI}} = 3.0$	$I_{1} = 70^{\circ}C$
(.,.,,

		-3 Speed ¹	–2 Spee	ed	–1 Spee	d	Std. 9	td. Speed –F Speed			
Parameter	Description	Min. Max.	Min. M	ax.	Min. Ma	x.	Min.	Max.	Min.	Max.	Units
3.3 V PCI O	utput Module Timing ²		•								
t _{DLH}	Data-to-Pad Low to High	2.3	2	.7	3.	0		3.6		5.0	ns
t _{DHL}	Data-to-Pad High to Low	2.5	2	.9	3.	2		3.8		5.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4	1	.7	1.	9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2	.7	3.	0		3.6		5.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5	2	.8	3.	2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5	2	.9	3.	2		3.8		5.3	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.0)3		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0	015	0.0	15		0.015		0.025	ns/pF
3.3 V LVTTL	Output Module Timing ⁴										
t _{DLH}	Data-to-Pad Low to High	3.2	3	.7	4.	2		5.0		6.9	ns
t _{DHL}	Data-to-Pad High to Low	3.2	3	.7	4.	2		4.9		6.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3	11	1.9	13	.5		15.8		22.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2	2	.6	2.	9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8	18	3.9	21	.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2	3	.7	4.	2		5.0		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9	3	.3	3.	7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2	3	.7	4.	2		4.9		6.9	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.0)3		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0	015	0.0	15		0.015		0.025	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053	0.0)53	0.0	67		0.073		0.107	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 10 pF loading and 25 Ω resistance.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.



	256-Pi	n FBGA		256-Pin FBGA							
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function	Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function				
E11	I/O	I/O	I/O	G16	I/O	I/O	I/O				
E12	I/O	I/O	I/O	H1	I/O	I/O	I/O				
E13	NC	I/O	I/O	H2	I/O	I/O	I/O				
E14	I/O	I/O	I/O	H3	V _{CCA}	V _{CCA}	V _{CCA}				
E15	I/O	I/O	I/O	H4	TRST, I/O	TRST, I/O	TRST, I/O				
E16	I/O	I/O	I/O	H5	I/O	I/O	I/O				
F1	I/O	I/O	I/O	H6	V _{CCI}	V _{CCI}	V _{CCI}				
F2	I/O	I/O	I/O	H7	GND	GND	GND				
F3	I/O	I/O	I/O	H8	GND	GND	GND				
F4	TMS	TMS	TMS	Н9	GND	GND	GND				
F5	I/O	I/O	I/O	H10	GND	GND	GND				
F6	I/O	I/O	I/O	H11	V _{CCI}	V _{CCI}	V _{CCI}				
F7	V _{CCI}	V _{CCI}	V _{CCI}	H12	I/O	I/O	I/O				
F8	V _{CCI}	V _{CCI}	V _{CCI}	H13	I/O	I/O	I/O				
F9	V _{CCI}	V _{CCI}	V _{CCI}	H14	I/O	I/O	I/O				
F10	V _{CCI}	V _{CCI}	V _{CCI}	H15	I/O	I/O	I/O				
F11	I/O	I/O	I/O	H16	NC	I/O	I/O				
F12	VCCA	VCCA	VCCA	J1	NC	I/O	I/O				
F13	I/O	I/O	I/O	J2	NC	I/O	I/O				
F14	I/O	I/O	I/O	J3	NC	I/O	I/O				
F15	I/O	I/O	I/O	J4	I/O	I/O	I/O				
F16	I/O	I/O	I/O	J5	I/O	I/O	I/O				
G1	NC	I/O	I/O	J6	V _{CCI}	V _{CCI}	V _{CCI}				
G2	I/O	I/O	I/O	J7	GND	GND	GND				
G3	NC	I/O	I/O	J8	GND	GND	GND				
G4	I/O	I/O	I/O	J9	GND	GND	GND				
G5	I/O	I/O	I/O	J10	GND	GND	GND				
G6	V _{CCI}	V _{CCI}	V _{CCI}	J11	V _{CCI}	V _{CCI}	V _{CCI}				
G7	GND	GND	GND	J12	I/O	I/O	I/O				
G8	GND	GND	GND	J13	I/O	I/O	I/O				
G9	GND	GND	GND	J14	I/O	I/O	I/O				
G10	GND	GND	GND	J15	I/O	I/O	I/O				
G11	V _{CCI}	V _{CCI}	V _{CCI}	J16	I/O	I/O	I/O				
G12	I/O	I/O	I/O	K1	I/O	I/O	I/O				
G13	GND	GND	GND	K2	I/O	I/O	I/O				
G14	NC	I/O	I/O	К3	NC	I/O	I/O				
G15	V _{CCA}	V _{CCA}	V _{CCA}	K4	V _{CCA}	V _{CCA}	V _{CCA}				

	A	484-Pin FBG	
P Nur	A54SX72A Function	A54SX32A Function	Pin Number
AA	NC	NC*	A1
A	NC	NC*	A2
A	I/O	NC*	A3
A	I/O	NC*	A4
A	I/O	NC*	A5
A	I/O	I/O	A6
A	I/O	I/O	A7
A	I/O	I/O	A8
A	I/O	I/O	A9
A	I/O	I/O	A10
AB	I/O	NC*	A11
AE	I/O	NC*	A12
A	I/O	I/O	A13
AE	NC	NC*	A14
AE	I/O	NC*	A15
AE	I/O	NC*	A16
AE	I/O	I/O	A17
AE	I/O	I/O	A18
AE	I/O	I/O	A19
AB	I/O	I/O	A20
AB	I/O	NC*	A21
A	I/O	NC*	A22
AE	I/O	NC*	A23
AE	I/O	NC*	A24
AE	NC	NC*	A25
AE	NC	NC*	A26
AE	I/O	NC*	AA1
A	I/O	NC*	AA2
A	V _{CCA}	V _{CCA}	AA3
А	I/O	I/O	AA4
A	I/O	I/O	AA5
A	I/O	I/O	AA22
A	I/O	I/O	AA23
A	I/O	I/O	AA24
А	I/O	NC*	AA25

484-Pin FBGA									
Pin Number	A54SX32A Function	A54SX72A Function							
AA26	NC*	I/O							
AB1	NC*	NC							
AB2	V _{CCI}	V _{CCI}							
AB3	I/O	I/O							
AB4	I/O	ΙΟ							
AB5	NC*	ΙΟ							
AB6	I/O	ΙΟ							
AB7	I/O	ΙΟ							
AB8	I/O	I/O							
AB9	I/O	I/O							
AB10	I/O	I/O							
AB11	I/O	I/O							
AB12	PRB, I/O	PRB, I/O							
AB13	V _{CCA}	V _{CCA}							
AB14	I/O	I/O							
AB15	I/O	I/O							
AB16	I/O	I/O							
AB17	I/O	I/O							
AB18	I/O	I/O							
AB19	I/O	I/O							
AB20	TDO, I/O	TDO, I/O							
AB21	GND	GND							
AB22	NC*	I/O							
AB23	I/O	I/O							
AB24	I/O	I/O							
AB25	NC*	I/O							
AB26	NC*	I/O							
AC1	I/O	I/O							
AC2	I/O	I/O							
AC3	I/O	I/O							
AC4	NC*	I/O							
AC5	V _{CCI}	V _{CCI}							
AC6	I/O	I/O							
AC7	V _{CCI}	V _{CCI}							
AC8	I/O	I/O							

484-Pin FBGA									
Pin Number	A54SX32A Function	A54SX72A Function							
AC9	I/O	Ι/O							
AC10	I/O	I/O							
AC11	I/O	I/O							
AC12	I/O	QCLKA							
AC13	I/O	I/O							
AC14	I/O	I/O							
AC15	I/O	I/O							
AC16	I/O	I/O							
AC17	I/O	I/O							
AC18	I/O	I/O							
AC19	I/O	١/O							
AC20	V _{CCI}	V _{CCI}							
AC21	I/O	I/O							
AC22	I/O	I/O							
AC23	NC*	I/O							
AC24	I/O	I/O							
AC25	NC*	I/O							
AC26	NC*	I/O							
AD1	I/O	I/O							
AD2	I/O	I/O							
AD3	GND	GND							
AD4	I/O	I/O							
AD5	I/O	I/O							
AD6	I/O	I/O							
AD7	I/O	I/O							
AD8	I/O	I/O							
AD9	V _{CCI}	V _{CCI}							
AD10	I/O	I/O							
AD11	I/O	I/O							
AD12	I/O	I/O							
AD13	V _{CCI}	V _{CCI}							
AD14	I/O	I/O							
AD15	I/O	I/O							
AD16	I/O	I/O							
AD17	V _{CCI}	V _{CCI}							

Actel°

SX-A Family FPGAs

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA				
Pin Number	A54SX32A Function	A54SX72A Function		
K10	GND	GND		
K11	GND	GND		
K12	GND	GND		
K13	GND	GND		
K14	GND	GND		
K15	GND	GND		
K16	GND	GND		
K17	GND	GND		
K22	I/O	I/O		
K23	I/O	I/O		
K24	NC*	NC		
K25	NC*	I/O		
K26	NC*	I/O		
L1	NC*	I/O		
L2	NC*	I/O		
L3	I/O	I/O		
L4	I/O	I/O		
L5	I/O	I/O		
L10	GND	GND		
L11	GND	GND		
L12	GND	GND		
L13	GND	GND		
L14	GND	GND		
L15	GND	GND		
L16	GND	GND		
L17	GND	GND		
L22	I/O	I/O		
L23	I/O	I/O		
L24	I/O	I/O		
L25	I/O	I/O		
L26	I/O	I/O		
M1	NC*	NC		
M2	I/O	I/O		
M3	I/O	I/O		
M4	I/O	I/O		

484-Pin FBGA				
Pin Number	A54SX32A Function	A54SX72A Function		
M5	I/O	I/O		
M10	GND	GND		
M11	GND	GND		
M12	GND	GND		
M13	GND	GND		
M14	GND	GND		
M15	GND	GND		
M16	GND	GND		
M17	GND	GND		
M22	I/O	I/O		
M23	I/O	I/O		
M24	I/O	I/O		
M25	NC*	I/O		
M26	NC*	I/O		
N1	I/O	I/O		
N2	V _{CCI}	V _{CCI}		
N3	I/O	I/O		
N4	I/O	I/O		
N5	I/O	I/O		
N10	GND	GND		
N11	GND	GND		
N12	GND	GND		
N13	GND	GND		
N14	GND	GND		
N15	GND	GND		
N16	GND	GND		
N17	GND	GND		
N22	V _{CCA}	V _{CCA}		
N23	I/O	I/O		
N24	I/O	I/O		
N25	I/O	I/O		
N26	NC*	NC		
P1	NC*	I/O		
P2	NC*	I/O		
P3	I/O	I/O		

484-Pin FBGA				
Pin Number	A54SX32A Function	A54SX72A Function		
P4	I/O	I/O		
P5	V _{CCA}	V _{CCA}		
P10	GND	GND		
P11	GND	GND		
P12	GND	GND		
P13	GND	GND		
P14	GND	GND		
P15	GND	GND		
P16	GND	GND		
P17	GND	GND		
P22	I/O	I/O		
P23	Ι/O	I/O		
P24	V _{CCI}	V _{CCI}		
P25	I/O	I/O		
P26	I/O	I/O		
R1	NC*	I/O		
R2	NC*	I/O		
R3	I/O	I/O		
R4	I/O	I/O		
R5	TRST, I/O	TRST, I/O		
R10	GND	GND		
R11	GND	GND		
R12	GND	GND		
R13	GND	GND		
R14	GND	GND		
R15	GND	GND		
R16	GND	GND		
R17	GND	GND		
R22	I/O	I/O		
R23	I/O	I/O		
R24	I/O	I/O		
R25	NC*	I/O		
R26	NC*	I/O		
T1	NC*	I/O		
T2	NC*	Ι/O		

Note: *These pins must be left floating on the A54SX32A device.

Actel and the Actel logo are registered trademarks of Actel Corporation. All other trademarks are the property of their owners.



www.actel.com

Actel Corporation

Actel Europe Ltd.

2061 Stierlin Court Mountain View, CA 94043-4655 USA **Phone** 650.318.4200 **Fax** 650.318.4600 River Court, Meadows Business Park Station Approach, Blackwater Camberley, Surrey GU17 9AB United Kingdom Phone +44 (0) 1276 609 300 Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F 1-24-14 Ebisu Shibuya-ku Tokyo 150 Japan Phone +81.03.3445.7671 Fax +81.03.3445.7668 www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place 88 Queensway, Admiralty Hong Kong Phone +852 2185 6460 Fax +852 2185 6488 www.actel.com.cn