Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	171
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-pq208a

Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. *C = Commercial*
2. *I = Industrial*
3. *A = Automotive*
4. *M = Military*
5. *B = MIL-STD-883 Class B*
6. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
7. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Speed Grade and Temperature Grade Matrix

	F	Std	–1	–2	–3
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

Notes:

1. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
2. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Contact your Actel Sales representative for more information on availability.

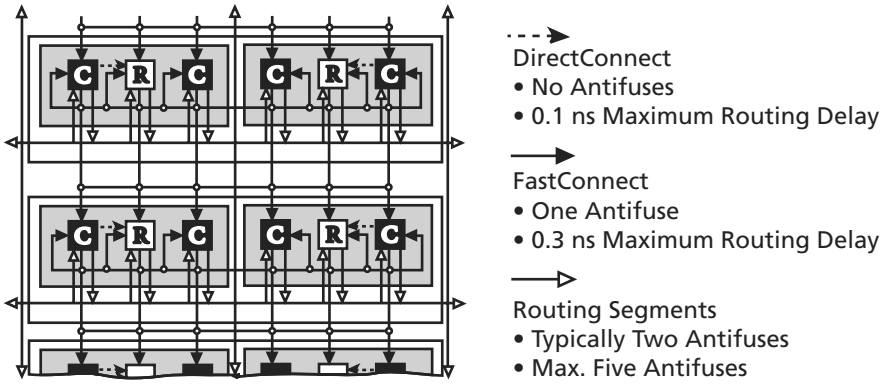

Figure 1-5 • **DirectConnect and FastConnect for Type 1 SuperClusters**

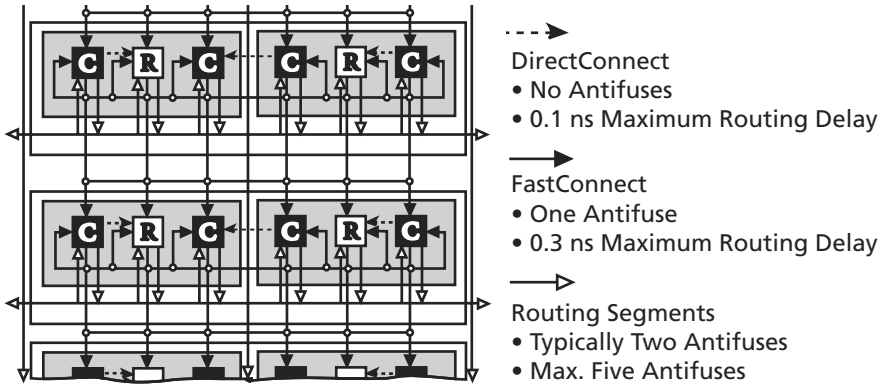

Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selections	• 5 V: PCI, TTL • 3.3 V: PCI, LVTTL • 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	• 5 V: PCI, TTL • 3.3 V: PCI, LVTTL • 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • **I/O Characteristics for All I/O Configurations**

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • **Power-Up Time at which I/Os Become Active**

Supply Ramp Rate	0.25 V/µs	0.025 V/µs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • **Device Configuration Options for Probe Capability (TRST Pin Reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	Low	No	User I/O[3]	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O[3]	User I/O[3]
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

Electrical Specifications

Table 2-5 • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	0.9 V_{CCI}		0.9 V_{CCI}		V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –8 mA)	2.4		2.4		V
V_{OL}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12 mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Table 2-6 • **2.5 V LVCMOS2 Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –100 µA)	2.1		2.1		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	2.0		2.0		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} =–-2 mA)	1.7		1.7		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 100 µA)		0.2		0.2	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • **DC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	5.75	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{IH}	Input High Leakage Current[1]	V_{IN} = 2.7	–	70	µA
I_{IL}	Input Low Leakage Current[1]	V_{IN} = 0.5	–	–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4	–	V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA	–	0.55	V
C_{IN}	Input Pin Capacitance[3]		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Table 2-23 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.6	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.5		2.1	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.4		1.7		2.3	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.7	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-24 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-26 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.0		2.3		2.6		3.1		4.3	ns
t_{DHL}	Data-to-Pad High to Low		2.2		2.5		2.8		3.3		4.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.0		2.3		2.6		3.1		4.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.2		2.5		2.8		3.3		4.6	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.8		3.2		3.6		4.3		6.0	ns
t_{DHL}	Data-to-Pad High to Low		2.7		3.1		3.5		4.1		5.7	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		9.5		10.9		12.4		14.6		20.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		3.2		3.6		4.3		6.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.7		3.1		3.5		4.1		5.7	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-31 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-33 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.4		2.9		4.0	ns
t_{DHL}	Data-to-Pad High to Low		2.0		2.3		2.6		3.1		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.4		2.9		4.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.0		2.3		2.6		3.1		4.3	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.6		3.0		3.4		4.0		5.6	ns
t_{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		9.0		10.4		11.8		13.8		19.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.6		3.0		3.4		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP	
Pin Number	**A54SX32A Function**
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	TMS
11	V_{CCI}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	V_{CCA}
23	GND
24	I/O
25	TRST, I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	V_{CCI}
33	V_{CCA}
34	I/O
35	I/O
36	I/O

176-Pin TQFP	
Pin Number	**A54SX32A Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	GND
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	V_{CCI}
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	PRB, I/O
65	GND
66	V_{CCA}
67	NC
68	I/O
69	HCLK
70	I/O
71	I/O
72	I/O

176-Pin TQFP	
Pin Number	**A54SX32A Function**
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V_{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	TDO, I/O
88	I/O
89	GND
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V_{CCA}
99	V_{CCI}
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	GND

176-Pin TQFP	
Pin Number	**A54SX32A Function**
109	V_{CCA}
110	GND
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	V_{CCA}
123	GND
124	V_{CCI}
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	GND
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	V_{CCI}
141	I/O
142	I/O
143	I/O
144	I/O

144-Pin FBGA

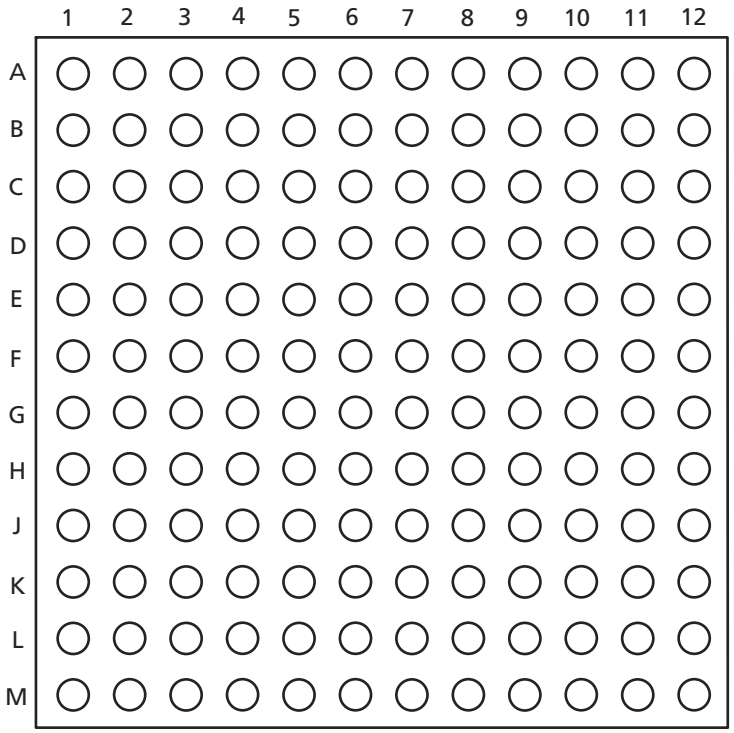

Figure 3-6 • **144-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V_{CCA}	V_{CCA}	V_{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

5172147-10/2.07