E·XFL



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	171
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-pqg208a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Logic Module Design

The SX-A family architecture is described as a "sea-ofmodules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-byregister basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.



Figure 1-2 • R-Cell



Figure 1-3 • C-Cell

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.



Figure 1-4 • Cluster Organization



Figure 1-9 • SX-A QCLK Architecture







Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using $0.22 \,\mu/0.25 \,\mu$ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

For more information, refer to Actel's *Implementation* of Security in Actel Antifuse FPGAs application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pinto-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os.* Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.



Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6	٠	Boundary-Scan Pin Configurations an	d
		Functions	

Mode	Designer "Reserve JTAG" Selection	TAP Controller State		
Dedicated (JTAG)	Checked	Any		
Flexible (User I/O)	Unchecked	Test-Logic-Reset		
Flexible (JTAG)	Unchecked	Any EXCEPT Test- Logic-Reset		

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function						
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)						
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up						
Reserve Probe	Keeps pins from being used or regular I/O						

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 •	JTAG	Instruction	Code
-------------	------	-------------	------

Instructions (IR4:IR0)	Binary Code
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HighZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-8 JTAG Instruction Code

Device	Process	Revision	Bits 31-28	Bits 27-12
A54SX08A	0.22 µ	0	8, 9	40B4, 42B4
		1	А, В	40B4, 42B4
A54SX16A	0.22 µ	0	9	4088, 4288
		1	В	4088, 4288
	0.25 µ	1	В	22B8
A54SX32A	0.2 2µ	0	9	40BD, 42BD
		1	В	40BD, 42BD
	0.25 µ	1	В	22BD
A54SX72A	0.22 µ	0	9	40B2, 42B2
		1	В	40B2, 42B2
	0.25 µ	1	В	22B2

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer builtin programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any userdefined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.



PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	5.75	V
V _{IL}	Input Low Voltage		-0.5	0.8	V
I _{IH}	Input High Leakage Current ¹	V _{IN} = 2.7	-	70	μΑ
IIL	Input Low Leakage Current ¹	V _{IN} = 0.5	-	-70	μΑ
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4	-	V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA	-	0.55	V
C _{IN}	Input Pin Capacitance ³		-	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.

2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.

3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 2-14 A545X08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCA} = 2.25 V$, $V_{CCI} = 3.0 V$, $T_J = 70^{\circ}$ C)

		-2 Speed		–1 Speed		Std. Speed		-F Speed		
Parameter	Description	Min. N	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t _{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Modul	e Predicted Routing Delays ²									
t _{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t _{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-16 A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions	V _{CCA} = 2.25 V, V _{CC}	₁ = 3.0 V, T _J = 70°C)
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		-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lardwired) Array Clock Networks									
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.3		1.5		1.7		2.6	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.1		1.3		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPVVL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.5		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Arra	y Clock Networks									
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.8		0.9		1.1		1.5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		1.9	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.2		1.3		1.6		2.2	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPVVL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.8		0.9		1.1		1.5	ns

Table 2-28 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-3 Sp	beed ¹	-2 S	peed	-1 S	peed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	agation Delays ²											
t _{PD}	Internal Array Module		0.8		0.9		1.1		1.2		1.7	ns
Predicted R	outing Delays ³											
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timin	ng											
t _{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays					-						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.2		1.3		1.5		1.8		2.5	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.6		0.7		0.8		0.9		1.3	ns
t _{INYH}	lnput Data Pad to Y High 3.3 V LVTTL		0.8		0.9		1.0		1.2		1.6	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.4		1.6		1.8		2.2		3.0	ns

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-35 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-3 Sp	beed ¹	-2 S	peed	–1 S	peed	Std. Speed		–F S	peed			
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units		
C-Cell Propagation Delays ²														
t _{PD}	Internal Array Module		1.0		1.1		1.3		1.5		2.0	ns		
Predicted R	outing Delays ³													
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns		
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns		
t _{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns		
t _{RD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns		
t _{RD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns		
t _{RD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns		
t _{RD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns		
t _{RD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		3		4.2	ns
R-Cell Timin	ng													
t _{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.1		1.5	ns		
t _{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.7		0.9		1.2	ns		
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns		
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns		
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns		
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns		
t _{recasyn}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns		
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns		
t _{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns		
Input Modu	le Propagation Delays							-						
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.3	ns		
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		1.0		1.1		1.3		1.7	ns		
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.7		0.7		0.9		1.2	ns		
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns		
t _{INYH}	lnput Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns		
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.2		1.3		1.5		2.1	ns		

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-37 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_{J} =	: 70°C)
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		-3 Sp	beed*	-2 Speed -1 Speed		Speed Std.		Std. Speed		-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-39 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 2.3 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

		-3 Speed	1	-2 S	peed	–1 Speed S		Std. S	Speed	-F Speed		
Parameter	Description	Min. Ma	х.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCM												
t _{DLH}	Data-to-Pad Low to High	3.	9		4.5		5.1		6.0		8.4	ns
t _{DHL}	Data-to-Pad High to Low	3.	1		3.6		4.1		4.8		6.7	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12	.7		14.6		16.5		19.4		27.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.	4		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11	.8		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.	9		4.5		5.1		6.0		8.4	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.	1		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.	1		3.6		4.1		4.8		6.7	ns
d_{TLH}^{4}	Delta Low to High	0.0	31		0.037		0.043		0.051		0.071	ns/pF
d_{THL}^4	Delta High to Low	0.0	17		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.0	57		0.06		0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-40 A54SX72A Timing Characteristics

(Worst-Case Commercial	Conditions $V_{CCA} = 2.25$	$V_{V_{CCI}} = 3.0$	$I_{1} = 70^{\circ}C$
(.,.,,

		-3 Speed ¹	–2 Spee	ed	–1 Spee	ed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min. Max.	Min. M	ax.	Min. M	ax.	Min.	Max.	Min.	Max.	Units
3.3 V PCI O	3.3 V PCI Output Module Timing ²										
t _{DLH}	Data-to-Pad Low to High	2.3	2	.7	3	.0		3.6		5.0	ns
t _{DHL}	Data-to-Pad High to Low	2.5	2	.9	3	.2		3.8		5.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4	1	.7	1	.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2	.7	3	.0		3.6		5.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5	2	.8	3	.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5	2	.9	3	.2		3.8		5.3	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0	015	0.0	015		0.015		0.025	ns/pF
3.3 V LVTTL	Output Module Timing ⁴				•						
t _{DLH}	Data-to-Pad Low to High	3.2	3	.7	4	.2		5.0		6.9	ns
t _{DHL}	Data-to-Pad High to Low	3.2	3	.7	4	.2		4.9		6.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3	11	1.9	13	3.5		15.8		22.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2	2	.6	2	.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8	18	3.9	2	1.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2	3	.7	4	.2		5.0		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9	3	.3	3	.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2	3	.7	4	.2		4.9		6.9	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0)15	0.0	015		0.015		0.025	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053	0.0)53	0.0	067		0.073		0.107	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 10 pF loading and 25 Ω resistance.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.



Package Pin Assignments

208-Pin PQFP



Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

	2	08-Pin PQF	Р		208-Pin PQFP					
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function	Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function	
141	NC	I/O	I/O	I/O	176	NC	I/O	I/O	I/O	
142	I/O	I/O	I/O	I/O	177	I/O	I/O	I/O	I/O	
143	NC	I/O	I/O	I/O	178	I/O	I/O	I/O	QCLKD	
144	I/O	I/O	I/O	I/O	179	I/O	I/O	I/O	I/O	
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}	180	CLKA	CLKA	CLKA	CLKA	
146	GND	GND	GND	GND	181	CLKB	CLKB	CLKB	CLKB	
147	I/O	I/O	I/O	I/O	182	NC	NC	NC	NC	
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}	183	GND	GND	GND	GND	
149	I/O	I/O	I/O	I/O	184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}	
150	I/O	I/O	I/O	I/O	185	GND	GND	GND	GND	
151	I/O	I/O	I/O	I/O	186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O	
152	I/O	I/O	I/O	I/O	187	I/O	I/O	I/O	V _{CCI}	
153	I/O	I/O	I/O	I/O	188	I/O	I/O	I/O	I/O	
154	I/O	I/O	I/O	I/O	189	NC	I/O	I/O	I/O	
155	NC	I/O	I/O	I/O	190	I/O	I/O	I/O	QCLKC	
156	NC	I/O	I/O	I/O	191	I/O	I/O	I/O	I/O	
157	GND	GND	GND	GND	192	NC	I/O	I/O	I/O	
158	I/O	I/O	I/O	I/O	193	I/O	I/O	I/O	I/O	
159	I/O	I/O	I/O	I/O	194	I/O	I/O	I/O	I/O	
160	I/O	I/O	I/O	I/O	195	NC	I/O	I/O	I/O	
161	I/O	I/O	I/O	I/O	196	I/O	I/O	I/O	I/O	
162	I/O	I/O	I/O	I/O	197	I/O	I/O	I/O	I/O	
163	I/O	I/O	I/O	I/O	198	NC	I/O	I/O	I/O	
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}	199	I/O	I/O	I/O	I/O	
165	I/O	I/O	I/O	I/O	200	I/O	I/O	I/O	I/O	
166	I/O	I/O	I/O	I/O	201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}	
167	NC	I/O	I/O	I/O	202	NC	I/O	I/O	I/O	
168	I/O	I/O	I/O	I/O	203	NC	I/O	I/O	I/O	
169	I/O	I/O	I/O	I/O	204	I/O	Ι/O	I/O	I/O	
170	NC	I/O	I/O	I/O	205	NC	I/O	I/O	I/O	
171	I/O	I/O	I/O	I/O	206	I/O	Ι/O	I/O	I/O	
172	I/O	I/O	I/O	I/O	207	I/O	ΙΟ	I/O	I/O	
173	NC	I/O	I/O	I/O	208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O	
174	I/O	I/O	I/O	I/O	<u>L</u>	<u>ı</u>		1	1	
175	I/O	I/O	I/O	I/O						



176-Pin TQFP



Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.



176-Pi	n TQFP
Pin Number	A54SX32A Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V _{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V _{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

329-Pi	n PBGA						
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
D11	V _{CCA}	H1	I/O	L14	GND	P12	GND
D12	NC	H2	I/O	L20	NC	P13	GND
D13	I/O	H3	I/O	L21	I/O	P14	GND
D14	I/O	H4	I/O	L22	I/O	P20	I/O
D15	I/O	H20	V _{CCA}	L23	NC	P21	I/O
D16	I/O	H21	I/O	M1	I/O	P22	I/O
D17	I/O	H22	I/O	M2	I/O	P23	I/O
D18	I/O	H23	I/O	M3	I/O	R1	I/O
D19	I/O	J1	NC	M4	V _{CCA}	R2	I/O
D20	I/O	J2	I/O	M10	GND	R3	I/O
D21	I/O	J3	I/O	M11	GND	R4	I/O
D22	I/O	J4	I/O	M12	GND	R20	I/O
D23	I/O	J20	I/O	M13	GND	R21	I/O
E1	V _{CCI}	J21	I/O	M14	GND	R22	I/O
E2	I/O	J22	I/O	M20	V _{CCA}	R23	I/O
E3	I/O	J23	I/O	M21	I/O	T1	I/O
E4	I/O	K1	I/O	M22	I/O	T2	I/O
E20	I/O	К2	I/O	M23	V _{CCI}	T3	I/O
E21	I/O	К3	I/O	N1	I/O	T4	I/O
E22	I/O	К4	I/O	N2	TRST, I/O	T20	I/O
E23	I/O	K10	GND	N3	I/O	T21	I/O
F1	I/O	K11	GND	N4	I/O	T22	I/O
F2	TMS	K12	GND	N10	GND	T23	I/O
F3	I/O	K13	GND	N11	GND	U1	I/O
F4	I/O	K14	GND	N12	GND	U2	I/O
F20	I/O	K20	I/O	N13	GND	U3	V _{CCA}
F21	I/O	K21	I/O	N14	GND	U4	I/O
F22	I/O	K22	I/O	N20	NC	U20	I/O
F23	I/O	K23	I/O	N21	I/O	U21	V _{CCA}
G1	I/O	L1	I/O	N22	I/O	U22	I/O
G2	I/O	L2	I/O	N23	I/O	U23	I/O
G3	I/O	L3	I/O	P1	I/O	V1	V _{CCI}
G4	I/O	L4	NC	P2	I/O	V2	I/O
G20	I/O	L10	GND	P3	I/O	V3	I/O
G21	I/O	L11	GND	P4	I/O	V4	I/O
G22	I/O	L12	GND	P10	GND	V20	I/O
G23	GND	L13	GND	P11	GND	V21	I/O