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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	171
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx72a-pqg208m

General Description

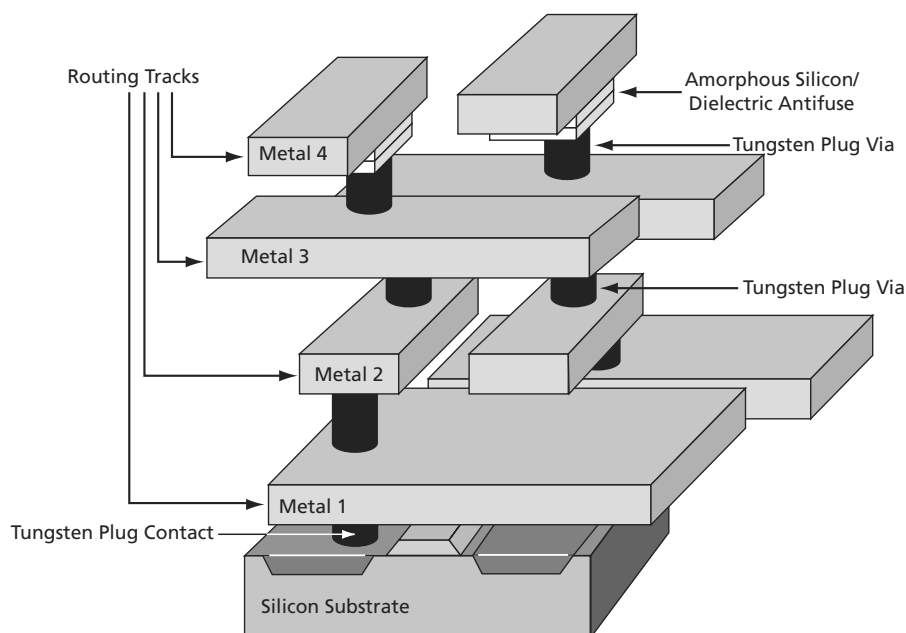
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices and Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • **SX-A Clock Resources**

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

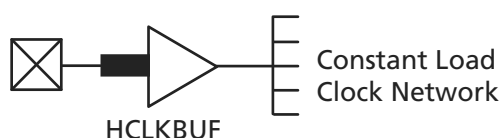


Figure 1-7 • **SX-A HCLK Clock Buffer**

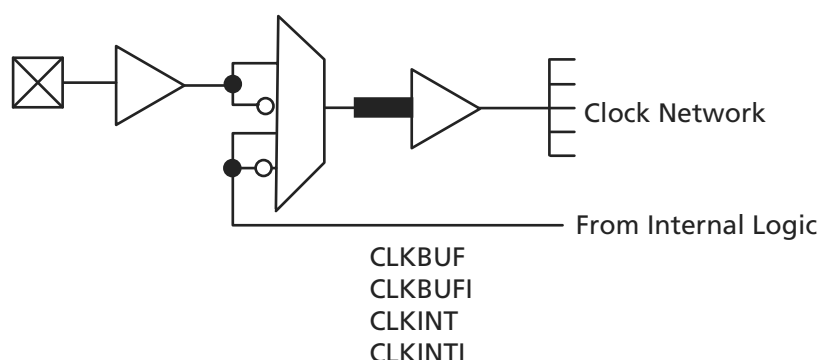


Figure 1-8 • **SX-A Routed Clock Buffer**

Table 2-10 • AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CCI}^1$	$-12V_{CCI}$	–	mA
		$0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}^1$	$(-17.1(V_{CCI} - V_{OUT}))$	–	mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}^{1,2}$	–	EQ 2-3 on page 2-7	–
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$	–	$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \geq 0.6V_{CCI}^1$	$16V_{CCI}$	–	mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^1$	$(26.7V_{OUT})$	–	mA
		$0.18V_{CCI} > V_{OUT} > 0^{1,2}$	–	EQ 2-4 on page 2-7	–
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$	–	$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI} - 0.6V_{CCI}$ load ³	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI} - 0.2V_{CCI}$ load ³	1	4	V/ns

Notes:

1. Refer to the V/I curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.

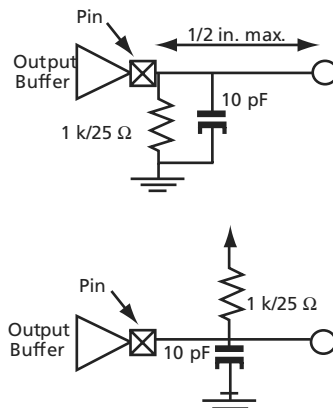


Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

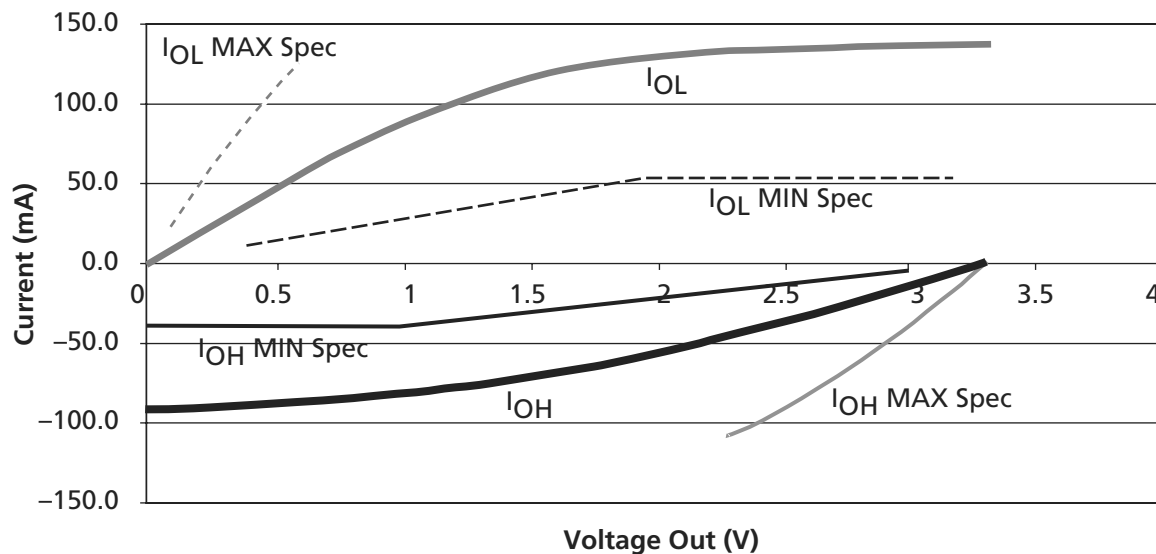


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) = f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX*, *SX-A* and *RT54SX-S* *Power Calculator* worksheet.

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_C = Ambient temperature
- P = total power dissipated by the device

Table 2-12 • Package Thermal Characteristics

Package Type	Pin Count	θ_{JC}	θ_{JA}			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP) ¹	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader ²	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

- The A54SX08A PQ208 has no heat spreader.
- The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

Input Buffer Delays

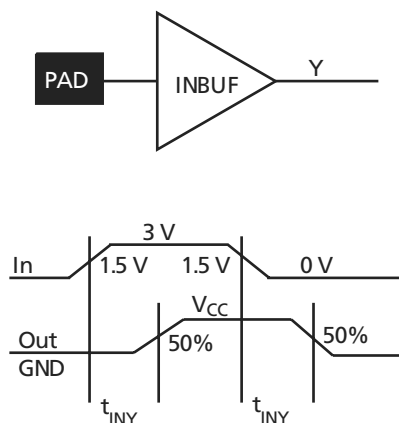


Figure 2-6 • Input Buffer Delays

C-Cell Delays

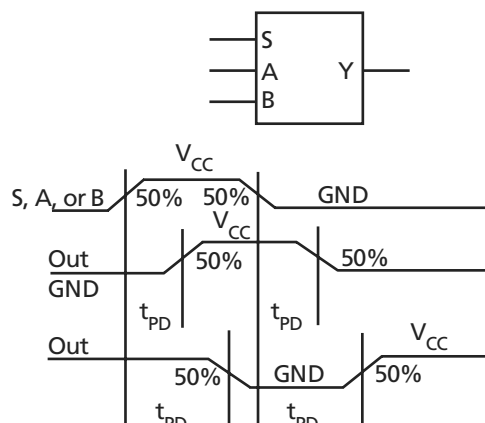


Figure 2-7 • C-Cell Delays

Cell Timing Characteristics

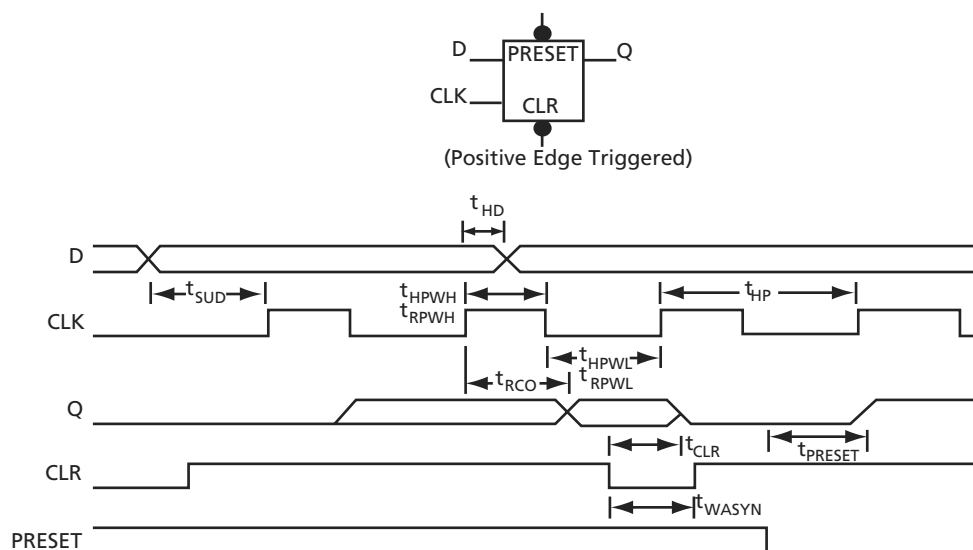


Figure 2-8 • Flip-Flops

Timing Characteristics

Table 2-14 • A54SX08A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.9		1.1		1.2		1.7		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.5		0.6		ns
t _{RD2}	FO = 2 Routing Delay	0.5		0.5		0.6		0.8		ns
t _{RD3}	FO = 3 Routing Delay	0.6		0.7		0.8		1.1		ns
t _{RD4}	FO = 4 Routing Delay	0.8		0.9		1		1.4		ns
t _{RD8}	FO = 8 Routing Delay	1.4		1.5		1.8		2.5		ns
t _{RD12}	FO = 12 Routing Delay	2		2.2		2.6		3.6		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.7		0.8		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.6		0.6		0.8		1.0		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.7		0.9		1.2		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.5		1.8		2.5		ns
t _{RECASYN}	Asynchronous Recovery Time	0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.8		0.9		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	1.0		1.2		1.4		1.9		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.6		0.6		0.7		1.0		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.3		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.7		0.7		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	1.0		1.1		1.3		1.8		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-21 • A54SX16A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	0.9		1.0		1.2		1.4		1.9		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.8		0.9		1		1.4		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2		2.2		2.6		3.6		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.8		1.0		1.4		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.6		1.9		2.7		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.4		1.7		1.9		2.2		3.0		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.5		0.6		0.7		0.8		1.1		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	0.8		0.9		1.0		1.1		1.6		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.0		1.4		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.7		0.7		0.8		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	0.9		1.1		1.2		1.4		2.0		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-26 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.0		2.3		2.6		3.1		4.3		ns
t _{DHL}	Data-to-Pad High to Low	2.2		2.5		2.8		3.3		4.6		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.0		2.3		2.6		3.1		4.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.2		2.5		2.8		3.3		4.6		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.8		3.2		3.6		4.3		6.0		ns
t _{DHL}	Data-to-Pad High to Low	2.7		3.1		3.5		4.1		5.7		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	9.5		10.9		12.4		14.6		20.4		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.8		3.2		3.6		4.3		6.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.7		3.1		3.5		4.1		5.7		ns
d _{TLH} ³	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} ³	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25 Ω resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-27 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6		ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.5		2.8		3.3		4.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9		ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6		ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.7		7.7		8.7		10.2		14.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4		ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-31 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-34 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.1		2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.1		2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9		ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	1.9		2.2		2.5		2.9		4.1		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.3		3.9		5.4		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.6		7.6		8.6		10.1		14.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4		ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-37 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Package Pin Assignments

208-Pin PQFP

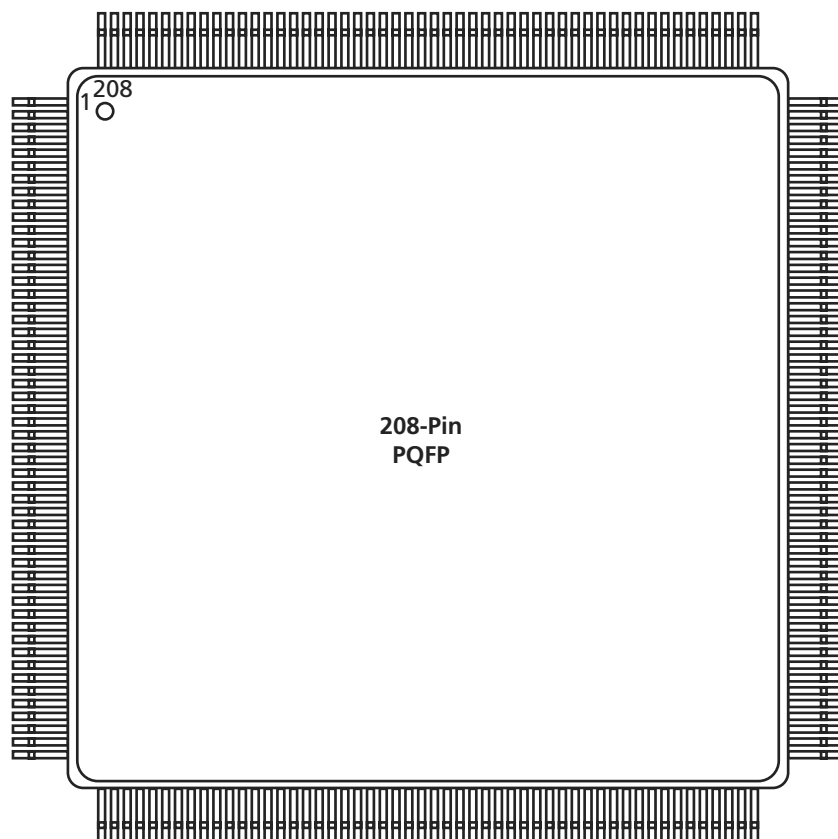


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V _{CCI}	V _{CCI}	V _{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V _{CCI}	V _{CCI}	V _{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V _{CCA}	V _{CCA}	V _{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V _{CCA}	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}	V _{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V _{CCA}	V _{CCA}	V _{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V _{CCA}	V _{CCA}	V _{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

176-Pin TQFP

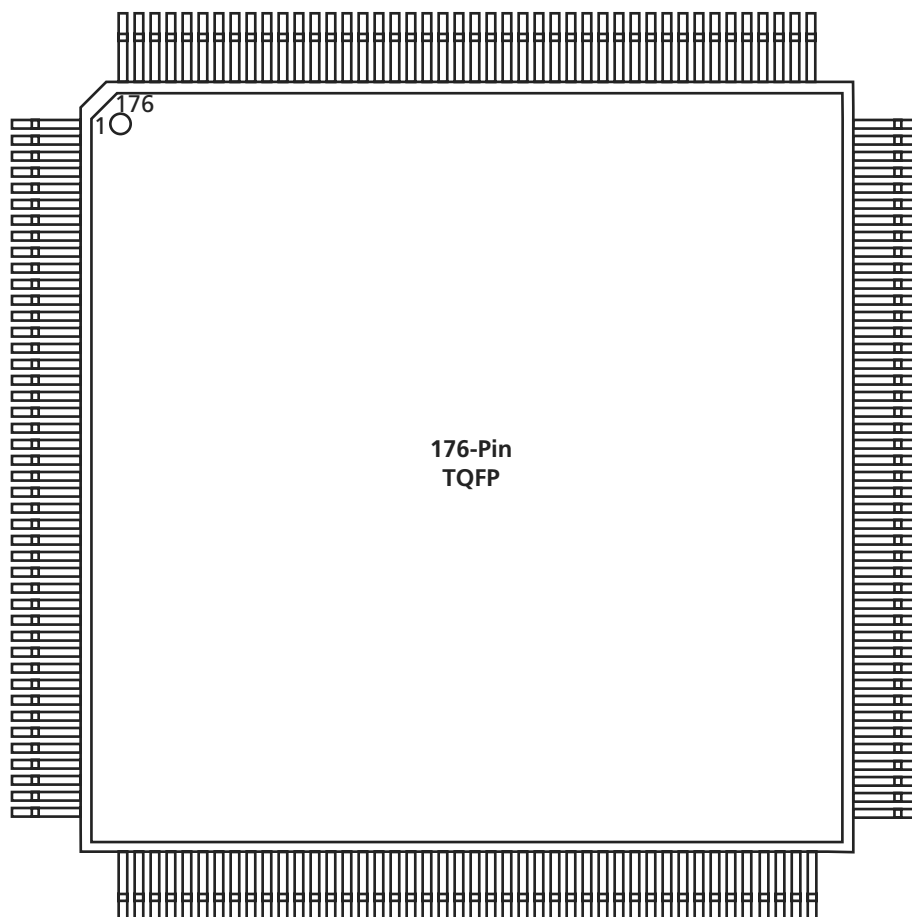


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

