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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	77.4MHz
Connectivity	IrDA, Microwire, SPI, SSP, UART/USART
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh79520n0m000b1

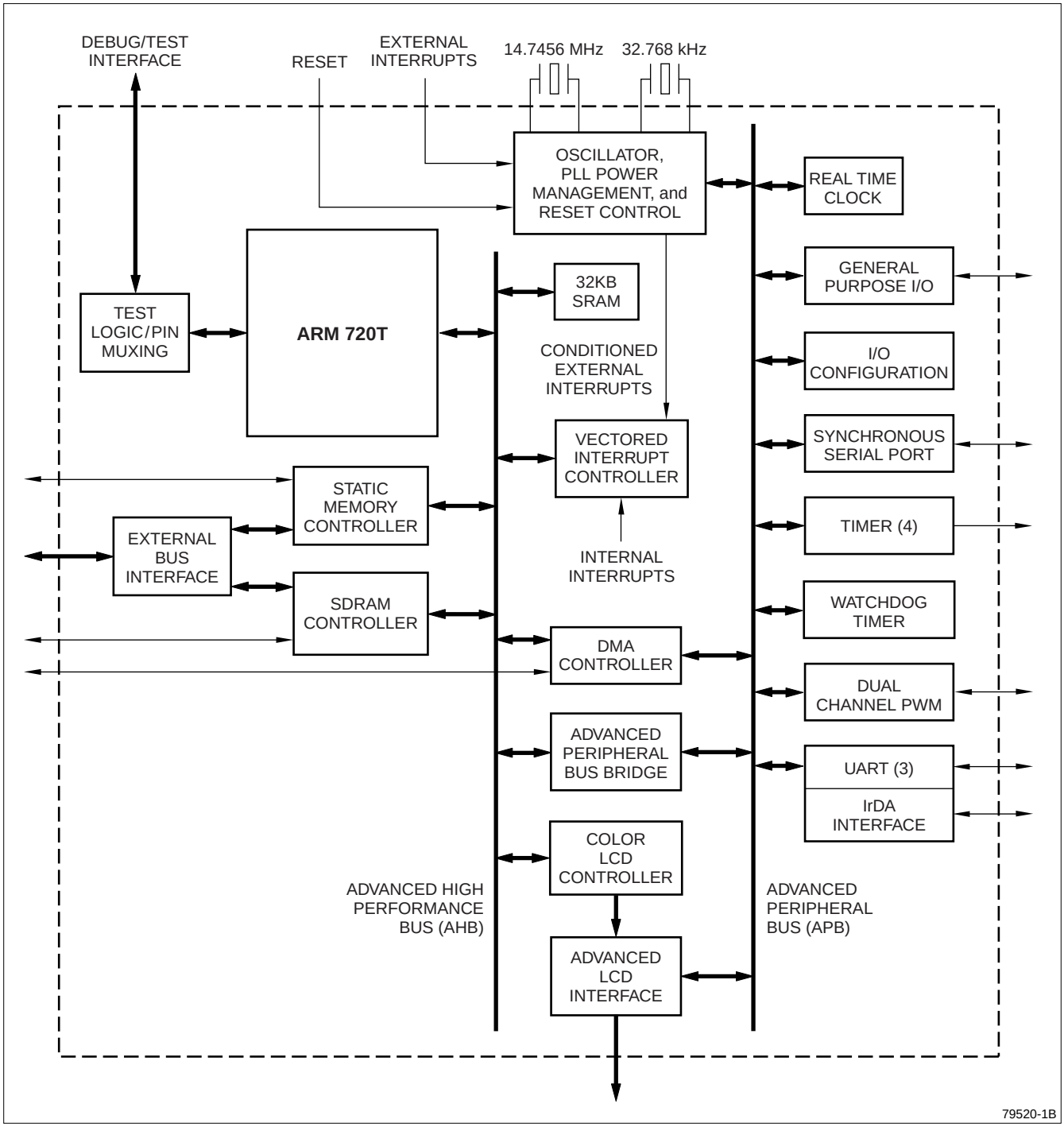


Figure 2. LH79520 Block Diagram

SIGNAL DESCRIPTIONS

Table 1. LH79520 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
2-7 9-12 14-17 19-22 24-27 29-32	A[25:0]	Output	Address Signals	
50-54 56-63 65-66 67-69 71-74 76-79 81-84 86-87	D[31:0]	Input/Output	Data Input/Output Signals	1
101	SDCLK	Output	SDRAM Clock	1
109	DQM3	Output	Data Mask Output to SDRAMs	1
110	DQM2	Output	Data Mask Output to SDRAMs	1
111	DQM1	Output	Data Mask Output to SDRAMs	1
112	DQM0	Output	Data Mask Output to SDRAMs	1
102	SDCKE	Output	SDRAM Clock Enable	1
104	nDCS1	Output	SDRAM Chip Select	1
105	nDCS0	Output	SDRAM Chip Select	1
107	nRAS	Output	Row Address Strobe	
108	nCAS	Output	Column Address Strobe	
106	nSDWE	Output	SDRAM Write Enable	1
41	nCS6	Output	Static Memory Controller Chip Select	1
42	nCS5	Output	Static Memory Controller Chip Select	1
43	nCS4	Output	Static Memory Controller Chip Select	1
44	nCS3	Output	Static Memory Controller Chip Select	1
46	nCS2	Output	Static Memory Controller Chip Select	
47	nCS1	Output	Static Memory Controller Chip Select	
48	nCS0	Output	Static Memory Controller Chip Select	
38	nOE	Output	Static Memory Controller Output Enable	
34	nBLE3	Output	Static Memory Controller Byte Lane Enable / Byte Write Enable	1
35	nBLE2	Output	Static Memory Controller Byte Lane Enable / Byte Write Enable	1
36	nBLE1	Output	Static Memory Controller Byte Lane Enable / Byte Write Enable	
37	nBLE0	Output	Static Memory Controller Byte Lane Enable / Byte Write Enable	
39	nWE	Output	Static Memory Controller Write Enable	
144	nWAIT	Input	Static Memory Controller External Wait Control	1, 3
DMA CONTROLLER (DMAC)				
148	DEOT0	Output	DMA 0 End of Transfer	1
147	nDACK0	Output	DMA 0 Acknowledge	1
146	DREQ0	Input	DMA 0 Request	1
157	DEOT1	Output	DMA 1 End of Transfer	1
145	DACK1	Output	DMA 1 Acknowledge	1
144	DREQ1	Input	DMA 1 Request	1, 3

Table 1. LH79520 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
POWER AND GROUND (GND)				
40 75 95 113 136 154	VDDC	Power	Core Power Supply	
45 120 138 158	VSSC	Ground	Core GND	
8 18 28 49 64 85 100 125 143 161	VDD	Power	Input/Output Power Supply	
13 23 33 55 70 80 103 128 149 168	VSS	Ground	Input/Output GND	
91	VDDA	Power	Analog Power Supply for PLLs and XTAL Oscillators	
92	VSSA	Ground	Analog GND for PLLs and XTAL Oscillators	

1. These pin numbers have multiplexed functions.
2. Signals preceded by 'n' are Active LOW.
3. Immediately after reset, pin 144 can be programmed to function as INT5, DREQ1 or both. Software should avoid enabling both of these functions simultaneously. Pin 144 can also be programmed to function as nWAIT, rendering the INT5/DREQ1 choice unavailable.

NUMERCIAL PIN LIST

Table 2. LH79520 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	TYPE[5]	OUTPUT DRIVE[7]	NOTES
1	nTSTA			Input	None	1
2	A25			Output	8 mA	
3	A24			Output	8 mA	
4	A23			Output	8 mA	
5	A22			Output	8 mA	
6	A21			Output	8 mA	
7	A20			Output	8 mA	
8	VDD			Power	None	
9	A19			Output	8 mA	
10	A18			Output	8 mA	
11	A17			Output	8 mA	
12	A16			Output	8 mA	
13	VSS			Ground	None	
14	A15			Output	8 mA	
15	A14			Output	8 mA	
16	A13			Output	8 mA	
17	A12			Output	8 mA	
18	VDD			Power	None	
19	A11			Output	8 mA	
20	A10			Output	8 mA	
21	A9			Output	8 mA	
22	A8			Output	8 mA	
23	VSS			Ground	None	
24	A7			Output	8 mA	
25	A6			Output	8 mA	
26	A5			Output	8 mA	
27	A4			Output	8 mA	
28	VDD			Power	None	
29	A3			Output	8 mA	
30	A2			Output	8 mA	
31	A1			Output	8 mA	
32	A0			Output	8 mA	
33	VSS			Ground	None	
34	PH7	nBLE3		I/O	8 mA	
35	PH6	nBLE2		I/O	8 mA	
36	nBLE1			Output	8 mA	
37	nBLE0			Output	8 mA	
38	nOE			Output	8 mA	

Table 2. LH79520 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	TYPE[5]	OUTPUT DRIVE[7]	NOTES
39	nWE			Output	8 mA	
40	VDDC			Power	None	
41	PH5	nCS6		I/O	8 mA	
42	PH4	nCS5		I/O	8 mA	
43	PH3	nCS4		I/O	8 mA	
44	PH2	nCS3		I/O	8 mA	
45	VSSC			Ground	None	
46	nCS2			Output	8 mA	
47	nCS1			Output	8 mA	
48	nCS0			Output	8 mA	
49	VDD			Power	None	
50	PH1	D31		I/O	8 mA	
51	PH0	D30		I/O	8 mA	
52	PG7	D29		I/O	8 mA	
53	PG6	D28		I/O	8 mA	
54	PG5	D27		I/O	8 mA	
55	VSS			Ground	None	
56	PG4	D26		I/O	8 mA	
57	PG3	D25		I/O	8 mA	
58	PG2	D24		I/O	8 mA	
59	PG1	D23		I/O	8 mA	
60	PG0	D22		I/O	8 mA	
61	PF7	D21		I/O	8 mA	
62	PF6	D20		I/O	8 mA	
63	PF5	D19		I/O	8 mA	
64	VDD			Power	None	
65	PF4	D18		I/O	8 mA	
66	PF3	D17		I/O	8 mA	
67	PF2	D16		I/O	8 mA	
68	D15			I/O	8 mA	
69	D14			I/O	8 mA	
70	VSS			Ground	None	
71	D13			I/O	8 mA	
72	D12			I/O	8 mA	
73	D11			I/O	8 mA	
74	D10			I/O	8 mA	
75	VDDC			Power	None	
76	D9			I/O	8 mA	
77	D8			I/O	8 mA	

Table 2. LH79520 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	TYPE[5]	OUTPUT DRIVE[7]	NOTES
117	PD6	LCDVD8		I/O	8 mA	
118	PD5	LCDVD7		I/O	8 mA	
119	PD4	LCDVD6	LCDPS	I/O	8 mA	
120	VSSC			Ground	None	
121	PD3	LCDVD5		I/O	8 mA	
122	PD2	LCDVD4		I/O	8 mA	
123	PD1	LCDVD3		I/O	8 mA	
124	PD0	LCDVD2		I/O	8 mA	
125	VDD			Power	None	
126	LCDVD1			Output	8 mA	
127	LCDVD0			Output	8 mA	
128	VSS			Ground	None	
129	PC7	LCDFP	LCDSPS	I/O	8 mA	
130	PC6	LCDVD17		I/O	8 mA	
131	PC5	LCDLP		I/O	8 mA	
132	PC4	LCDVD16		I/O	8 mA	
133	PC3	LCDDCLK		I/O	8 mA	
134	PC2	LCDDCLKIN		I/O	2 mA	
135	PC1	LCDVDDEN	LCDCLS	I/O	8 mA	
136	VDDC			Power	None	
137	PC0	LCDENAB	LCDSPL	I/O	8 mA	
138	VSSC			Ground	None	
139	PB7	LCDVD15	LCDDSPLEN	I/O	8 mA	
140	PB6	LCDVD14		I/O	8 mA	
141	PB5	LCDVD13		I/O	8 mA	
142	PB4	LCDVD12	LCDREV	I/O	8 mA	
143	VDD			Power	None	
144	INT5/DREQ1	nWAIT		Input	None	4, 6
145	CTOUT1B	DACK1		Output	4 mA	
146	PB3	DREQ0		I/O	2 mA	4
147	PB2	nDACK0		I/O	4 mA	
148	PB1	DEOT0		I/O	4 mA	
149	VSS			Ground	None	
150	INT4	PWM0		I/O	4 mA	4
151	INT3	PWMSYNC0		Input	None	4
152	PB0	INT2		I/O	2 mA	4
153	PA7	INT1		I/O	2 mA	4
154	VDDC			Power	None	
155	PA6	INT0		I/O	2 mA	4

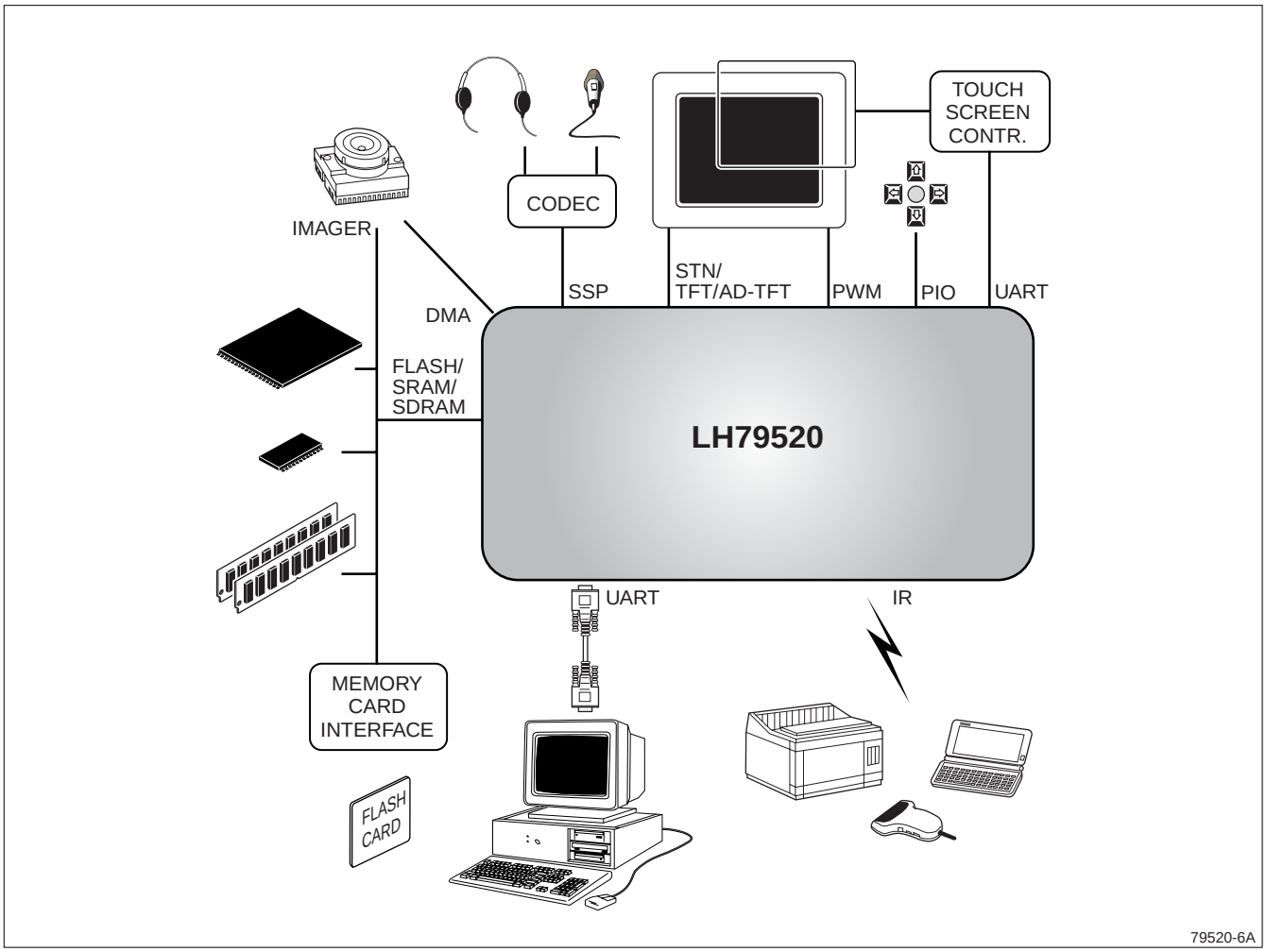


Figure 3. LH79520 Application Diagram Example

SYSTEM DESCRIPTIONS

ARM720T Processor

The LH79520 microcontroller features the ARM720T cached core with an Advanced High-Performance Bus (AHB) interface. The ARM720T features:

- 32-bit ARM7TDMI™ RISC Core
- 8KB Cache
- MMU (Windows CE enabled)

The processor is a member of the ARM7T family of processors. For more information, see the ARM document, 'ARM720T (Rev 3) Technical Reference Manual', available on Sharp's website at www.sharpsma.com.

The LH79520 MMU provides a means to map Physical Memory (PA) addresses to virtual memory addresses. This allows physical memory, which is constrained by hardware to specific addresses, to be reorganized at addresses identified by the user. These user identified locations are called Virtual Addresses (VA). When the MMU is enabled, Code and Data must be built, loaded, and executed using Virtual Addresses which the MMU translates to Physical Addresses. In addition, the user may implement a memory protection scheme by using the features of the MMU. Address translation and memory protection services provided by the MMU are controlled by the user. The MMU is directly controlled through the System Control Coprocessor, Coprocessor 15 (CP15). The MMU is indirectly controlled by a Translation Table (TT) and Page Tables (PT) prepared by the user and established using a portion of physical memory dedicated by the user to storing the TT and PT's.

Memory Architecture

An integrated SDRAM Controller and Static Memory Controller provide a glueless interface to external SDRAM, Flash, SRAM, ROM, and burst ROM. Three remap options for the physical memory are selectable by software, as shown in Figures 4, 5, and 6. Memory is exclusively Little Endian.

SDRAM CONTROLLER

The SDRAM Controller provides the interface between the internal bus and external (off-chip) SDRAM memory devices (Figure 2).

The SDRAM Controller provides the following features:

- Two independently controlled chip selects.
- Transfers data between the controller and SDRAM in quad-word bursts.
- Supports both 32-bit and 16-bit SDRAM.
- Supports 2K, 4K, and 8K row address memory parts, i.e. typical 256M, 128M, 64M, and 16M parts, with 8, 16, or 32 DQ bits per device.
- Two reset domains allow SDRAM contents to be preserved over a soft reset.

STATIC MEMORY CONTROLLER (SMC)

The SMC provides the interface between the internal bus and external (off-chip) memory devices.

The LH79520 boots from 16-bit memory. The SMC address space is divided into eight memory banks of 64MB each. The SMC supports:

- Static Memory-mapped Devices including RAM, ROM, Flash, and Burst ROM
- Asynchronous Operations:
  - Page Mode Reads for non-clocked memory
  - Burst Mode Reads for burst mode ROM
- 8-, 16-, and 32-bit wide external memory data paths
- Independent configuration for up to eight memory banks, each up to 64MB
- Programmable Parameters:
  - WAIT States (up to 32)
  - Bus Turnaround Cycles (1 to 16)
  - Initial and Subsequent Burst Read WAIT State for Burst ROM Devices.

The Static Memory Controller (SMC) also supports an nWAIT input that can be used by an external device to vary the wait time.

DMA Controller

The DMA Controller provides support for DMA-capable peripherals. The LCD controller uses its own DMA port, connecting directly to memory for retrieving display data.

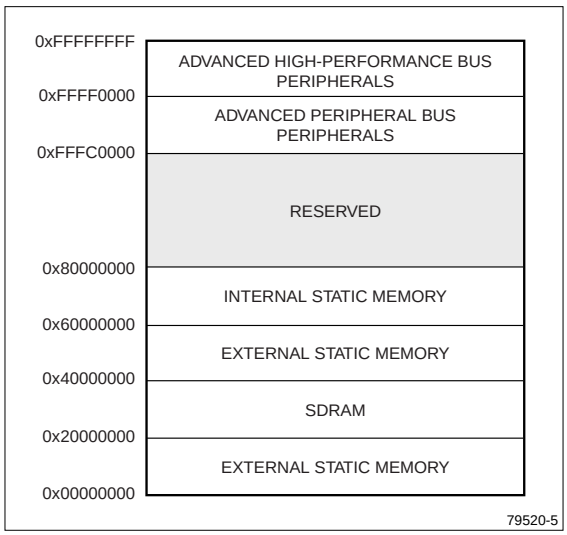


Figure 4. Memory Remap '00' and '11'

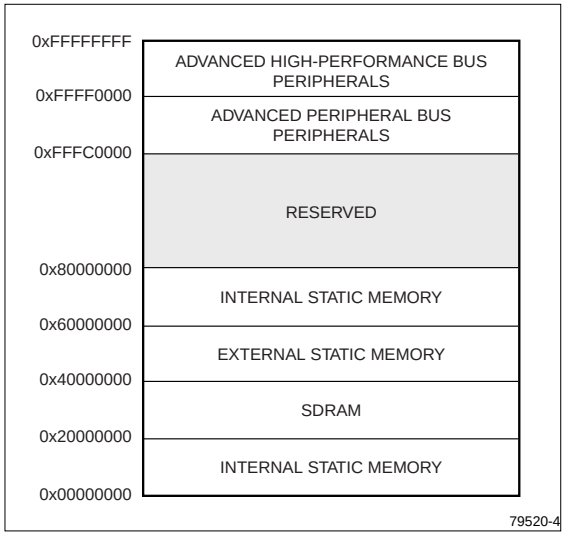


Figure 5. Memory Remap '10'

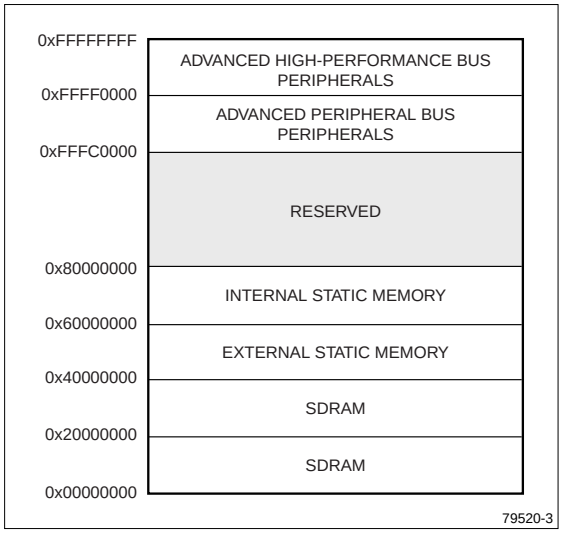


Figure 6. Memory Remap '01'

- Simultaneous servicing of up to 4 data streams
- Three transfer modes are supported:
  - Memory to Memory
  - Peripheral to Memory
  - Memory to Peripheral
- Identical source and destination capabilities
- Transfer Size Programmable (Byte, Half-word, Word)
- Burst Size Programmable
- Address Increment or Address Freeze
- Transfer Error indication for each stream via an interrupt
- 16-word FIFO array with pack and unpack logic

Handles all combinations of byte, half-word or word transfers from input to output.

Color LCD Controller (CLCDC)

The CLCDC provides all the necessary control and drive signals to interface directly with a variety of color and monochrome LCD panels.

- Supports single and dual scan color and monochrome Super Twisted Nematic (STN) displays with 4- or 8-bit interfaces
- Supports Thin Film Transistor (TFT) color displays
- Programmable resolution up to 800 × 600
  - 800 × 600 (16-bit color can only be supported at ≤ 65 Hz refresh rates with 800 × 600 resolution).
- 15 gray-level mono, 3,375 color STN, and 64 k color TFT support
- 1, 2, or 4 bits-per-pixel (BPP) for monochrome STN
- 1-, 2-, 4-, or 8-BPP palettized color displays for color STN and TFT
- True-color non-palettized, for color STN and TFT
- Programmable timing for different display panels
- 256-entry, 16-bit palette fast-access RAM
- Frame, line and pixel clock signals
- AC bias signal for STN or data enable signal for TFT panels
- Patented grayscale algorithm
- Interrupt Generation Events
- Dual 16-deep programmable 32-bit wide FIFOs for buffering incoming data.

ADVANCED LCD INTERFACE

The Advanced LCD Interface peripheral allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The Advanced LCD Interface peripheral also provides a bypass mode that allows the LH79520 to interface to the built-in timing ASIC in standard TFT and STN panels.

Synchronous Serial Port (SSP)

The SSP is a master-only interface for synchronous serial communication with slave peripheral devices that support protocols for Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Interface.

- Master-only operation
- Programmable clock rate
- Separate transmit FIFO and receive FIFO buffers, 16 bits wide, 8 locations deep
- DMA for transmit and receive
- Programmable interface protocols: Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Port
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts
- Available internal loopback test mode.

Universal Asynchronous Receiver Transmitter (UART)

The LH79520 incorporates three UARTs.

- Programmable use of UART0 or IrDA SIR input/output
- Separate 16-byte transmit and receive FIFOs to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Independent masking of transmit FIFO, receive FIFO, receive timeout and modem status interrupts
- False start bit detection
- Line Break generation and detection
- Fully-programmable serial interface characteristics:
  - 5-, 6-, 7-, or 8-bit data word length
  - Even-, odd- or no-parity bit generation and detection
  - 1 or 2 stop bit generation
- IrDA SIR Encode/Decode block, providing:
  - Programmable use of IrDA SIR or UART0 input/output
  - Supports data rates up to 115.2 Kbps half-duplex
  - Programmable internal clock generator, allowing division of the Reference clock in increments of 1 to 512 for low-power mode bit durations.

VARIATIONS FROM THE 16C550 UART

The UART varies from the industry-standard 16C550 UART device in six ways:

- Receive FIFO trigger levels are fixed at 8 bytes
- Receive errors are stored in the FIFO, and do not generate an interrupt.
- The internal register map address space and each register's bit function differ.

The following 16C550 UART features are not supported:

- 1.5 stop bits (1 or 2 stop bits only are supported)
- The forcing stick parity function
- Independent receive clock.

Pulse Width Modulator (PWM)

- Two independent output channels with separate input clocks
- Up to 16-bit resolution
- Programmable synchronous mode support
  - Allows external input to start PWM
- Programmable pulse width (duty cycle), interval (frequency), and polarity
  - Static programming: PWM is stopped
  - Dynamic programming: PWM is running
  - Updates duty cycle, frequency, and polarity at the end of a PWM cycle
  - Wide programming range.

Vectored Interrupt Controller

The Vectored Interrupt Controller combines the interrupt request signals from 20 internal and eight external interrupt sources and applies them, after masking and prioritization, to the IRQ and FIQ interrupt inputs of the ARM7TDMI processor core.

The Interrupt Controller incorporates a hardware interrupt vector logic with programmable priority for up to 16 interrupt sources. This logic reduces the interrupt response time for IRQ type interrupts compared to solutions using software polling to determine the highest priority interrupt source. This significantly improves the real-time capabilities of the LH79520 in embedded control applications.

- 20 internal and eight external interrupt sources
  - Individually maskable
  - Status accessible for software polling
- IRQ interrupt vector logic for up to 16 channels with programmable priorities
- All of the interrupt channels, with the exception of the Watchdog Timer interrupt, can be programmed to generate:
  - FIQ interrupt request
  - Non-vectored IRQ interrupt request (software to poll IRQ source)
  - Vectored IRQ interrupt request (up to 16 channels total)
- The Watchdog timer can only generate FIQ interrupt requests
- External interrupt inputs programmable
  - Edge triggered or level triggered
  - Rising edge/active HIGH or falling edge/active LOW

The 28 interrupt channels are shown in Table 4.

Table 4. Interrupt Channels

CHANNEL	INTERRUPT SOURCE
0	External Interrupt 0
1	External Interrupt 1
2	External Interrupt 2
3	External Interrupt 3
4	External Interrupt 4
5	External Interrupt 5
6	External Interrupt 6
7	External Interrupt 7
8	Spare Internal Interrupt 0
9	COMRX (used for debug)
10	COMTX (used for debug)
11	SSP RX time-out interrupt SSPRXTO
12	CLCD Combined Interrupt
13	SSP SSPTXINTR
14	SSP SSPRXINTR
15	SSP SSPRORINTR
16	SSP SSPINTR
17	Counter/Timer0
18	Counter/Timer1
19	Counter/Timer2
20	Counter/Timer3
21	UART ch0 Rx
22	UART ch0 Tx
23	UART ch0
24	UART ch1
25	UART ch2
26	DMA Combined
27-29	Unused
30	RTC_ALARM
31	WDT

Reset, Clock, and Power Controller (RCPC)

The RCPC generates the various clock signals for the operation of the LH79520 and provides for an orderly start-up after power-on and during a wake-up from one of the power saving operating modes. The RCPC allows the software to individually select the frequency of the various on-chip clock signals as required to operate the chip in the most power-efficient mode. It features:

- 14.7456 MHz crystal oscillator and PLL for on-chip Clock generation
- External Clock input if on-chip oscillator and PLL are not used
- 32.768 kHz crystal oscillator generating 1 Hz clock for Real Time Clock
- Individually controlled clocks for peripherals and CPU
- Clock source for UARTs is selectable between 14.7456 MHz crystal oscillator and external clock source
- Programmable clock prescalers for UARTs and PWMs
- Five global power control modes are available:
  - Active
  - Standby
  - Sleep
  - Stop1
  - Stop2
- CPU and Bus clock frequency can be changed on the fly
- Selectable clock output
- Hardware reset (nRESETIN) and software reset.

Table 5. Clock and Enable States for Different Power Modes (Using On-chip Oscillator and PLL)

FUNCTION	ACTIVE	STANDBY	SLEEP	STOP1	STOP2
14.7456 MHz Oscillator	ON	ON	ON	ON	OFF
PLL	ON	ON	ON	OFF	OFF
Peripheral Clock	ON	ON	OFF	OFF	OFF
CPU Clock	ON	OFF	OFF	OFF	OFF

AC Specifications

All signals described in Table 6 relate to transitions after a reference clock signal. The illustration in Figure 7 represents all cases of these sets of measurement parameters; except for the Asynchronous Memory Interface — which are referenced to Address Valid.

The reference clock signals in this design are:

- HCLK, the System Bus clock
- PCLK, the Peripheral Bus clock (locked to HCLK in the LH79520)
- SSPCLK, the Synchronous Serial Interface clock
- UARTCLK, the UART Interface clock
- LCDDCLK, the LCD Data clock from the LCD Controller
- and SDCLK, the SDRAM clock.

All signal transitions are measured from the 50% point of the clock to the 50% point of the signal. See Figure 7.

For outputs from the LH79520, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from the rising edge of the reference clock signal. Maximum requirements for tOVXXX are shown in Table 6.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output will be held valid from the rising edge of the reference clock signal. Minimum requirements for tOHXXX are listed in Table 6.

For Inputs, tISXXX (e.g. tISD) represents the amount of time the input signal must be valid before the rising edge of the clock signal. Minimum requirements for tISXXX are shown in Table 6.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid from the rising edge of the reference clock signal. Minimum requirements are shown in Table 6.

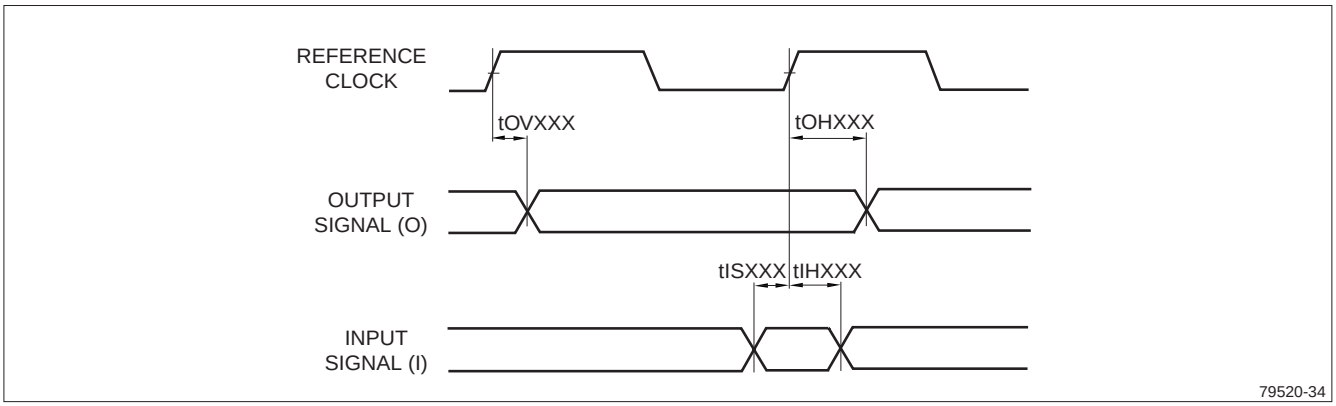


Figure 7. LH79520 Signal Timing

Table 7. AC Signal Characteristics (Cont'd)(Industrial)

SIGNAL	TYPE	LOAD	DRIVE	SYMBOL	MIN.	MAX.	DESCRIPTION
SYNCHRONOUS SERIAL PORT (SSP)							
SSPFRM	Output	50 pF	2 mA	tOVSSPFRM		14 ns	tOVSSPFRM Output Valid, Referenced to SSPCLK
SSPENB	Output	50 pF	2 mA	tOVSSPENB		14ns	tOVSSPENB Output Valid, Referenced to SSPCLK
SSPTX	Output	50 pF	2 mA	tOVSSPOUT		14ns	SSP Transmit Valid
SSPRX	Input			tISSSPIN	17 ns		SSP Receive Setup
INTERRUPTS							
INTR[5:0]	Input						Note 1

NOTES:

1. INTR[5:0] are asynchronous signals. Interrupts must be held Active until serviced in Level Sensitive Mode, and held Active for a minimum of 20 ns in Edge Sensitive Mode.
2. DACK0, nDACK1 and DREQ[1:0] are asynchronous signals. They must be held Active until serviced, for a minimum of 20 ns.

EXTERNAL CLOCKS

Table 8. External Clocks AC Specifications

SYMBOL	DESCRIPTION	MIN.	UNIT
tCLKIN	CLKIN Period	6.66	ns
tCLKINH	CLKIN HIGH Time	2.8	ns
tCLKINL	CLKIN LOW TIme	2.8	ns
tSSPCLK	SSPCLK Period	1	PCLK
tSSPCLKH	SSPCLK HIGH Time	0.4	PCLK
tSSPCLKL	SSPCLK LOW Time	0.4	PCLK
tUCLK	UCLK	1	PCLK
tUCLKH	UCLK HIGH Time	0.4	PCLK
tUCLKL	UCLK LOW Time	0.4	PCLK

NOTES:
1. PCLK is the period chosen for the internal peripheral clock domain.
2. MAX. period is DC. See ‘Recommended Operating Conditions’.

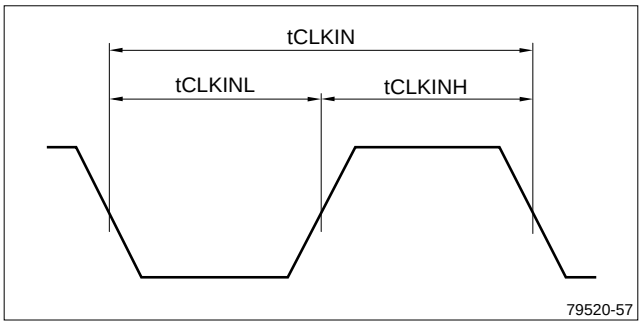


Figure 8. External Clock AC Timing

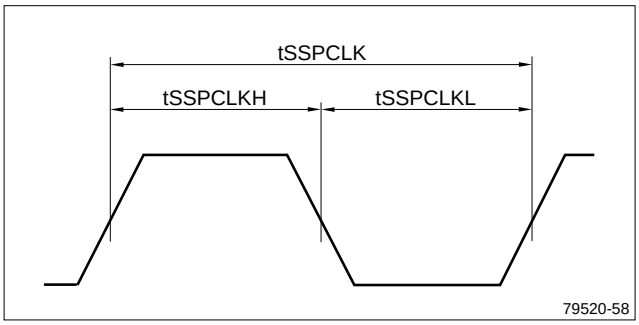


Figure 9. Synchronous Serial I/F Clocks AC Timing

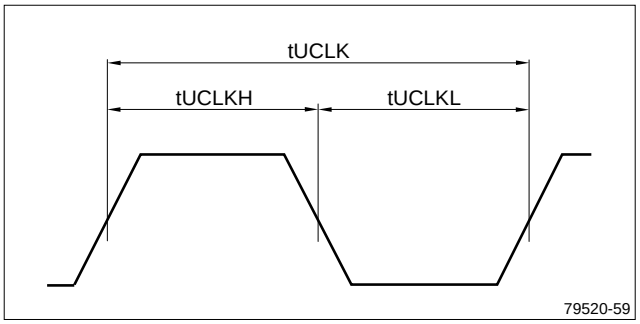


Figure 10. External UARTs/SIR Clock AC Timing

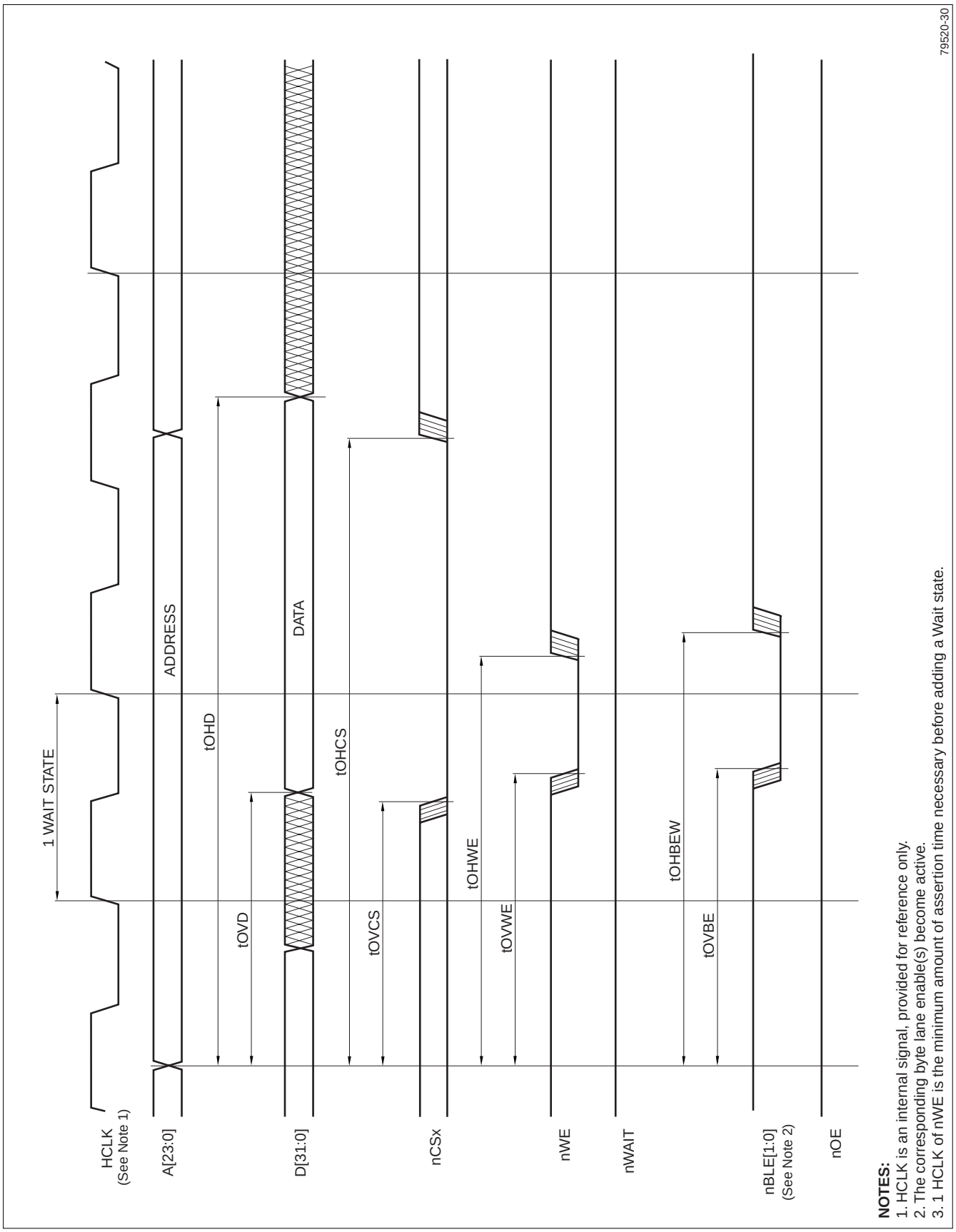


Figure 12. External Static Memory Write, One Wait State

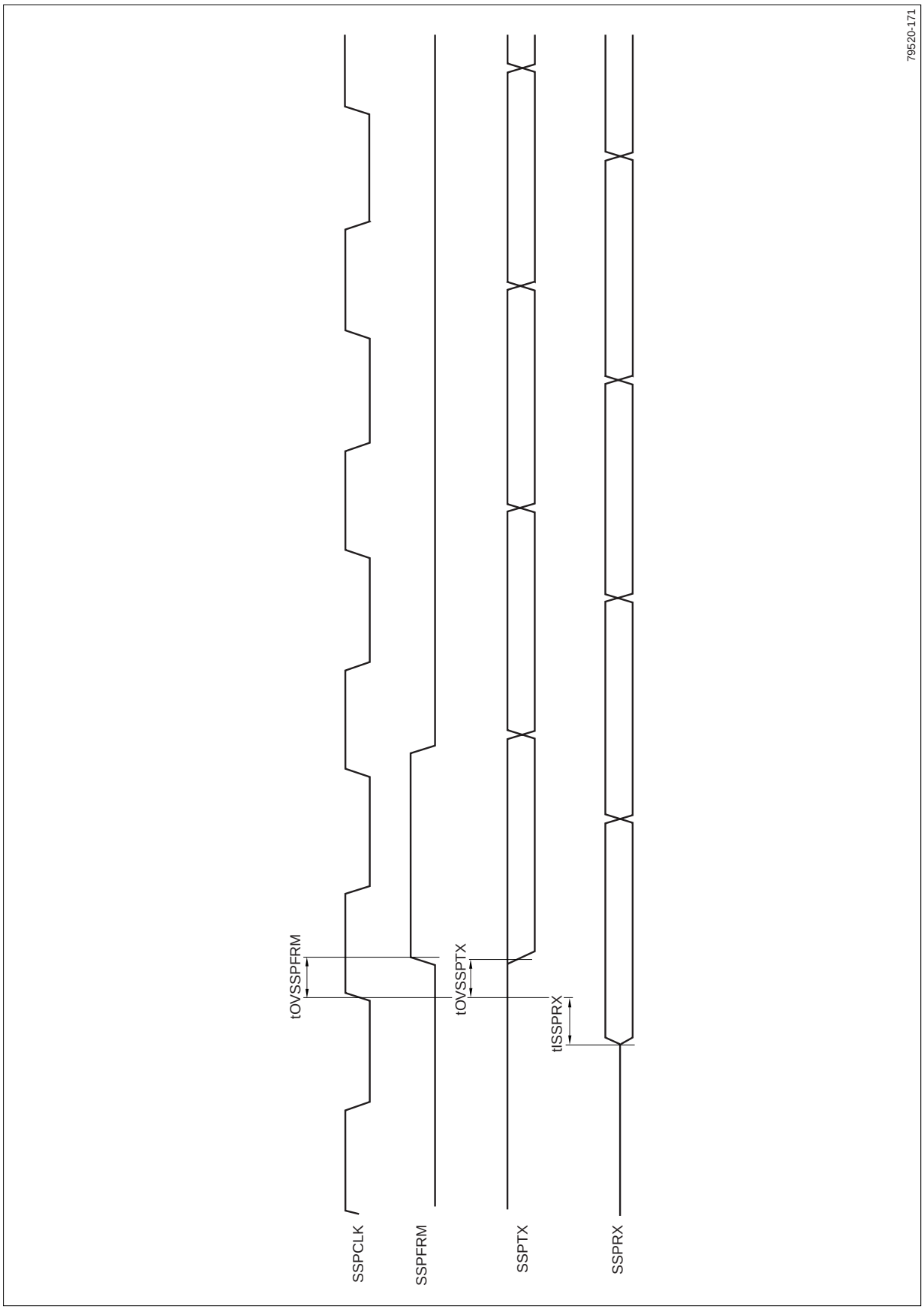


Figure 15. Synchronous Serial Port Waveform

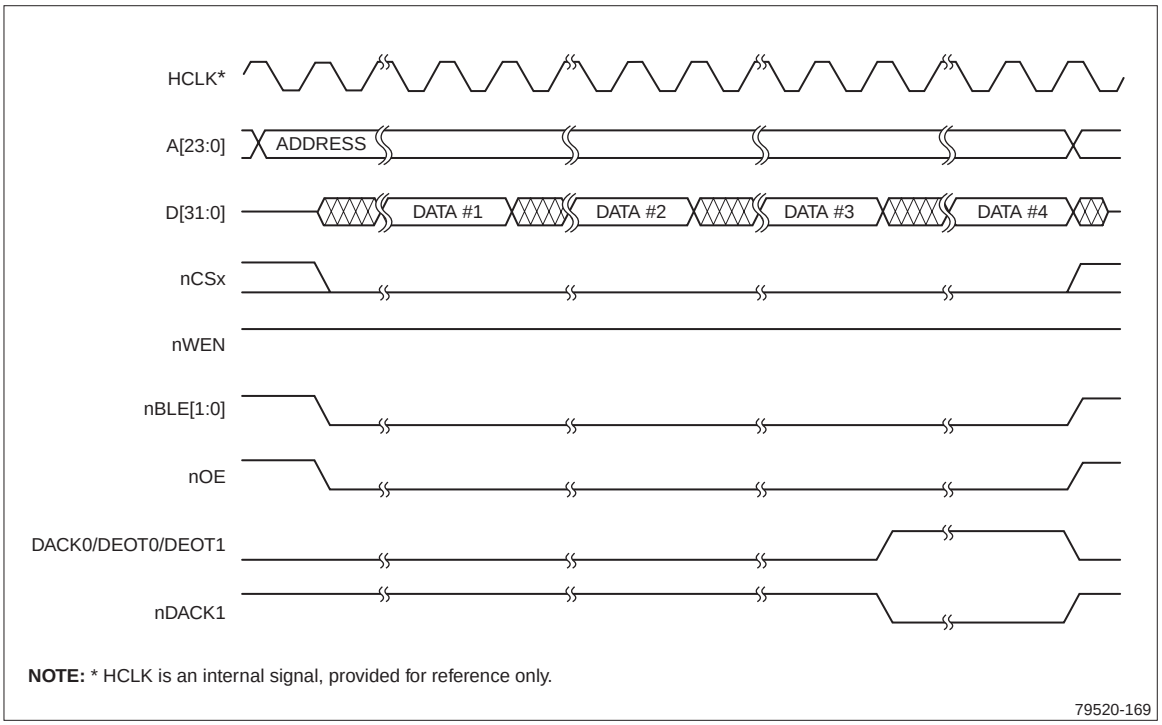


Figure 21. Read, Peripheral to Memory: Peripheral Burst Size = 4

Reset, Clock, and Power Controller (RCPC) Waveforms

Figure 23 shows the method the LH79520 uses when coming out of Reset or Power On.

Figure 24 shows external reset timing, and Table 9 gives the timing parameters.

Table 9. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
tOSC32	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)			550	ms
tOSC14	Oscillator stabilization time after Power Up (VDDC = VDDCMIN)			2.5	ms
tRSTIW	nRESETIN Pulse Width (once sampled LOW)	2			HCLK
tRSTOV	nRESETIN LOW to nRESETOUT valid (once nRESETIN sampled LOW)		3.5		HCLK
tRSTIH	nRESETIN hold extend to allow PLL to lock once XTAL is stable			10	µs
tRSTOH	nRESETOUT hold relative to nRESETIN HIGH		1		HCLK

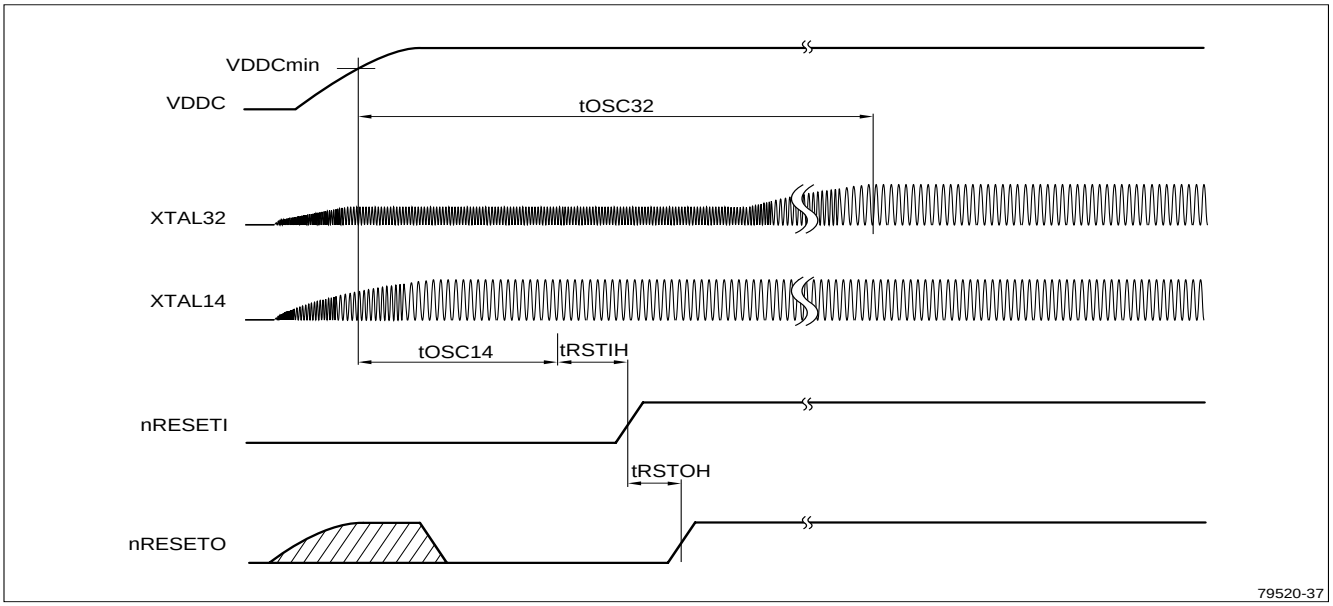


Figure 23. PLL Start-up

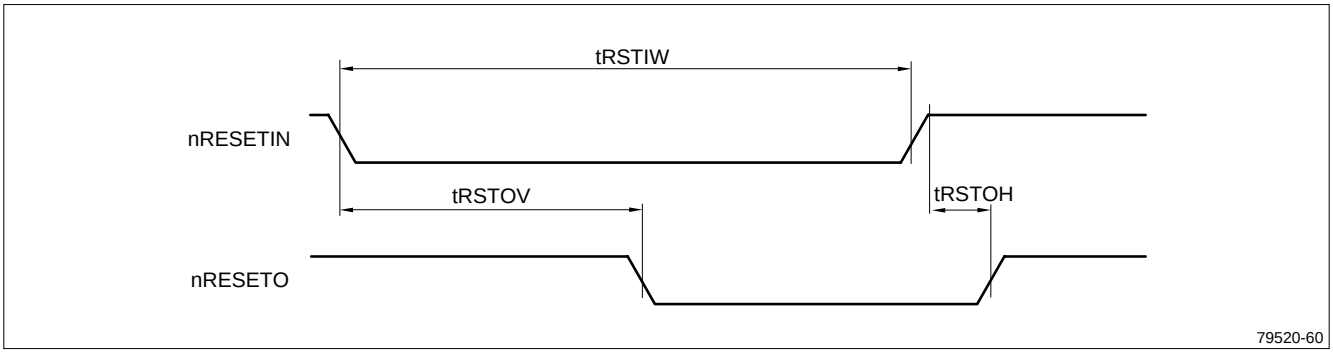
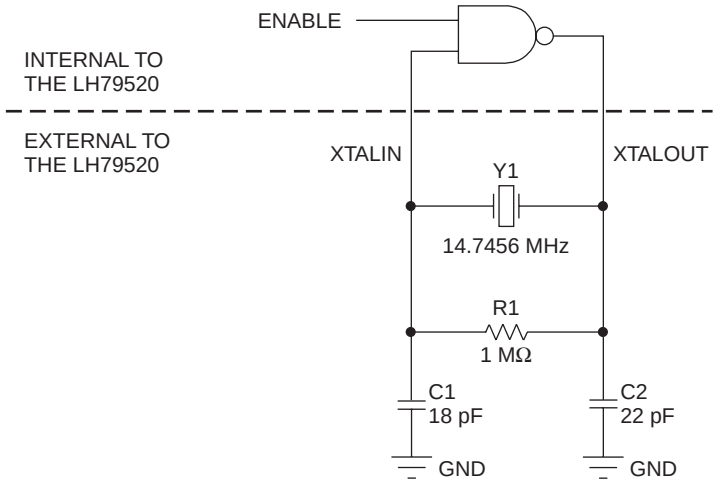


Figure 24. External Reset

Figure 27 shows the suggested external components for the 14.7456 MHz crystal circuit to be used with the SHARP LH79520. The NAND gate represents the logic inside the SoC. See the chart for crystal specifics.



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

79520-173

Figure 27. Suggested External Components, 14.7456 MHz Oscillator

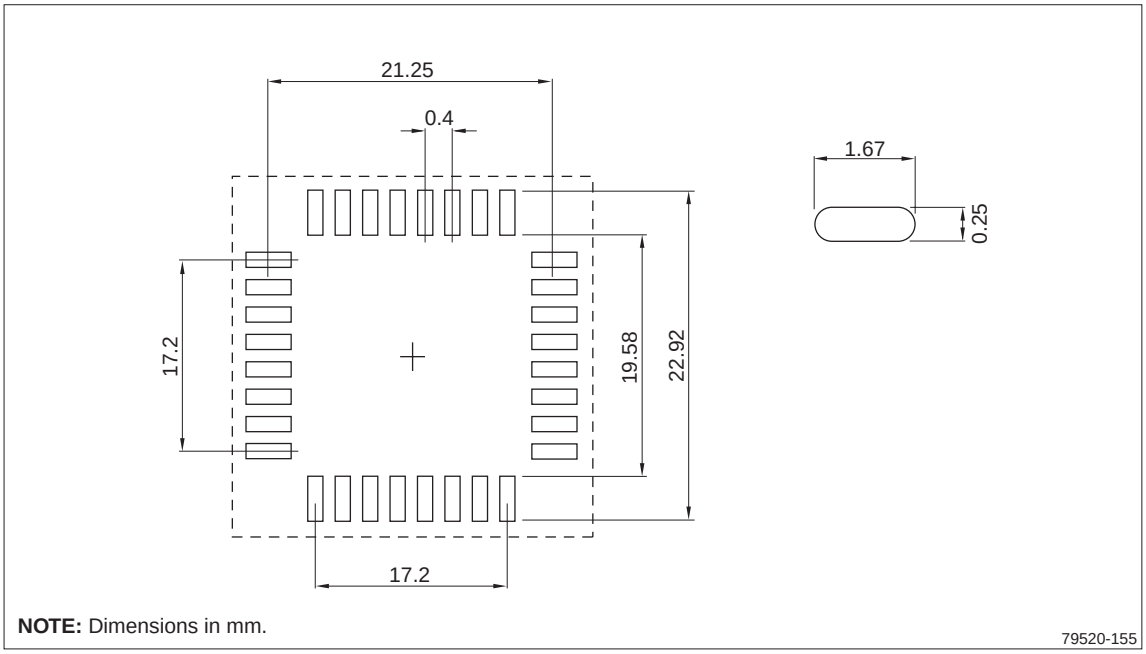


Figure 29. Recommended PCB Footprint