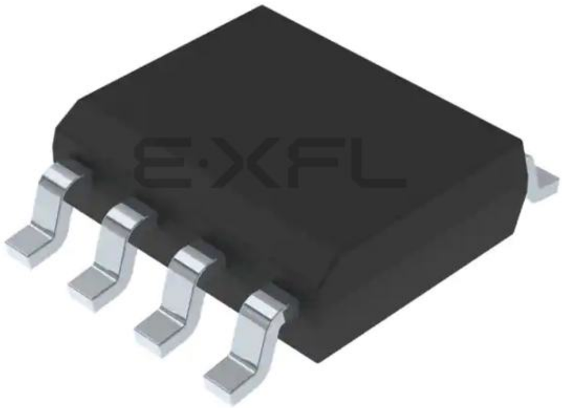

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s001j3m3tr

List of figures

1 Introduction

This datasheet contains the description of the STM8S001J3 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S and STM8A microcontroller families reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the PM0051 (How to program STM8S and STM8A Flash program memory and data EEPROM).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between the lowest power consumption, the fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: the down-counter is refreshed before its value is lower than the one stored in the window register.

4.13.3 I2C

- I2C master features
  - Clock generation
  - Start and stop generation
- I2C slave features
  - Programmable I2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

Table 6 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 6. Flash, Data EEPROM and RAM boundary addresses

Memory area	Size (byte)	Start address	End address
Flash program memory	8 K	0x00 8000	0x00 9FFF
RAM	1 K	0x00 0000	0x00 03FF
Data EEPROM	128	0x00 4000	0x00 407F

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		Reserved		
0x00 5302		Reserved		
0x00 5303		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5304		TIM2_SR1	TIM2 status register 1	0x00
0x00 5305		TIM2_SR2	TIM2 status register 2	0x00
0x00 5306		TIM2_EGR	TIM2 event generation register	0x00
0x00 5307		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5308		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5309		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 530A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 530B		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5310		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5311		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5312		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5313		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5314		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5315		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5316		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		Reserved		
0x00 5342		Reserved		
0x00 5343		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5344		TIM4_SR	TIM4 status register	0x00
0x00 5345		TIM4_EGR	TIM4 event generation register	0x00
0x00 5346		TIM4_CNTR	TIM4 counter	0x00
0x00 5347		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5348		TIM4_ARR	TIM4 auto-reload register	0xFF

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	-	Reserved			0x00 8028
9	-	Reserved			0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/overflow/underflow/ trigger/break	-	-	0x00 8034
12	TIM1	TIM1 capture/compare	-	-	0x00 8038
13	TIM2	TIM2 update /overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/compare	-	-	0x00 8040
15	-	Reserved			0x00 8044
16	-	Reserved			0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054
20	-	Reserved			0x00 8058
21	-	Reserved			0x00 805C
22	ADC1	ADC1 end of conversion/analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1

Table 15. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(3)(4)	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
$\Sigma I_{INJ(PIN)}$(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Guaranteed by characterization results.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

9.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 17*. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	At 1 MHz(2)	-	0.3	ohm
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 125° C	SO8N	-	49	mW
T_A	Ambient temperature	Maximum power dissipation	-40	125	°C
T_J	Junction temperature range	-	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by the design of the internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 10.2: Thermal characteristics on page 79*) with the value for T_{Jmax} given in *Table 17* above and the value for Θ_{JA} given in *Table 49: Thermal characteristics*.

Figure 7. f_{CPUmax} versus V_{DD}

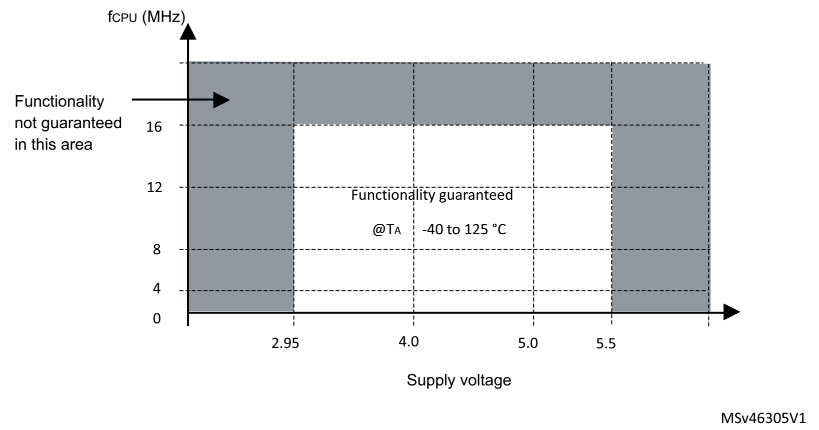


Table 18. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	∞	µs/V
	V_{DD} fall time rate(1)	-	2	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

Total current consumption and timing in forced reset state

Table 28. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
$I_{DD(R)}$	Supply current in reset state [2]	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, VDD = 5 V.

Table 29. Peripheral current consumption

Symbol	Parameter	Typ.	Unit
$I_{DD(TIM1)}$	TIM1 supply current [1]	210	µA
$I_{DD(TIM2)}$	TIM2 supply current [1]	130	
$I_{DD(TIM4)}$	TIM4 timer supply current [1]	50	
$I_{DD(UART1)}$	UART1 supply current[1]	120	
$I_{DD(SPI)}$	SPI supply current[1]	45	
$I_{DD(I2C)}$	I2C supply current [1]	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting[1]	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250 (3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Table 38. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
	Output low level with 4 pins sunk	I_{IO} = 20 mA, V_{DD} = 5 V	-	1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Typical output level curves

Figure 22 to *Figure 29* show typical output level curves measured with output on a single pin.

Figure 21. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

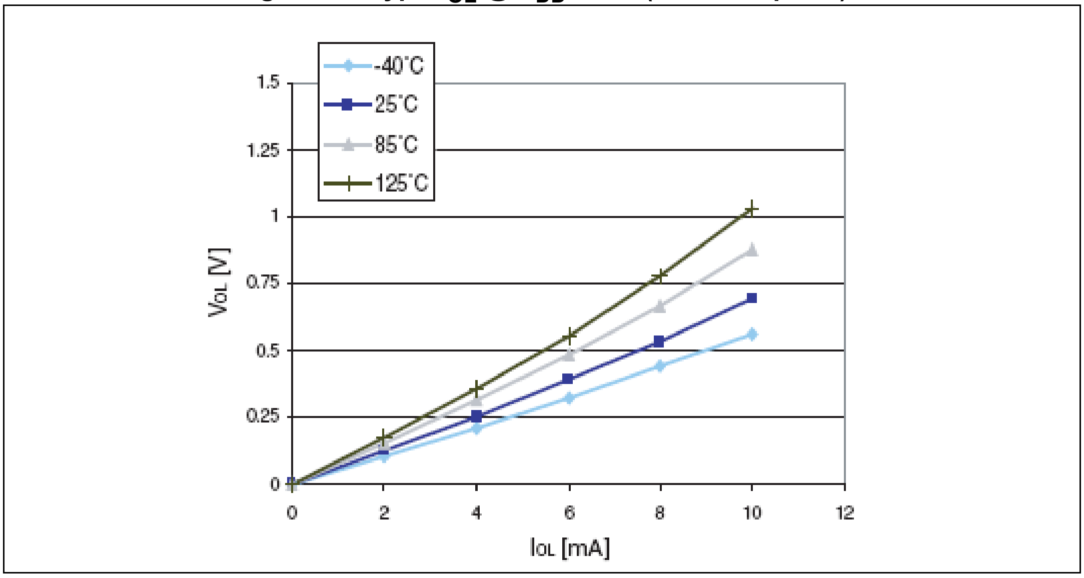
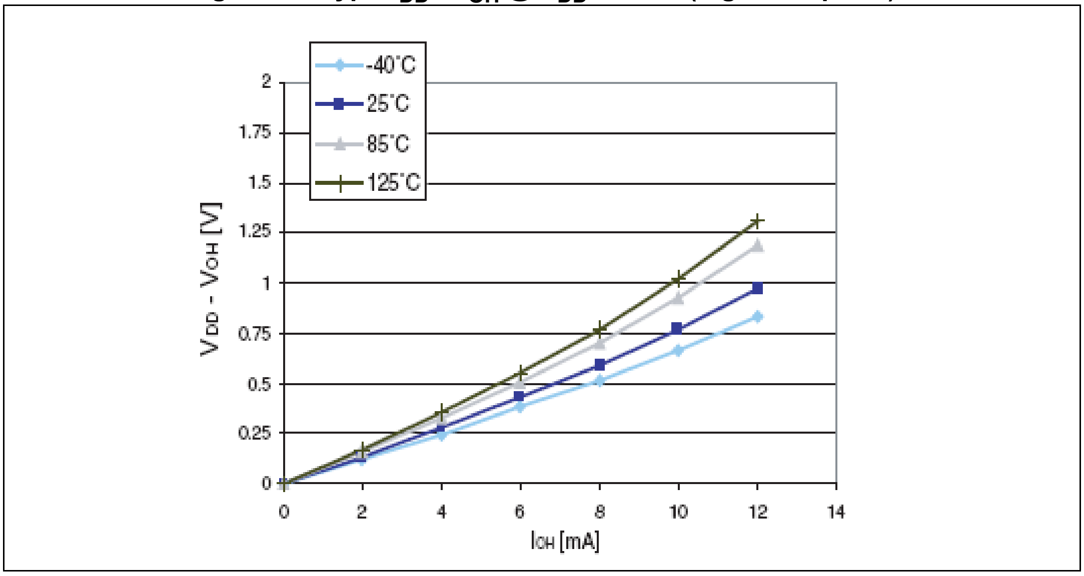


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)



9.3.7 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 39. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

Table 39. SPI characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2 - 15$	$t_{SCK}/2 + 15$	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode	-	3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	65	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	27	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	11	-	

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

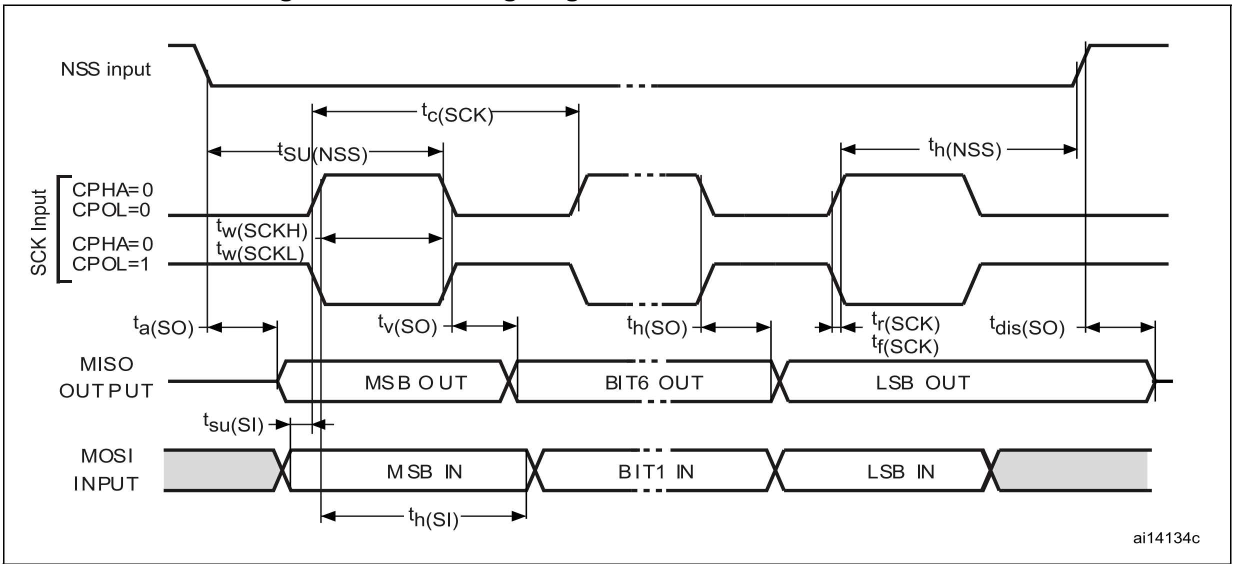
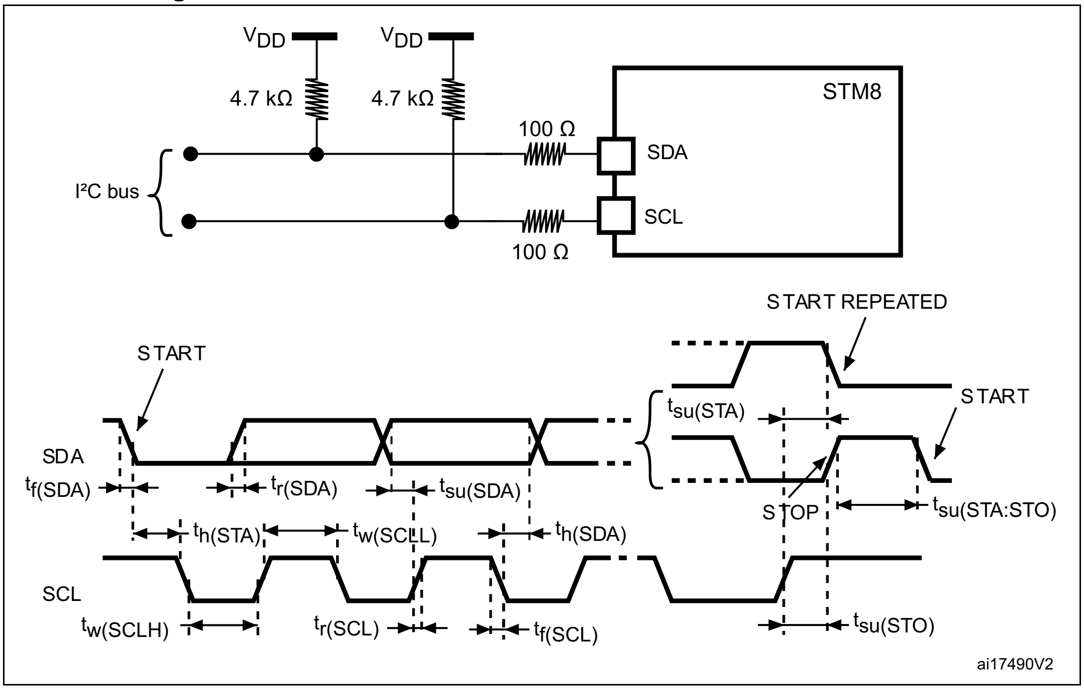


Figure 34. Typical application with I2C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

Table 42. ADC accuracy with R_{AIN} < 10 kΩ , V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\vert E_T \vert$	Total unadjusted error (2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\vert E_O \vert$	Offset error (2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\vert E_G \vert$	Gain error (2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\vert E_D \vert$	Differential linearity error (2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\vert E_L \vert$	Integral linearity error (2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 43. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\vert E_T \vert$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\vert E_O \vert$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\vert E_G \vert$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\vert E_D \vert$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\vert E_L \vert$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

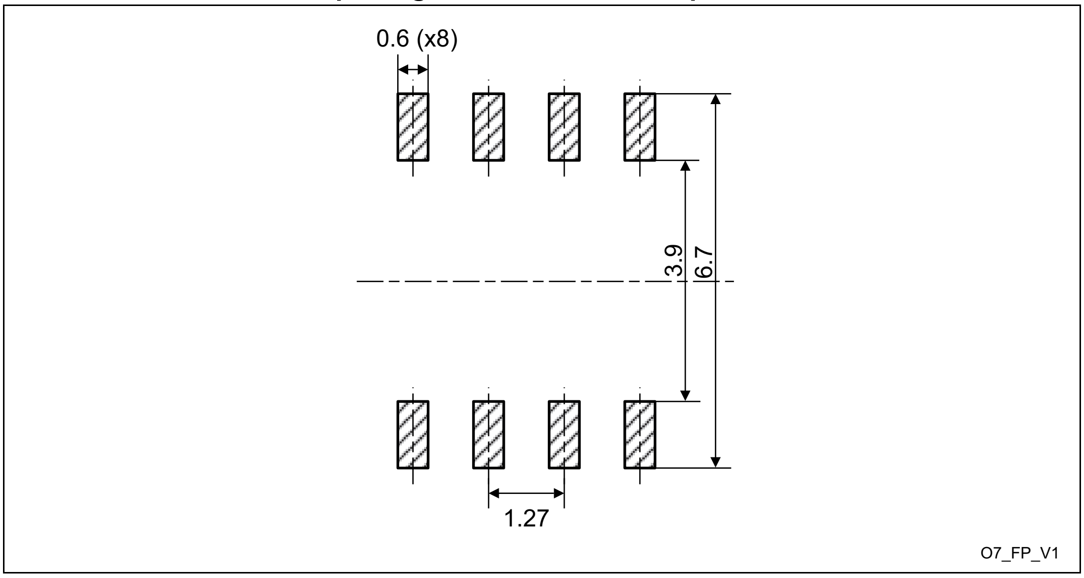
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 48. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 38. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package recommended footprint



Device marking for SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width

The following figure gives an example of topside marking orientation versus pin 1/ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Table 49. Thermal characteristics[1]

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient SO8N	102	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 40: STM8S001J3 ordering information scheme(1)*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax}= 75 °C (measured according to JESD51-2)
- I_{DDmax} = 8 mA, V_{DD} = 5.0 V
- Maximum 4 I/Os used at the same time in output at low level with
  I_{OL} = 8 mA, V_{OL}= 0.4 V
  P_{INTmax} = 8 mA x 5.0 V = 40 mW
  P_{Dmax} = 40 mW + (8 x 0.4 x 4) mW
  Thus: P_{Dmax} = 52.8 mW

Using the values obtained in *Section Table 49.: Thermal characteristics* T_{Jmax} is calculated as follows for SO8N package 102 °C/W :

T_{Jmax} = 75 °C + (102 °C/W x 52.8 mW) = 75 °C + 5.4 °C = 80.4 °C.

Above information is within the range (-40 < T_J < 130 °C)