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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcs12kg256cfue

- Clock and Reset Generator (CRG)
  - Phase-locked loop clock frequency multiplier
  - Self Clock mode in absence of external clock
  - COP watchdog
  - Real Time interrupt (RTI)
- Memory
  - 256K Byte Flash EEPROM
    - Internal program/erase voltage generation
    - Security and Block Protect bits
    - Hamming Error Correction Coding (ECC)
  - 4K Byte EEPROM
  - 12K Byte static RAM

  Single-cycle misaligned word accesses without wait states
- Analog-to-Digital Converters (ADC)
  - Two 8-channel modules with 10-bit resolution
  - External conversion trigger capability
- 8-channel Timer (TIM)
  - Programmable input capture or output compare channels
  - Simple PWM mode
  - Counter Modulo Reset
  - External Event Counting
  - Gated Time Accumulation
- 8-channel Pulse Width Modulator (PWM)
  - Programmable period and duty cycle per channel
  - 8-bit 8-channel or 16-bit 4-channel
  - Edge and center aligned PWM signals
  - Emergency shutdown input
- Three 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Serial interfaces
  - Two asynchronous serial communication interface (SCI)
  - Three synchronous serial peripheral interface (SPI)
  - Inter-IC Bus (IIC)
- Internal 2.5V Regulator
  - Input voltage range from 3.15V to 5.5V

1.2.1 Signal Properties Summary

Table 1-2 summarizes the pin functionality. Signals shown in **bold** are not available in the 80-pin package. Table 1-3 summarizes the power and ground pins.

Table 1-2. Signal Properties (Sheet 1 of 3)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	NA	NA	Oscillator Pins
XTAL	—	—	—	VDDPLL	NA	NA	
RESET	—	—	—	VDDR	None	None	External Reset
TEST	—	—	—	NA	NA	NA	Test Input
VREGEN	—	—	—	VDDX	NA	NA	Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL	NA	NA	PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD[15:8]	**AN1[7:0]**	**—**	**—**	**VDDA**	**None**	**None**	**Port AD Input, Analog Inputs of ATD1**
PAD[7:0]	AN0[7:0]	—	—	VDDA	None	None	Port AD Input, Analog Inputs of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—	VDDR	PUCR	Disabled	Port B I/O, Multiplexed Address/Data
PE7	NOACC	XCLKS	—	VDDR	PUCR	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—	VDDR	PUCR	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—	VDDR	PUCR	Up	Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—	VDDR	PUCR	Up	Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—	VDDR	PUCR	Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	VDDR	PUCR	Up	Port E Input, Non Maskable Interrupt
PH7	**KWH7**	**$\overline{\text{SS2}}$**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI2**
PH6	**KWH6**	**SCK2**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, SCK of SPI2**
PH5	**KWH5**	**MOSI2**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MOSI of SPI2**

Table 1-12. Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
0xFFFE, 0xFFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	—
0xFFFC, 0xFFFD	Clock Monitor fail reset	None	PLLCTL (CME, FCME)	—
0xFFFA, 0xFFFB	COP failure reset	None	COP rate select	—
0xFFF8, 0xFFF9	Unimplemented instruction trap	None	None	—
0xFFF6, 0xFFF7	SWI	None	None	—
0xFFF4, 0xFFF5	XIRQ	X Bit	None	—
0xFFF2, 0xFFF3	IRQ	I Bit	IRQCR (IRQEN)	0xF2
0xFFF0, 0xFFF1	Real Time Interrupt	I Bit	CRGINT (RTIE)	0xF0
0xFFEE, 0xFFEF	Standard Timer channel 0	I Bit	TIE (C0I)	0xEE
0xFFEC, 0xFFED	Standard Timer channel 1	I Bit	TIE (C1I)	0xEC
0xFFEA, 0xFFEB	Standard Timer channel 2	I Bit	TIE (C2I)	0xEA
0xFFE8, 0xFFE9	Standard Timer channel 3	I Bit	TIE (C3I)	0xE8
0xFFE6, 0xFFE7	Standard Timer channel 4	I Bit	TIE (C4I)	0xE6
0xFFE4, 0xFFE5	Standard Timer channel 5	I Bit	TIE (C5I)	0xE4
0xFFE2, 0xFFE3	Standard Timer channel 6	I Bit	TIE (C6I)	0xE2
0xFFE0, 0xFFE1	Standard Timer channel 7	I Bit	TIE (C7I)	0xE0
0xFFDE, 0xFFDF	Standard Timer overflow	I Bit	TSCR2 (TOI)	0xDE
0xFFDC, 0xFFDD	Pulse accumulator overflow	I Bit	PACTL (PAOVI)	0xDC
0xFFDA, 0xFFDB	Pulse accumulator input edge	I Bit	PACTL (PAI)	0xDA
0xFFD8, 0xFFD9	SPI0	I Bit	SPICR1 (SPIE, SPTIE)	0xD8
0xFFD6, 0xFFD7	SCI0	I Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	0xD6
0xFFD4, 0xFFD5	SCI1	I Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	0xD4
0xFFD2, 0xFFD3	ATD0	I Bit	ATDCTL2 (ASCIE)	0xD2
0xFFD0, 0xFFD1	ATD1	I Bit	ATDCTL2 (ASCIE)	0xD0
0xFFCE, 0xFFCF	Port J	I Bit	PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0)	0xCE
0xFFCC, 0xFFCD	Port H	I Bit	PIEH (PIEH7–0)	0xCC
0xFFCA, 0xFFCB	Reserved	I Bit	Reserved	0xCA
0xFFC8, 0xFFC9		I Bit		0xC8
0xFFC6, 0xFFC7	CRG PLL lock	I Bit	CRGINT (LOCKIE)	0xC6
0xFFC4, 0xFFC5	CRG Self Clock Mode	I Bit	CRGINT (SCMIE)	0xC4
0xFFC2, 0xFFC3	FLASH Double Fault Detect	I Bit	FCNFG (DFDIE)	0xC2

be stored in the lower six bits of FDATALO. The faulty parity bits remain readable until the start of the next command write sequence.

2.3.2.12 RESERVED1

This register is reserved for factory testing and is not accessible.

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-19. RESERVED1

All bits read 0 and are not writable.

2.3.2.13 RESERVED2

This register is reserved for factory testing and is not accessible.

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-20. RESERVED2

All bits read 0 and are not writable.

2.3.2.14 RESERVED3

This register is reserved for factory testing and is not accessible.

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-21. RESERVED3

The PVIOL flag will be set after the command is written to the FCMD register during a command write sequence if any of the following illegal operations are attempted, causing the command write sequence to immediately abort:

1. Writing the program command if the address written in the command write sequence was in a protected area of the Flash memory.
2. Writing the sector erase command if the address written in the command write sequence was in a protected area of the Flash memory.
3. Writing the mass erase command while any Flash protection is enabled.

If the PVIOL flag is set in the FSTAT register, the user must clear the PVIOL flag before starting another command write sequence (see Section 2.3.2.7, “Flash Status Register (FSTAT)”).

2.5 Operating Modes

2.5.1 Wait Mode

If a command is active (CCIF = 0) when the MCU enters wait mode, the active command and any buffered command will be completed.

The Flash module can recover the MCU from wait mode if the CBEIF and CCIF interrupts are enabled (Section 2.8, “Interrupts”).

2.5.2 Stop Mode

If a command is active (CCIF = 0) when the MCU enters stop mode, the operation will be aborted and, if the operation is program or erase, the Flash array data being programmed or erased may be corrupted and the CCIF and ACCERR flags will be set. If active, the high voltage circuitry to the Flash memory will immediately be switched off when entering stop mode. Upon exit from stop mode, the CBEIF flag is set and any buffered command will not be launched. The ACCERR flag must be cleared before starting a command write sequence (see Section 2.4.1.2, “Command Write Sequence”).

NOTE

As active commands are immediately aborted when the MCU enters stop mode, it is strongly recommended that the user does not use the STOP instruction during program or erase operations.

2.5.3 Background Debug Mode

In background debug mode (BDM), the FPROT register is writable. If the MCU is unsecured, then all Flash commands listed in Table 2-21 can be executed.

5. If the KEYACC bit does not remain set while the four 16-bit words are written.
6. If any two of the four 16-bit words are written on successive MCU clock cycles.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the Flash security byte can be programmed to the unsecure state, if desired.

In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF00–0xFF07 in the Flash configuration field.

The security as defined in the Flash security byte (0xFF0F) is not changed by using the backdoor key access sequence to unsecure. The backdoor keys stored in addresses 0xFF00–0xFF07 are unaffected by the backdoor key access sequence. After the next reset of the MCU, the security state of the Flash module is determined by the Flash security byte (0xFF0F). The backdoor key access sequence has no effect on the program and erase protections defined in the Flash protection register.

It is not possible to unsecure the MCU in special single-chip mode by using the backdoor key access sequence via the background debug mode (BDM).

2.6.2 Unsecuring the Flash Module in Special Single-Chip Mode using BDM

The MCU can be unsecured in special single-chip mode by erasing the Flash module by the following method:

- Reset the MCU into special single-chip mode, delay while the erase test is performed by the BDM secure ROM, send BDM commands to disable protection in the Flash module, and execute a mass erase command write sequence to erase the Flash memory.

After the CCIF flag sets to indicate that the mass operation has completed, reset the MCU into special single-chip mode. The BDM secure ROM will verify that the Flash memory is erased and will assert the UNSEC bit in the BDM status register. This BDM action will cause the MCU to override the Flash security state and the MCU will be unsecured. All BDM commands will be enabled and the Flash security byte may be programmed to the unsecure state by the following method:

- Send BDM commands to execute a word program sequence to program the Flash security byte to the unsecured state and reset the MCU.

2.7 Resets

2.7.1 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity while loading the following registers from the Flash memory according to Table 2-2:

- FPROT — Flash Protection Register (see Section 2.3.2.5).

  If a double bit fault is detected during the read of the protection field as part of the reset sequence, the FPOPEN bit in the FPROT register will be clear and remaining bits will be set leaving the Flash block fully protected from program and erase.
- FCTL — Flash Control Register (see Section 2.3.2.9).

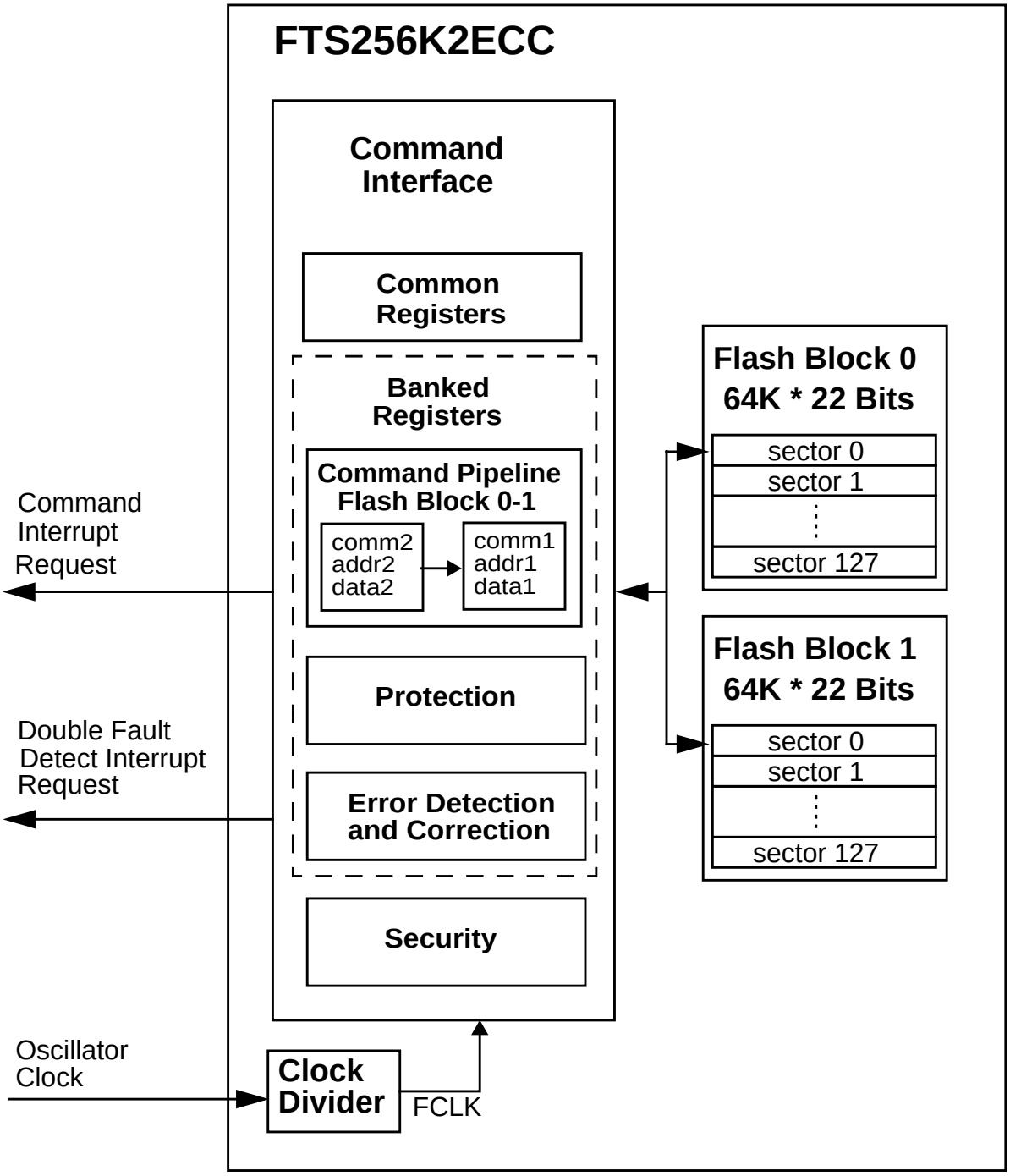

Figure 3-1. FTS256K2ECC Block Diagram

3.2 External Signal Description

The Flash module contains no signals that connect off-chip.

The Flash module also contains a set of 16 control and status registers located in address space module base + 0x0000 to module base + 0x000F. In order to accommodate more than one Flash block with a minimum register address space, a set of registers located from module base + 0x04 to module base + 0x0B are repeated in all banks. The active register bank is selected by the BKSEL bits in the unbanked Flash configuration register (FCNFG). A summary of these registers is given in Table 3-4 while their accessibility in normal and special modes is detailed in Section 3.3.2, “Register Descriptions”.

Table 3-4. Flash Register Map

Module Base +	Use	Normal Mode Access
0x0000	Flash Clock Divider Register (FCLKDIV)	R/W
0x0001	Flash Security Register (FSEC)	R
0x0002	Flash Test Mode Register (FTSTMOD)	R/W
0x0003	Flash Configuration Register (FCNFG)	R/W
0x0004	Flash Protection Register (FPROT)	R/W
0x0005	Flash Status Register (FSTAT)	R/W
0x0006	Flash Command Register (FCMD)	R/W
0x0007	Flash Control Register (FCTL)	R
0x0008	Flash High Address Register (FADDRHI)	R
0x0009	Flash Low Address Register (FADDRLO)	R
0x000A	Flash High Data Register (FDATAHI)	R
0x000B	Flash Low Data Register (FDATALO)	R
0x000C	RESERVED1[1]	R
0x000D	RESERVED2[1]	R
0x000E	RESERVED3[1]	R
0x000F	RESERVED4[1]	R

1 Intended for factory test purposes only.

4.3.2.10 EEPROM Data Register (EDATA)

EDATAHI and EDATALO are the EEPROM data registers.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	EDHI							
Reset	0	0	0	0	0	0	0	0

Figure 4-15. EEPROM Data High Register (EDATAHI)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	EDLO							
Reset	0	0	0	0	0	0	0	0

Figure 4-16. EEPROM Data Low Register (EDATALO)

In normal modes, all EDATAHI and EDATALO bits read 0 and are not writable.

In special modes, all EDATAHI and EDATALO bits are readable and writable.

4.4 Functional Description

4.4.1 Program and Erase Operation

Write and read operations are both used for the program and erase algorithms described in this subsection. These algorithms are controlled by a state machine whose timebase, EECLK, is derived from the oscillator clock via a programmable divider. The command register as well as the associated address and data registers operate as a buffer and a register (2-stage FIFO) so that a new command along with the necessary data and address can be stored to the buffer while the previous command is remains in progress. The pipelined operation allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the EEPROM status register. Interrupts for the EEPROM will be generated if enabled.

The next four subsections describe:

- How to write the ECLKDIV register.
- Command write sequences used to program, erase, and verify the EEPROM memory.
- Valid EEPROM commands.
- Errors resulting from illegal EEPROM operations.

Table 5-1. Pin Functions and Priorities (Sheet 4 of 4)

Port	Pin Name	Pin Function and Priority	Description	Pull Mode after Reset	Pin Function after Reset
Port H	PH7	SS2	Serial Peripheral Interface 2 slave select output in master mode, input in slave mode or master mode.	Hi-Z	GPIO
		GPIO/KWH7	General-purpose I/O with interrupt		
	PH6	SCK2	Serial Peripheral Interface 2 serial clock pin		
		GPIO/KWH6	General-purpose I/O with interrupt		
	PH5	MOSI2	Serial Peripheral Interface 2 master out/slave in pin		
		GPIO/KWH5	General-purpose I/O with interrupt		
	PH4	MISO2	Serial Peripheral Interface 2 master in/slave out pin		
		GPIO/KWH4	General-purpose I/O with interrupt		
	PH3	SS1	Serial Peripheral Interface 1 slave select output in master mode, input in slave mode or master mode.		
		GPIO/KWH3	General-purpose I/O with interrupt		
	PH2	SCK1	Serial Peripheral Interface 1 serial clock pin		
		GPIO/KWH2	General-purpose I/O with interrupt		
	PH1	MOSI1	Serial Peripheral Interface 1 master out/slave in pin		
		GPIO/KWH1	General-purpose I/O with interrupt		
	PH0	MISO1	Serial Peripheral Interface 1 master in/slave out pin		
		GPIO/KWH0	General-purpose I/O with interrupt		
Port J	PJ7	TXCAN4	MSCAN4 transmit pin	Pull-up	GPIO
		SCL	Inter Integrated Circuit serial clock line		
		GPIO/KWJ7	General-purpose I/O with interrupt		
	PJ6	RXCAN4	MSCAN4 receive pin		
		SDA	Inter Integrated Circuit serial data line		
		GPIO/KWJ6	General-purpose I/O with interrupt		
	PJ1	GPIO/KWJ1	General-purpose I/O with interrupt		
	PJ0	GPIO/KWJ0	General-purpose I/O with interrupt		

[1] If CAN0 is routed to PM[3:2] the SPI0 can still be used in bidirectional master mode.

5.3.3 Port M Registers

Port M is associated with three Freescale's scalable controller area network (CAN4, CAN1, CAN0) and one serial peripheral interface (SPI0) modules. Each pin is assigned to these modules according to the following priority: CAN1 > CAN0 > CAN4 > SPI0 > general-purpose I/O.

Refer to the SPI block description chapter for information on enabling and disabling the SPI0. Refer to the MSCAN block description chapter for information on enabling and disabling CAN0, CAN1 or CAN4. The SPI0, CAN0 and CAN4 pins can be re-routed. Refer to Section 5.3.3.8, "Module Routing Register (MODRR)".

During reset, port M pins are configured as high-impedance inputs.

5.3.3.1 Port M I/O Register (PTM)

Module Base + 0x0010

	7	6	5	4	3	2	1	0
R W	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
SPI0			SCK0	MOSI0	SS0	MISO0		
CAN4	TXCAN4	RXCAN4	TXCAN4	RXCAN4				
CAN0			TXCAN0	RXCAN0	TXCAN0	RXCAN0	TXCAN0	RXCAN0
CAN1					TXCAN1	RXCAN1		
Reset	0	0	0	0	0	0	0	0

Figure 5-15. Port M I/O Register (PTM)

Read: Anytime. Write: Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

5.3.3.2 Port M Input Register (PTIM)

Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
W								
Reset	u	u	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 5-16. Port M Input Register (PTIM)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

NOTE

Register address = base address + address offset, where the base address is defined at the MCU level and the address offset is defined at the module level.

6.3.2 Register Descriptions

This section describes in address order all the CRGV4 registers and their individual bits.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SYNR	R	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
	W								
0x0001 REFDV	R	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
	W								
0x0002 CTFLG	R	0	0	0	0	0	0	0	0
	W								
0x0003 CRGFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
	W								
0x0004 CRGINT	R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
	W								
0x0005 CLKSEL	R	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
	W								
0x0006 PLLCTL	R	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
	W								
0x0007 RTICTL	R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
	W								
0x0008 COPCTL	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
	W								
0x0009 FORBYP	R	0	0	0	0	0	0	0	0
	W								
0x000A CTCTL	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 6-3. CRG Register Summary

6.3.2.10 Reserved Register (FORBYP)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-13. Reserved Register (FORBYP)

Read: always read 0x0000 except in special modes

Write: only in special modes

6.3.2.11 Reserved Register (CTCTL)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-14. Reserved Register (CTCTL)

Read: always read 0x0080 except in special modes

Write: only in special modes

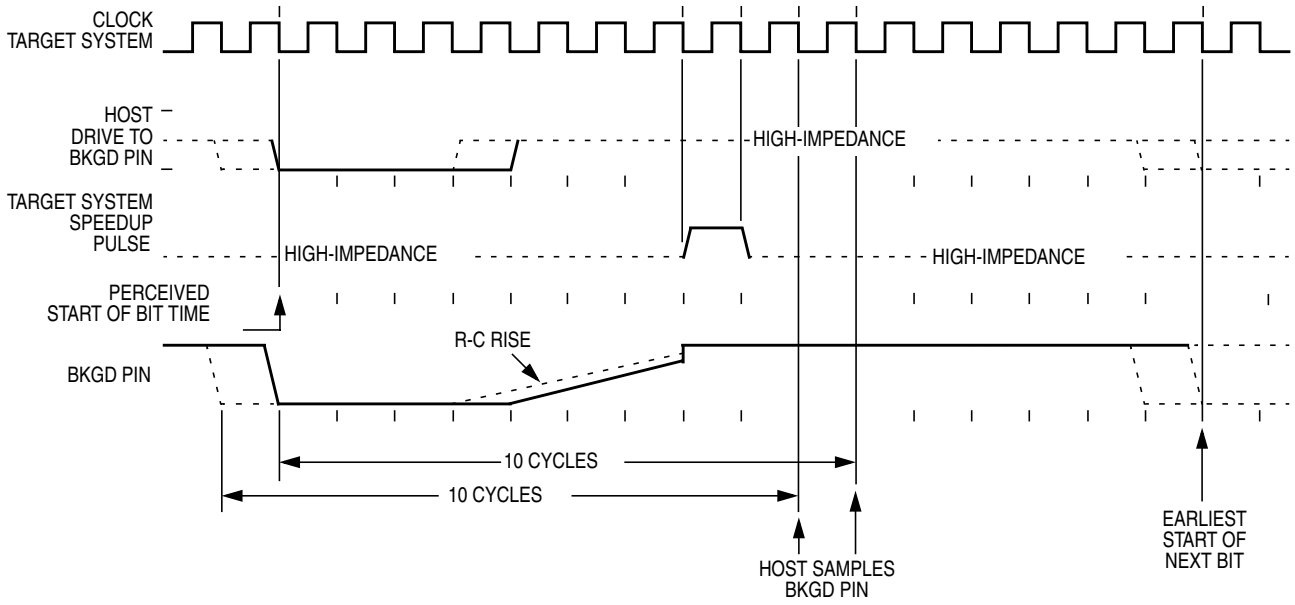

Figure 16-8. BDM Target-to-Host Serial Bit Timing (Logic 1)

Figure 16-9 shows the host receiving a logic 0 from the target. Because the host is asynchronous to the target, there is up to a one clock-cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target. The host initiates the bit time but the target finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

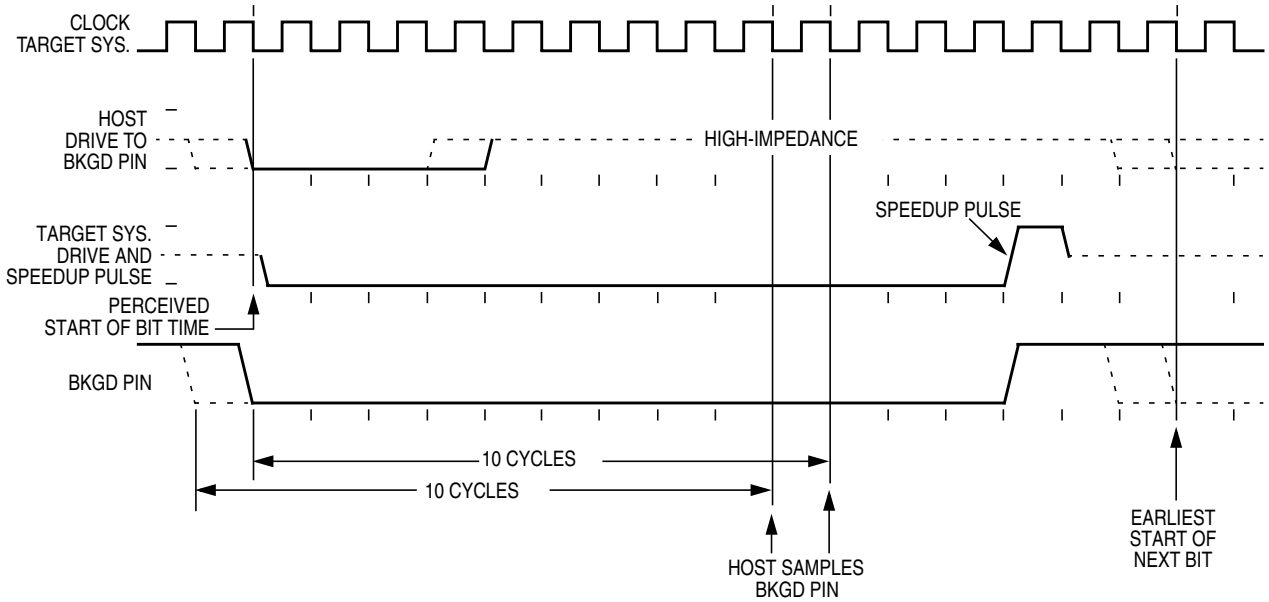

Figure 16-9. BDM Target-to-Host Serial Bit Timing (Logic 0)

19.4.3.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

19.4.3.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull resistors disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with internal pull resistors enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

19.4.3.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

19.4.3.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

19.4.3.3.1 Peripheral Mode

This mode is intended for factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different

The VDDR, VSSR pair supplies the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic.

VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDD1 and VDD2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE

In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 3.3V/5V I/O Pins

Those I/O pins have a nominal level of 3.3V or 5V depending on the application operating point. This group of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group of pins is comprised of the VRH and VRL pins.

A.1.3.3 Oscillator

The pins EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 PLL

The pin XFC dedicated to the oscillator have a nominal 2.5V level. It is supplied by VDDPLL.

A.1.3.5 TEST

This pin is used for production testing only.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	—	—	54	^{o}C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	41	^{o}C/W
3	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	^{o}C/W
4	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	^{o}C/W

1 The values for thermal resistance are achieved by package simulations

2 PC Board according to EIA/JEDEC Standard 51-2

3 PC Board according to EIA/JEDEC Standard 51-7

A.5.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than VRH and $000 for values less than VRL unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-13. ATD Electrical Characteristics

Conditions are shown in Table A-4 unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max input Source Resistance	R_S	—	—	1	KΩ
2	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}	 — —	 — —	 10 22	pF
3	Disruptive Analog Input Current	I_{NA}	–2.5	—	2.5	mA
4	Coupling Ratio positive current injection	K_p	—	—	10^{-4}	A/A
5	Coupling Ratio negative current injection	K_n	—	—	10^{-2}	A/A

A.5.3 ATD Accuracy

Table A-14 and Table A-15 specify the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-14. 5V ATD Conversion Performance

Conditions are shown in Table A-4 unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5m. Vf_{ATDCLK} = 2.0MHz							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB	—	5	—	mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	–3	±2.0	3	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE	—	±7.0	—	Counts
6	P	8-Bit Resolution	LSB	—	20	—	mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
9	P	8-Bit Absolute Error[1]	AE	–1.5	±1.0	1.5	Counts

[1] These values include quantization error which is inherently 1/2 count for any A/D converter.