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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcs12kg256vpve

  - Low power mode capability
  - Low Voltage Reset (LVR) and Low Voltage Interrupt (LVI)
- 20 key wake up inputs
  - Rising or falling edge triggered interrupt capability
  - Digital filter to prevent short pulses from triggering interrupts
  - Programmable pull ups and pull downs
- Operating frequency for ambient temperatures (T_A -40°C to 125°C)
  - 50MHz equivalent to 25MHz Bus Speed
- 112-Pin LQFP or 80-Pin QFP package
  - I/O lines with 3.3V/5V input and drive capability
  - 3.3V/5V A/D converter inputs

1.1.2 Modes of Operation

- Normal modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (Freescale use only)
  - Special Peripheral Mode (Freescale use only)
- Each of the above modes of operation can be configured for three Low power submodes
  - Stop Mode
  - Pseudo Stop Mode
  - Wait Mode
- Secure operation, preventing the unauthorized read and write of the memory contents.

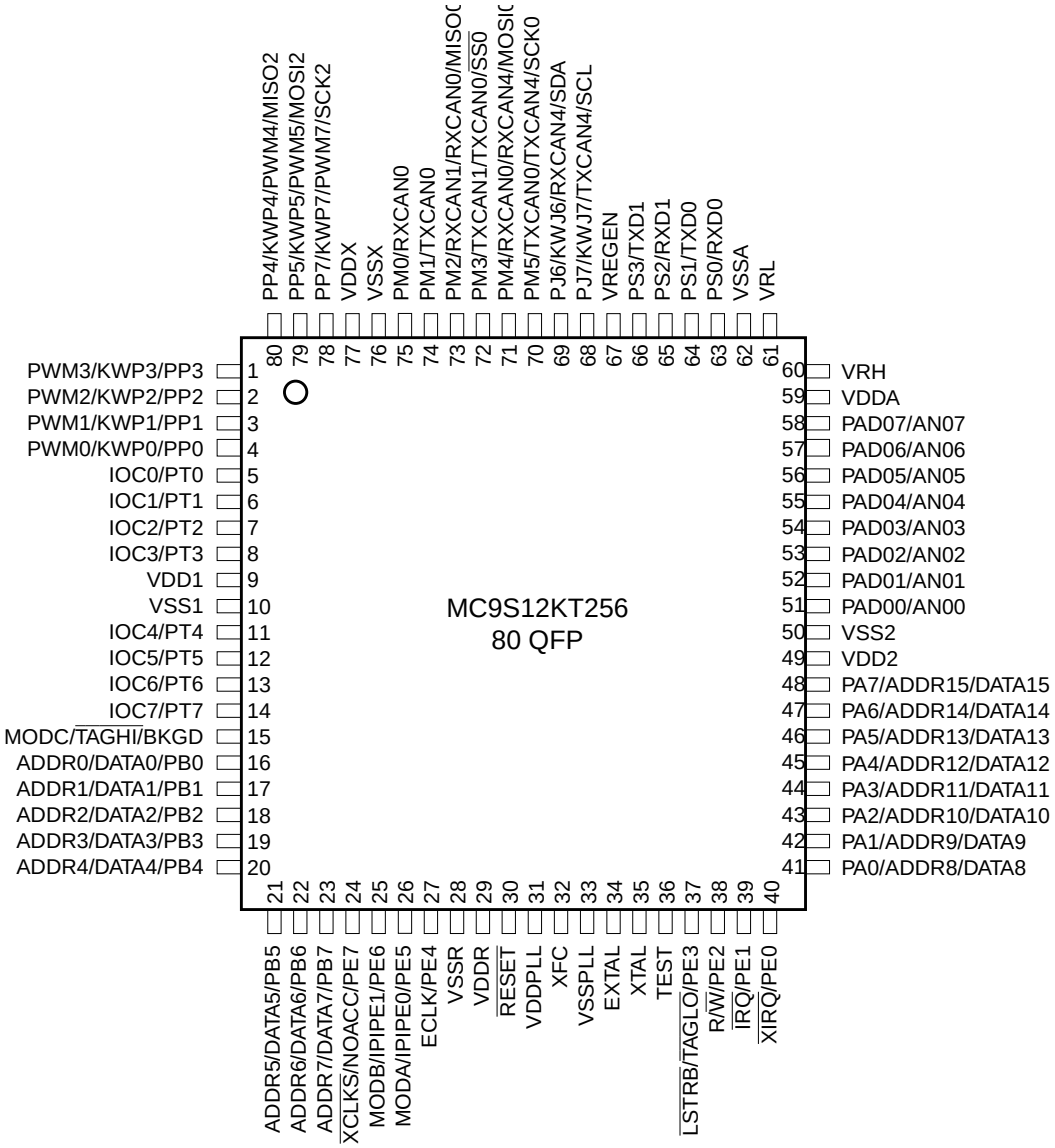

Figure 1-4. Pin Assignments for 80 QFP

0x001C–0x001D MMC Map 3 of 4 (HCS12 Module Mapping Control, Device Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001C	MEMSIZ0	R	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		W								
0x001D	MEMSIZ1	R	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		W								

0x001E–0x001E MEBI Map 2 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001E	INTCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								

0x001F–0x001F INT Map 2 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001F	HPRIO	R	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		W								

0x0020–0x002F DBG Map 1 of 1 (HCS12 Debug)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0020	DBGC1	R	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
	—	W								
0x0021	DBGSC	R	AF	BF	CF	0	TRG			
	—	W								
0x0022	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	—	W								
0x0023	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	—	W								
0x0024	DBGCNT	R	TBF	0	CNT					
	—	W								
0x0025	DBGCCX	R	PAGSEL		EXTCMP					
	—	W								
0x0026	DBGCCH	R	Bit 15	14	13	12	11	10	9	Bit 8
	—	W								
0x0027	DBGCCL	R	Bit 7	6	5	4	3	2	1	Bit 0
	—	W								
0x0028	DBGC2	R	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
	BKPCT0	W								
0x0029	DBGC3	R	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
	BKPCT1	W								
0x002A	DBGCAX	R	PAGSEL		EXTCMP					
	BKP0X	W								
0x002B	DBGCAH	R	Bit 15	14	13	12	11	10	9	Bit 8
	BKP0H	W								

Table 2-8. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01[1]	SECURED
10	**UNSECURED**
11	SECURED

1 Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 2.6, “Flash Module Security”.

2.3.2.3 Flash Test Mode Register (FTSTMOD)

The unbanked FTSTMOD register is used to control Flash test features.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	WRALL	FDFD	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-6. Flash Test Mode Register (FTSTMOD)

FDFD is readable and writable while all remaining bits read 0 and are not writable in normal mode. The WRALL bit is writable only in special mode to simplify mass erase and erase verify operations. When writing to the FTSTMOD register in special mode, all unimplemented/reserved bits must be written to 0.

Table 2-9. FTSTMOD Field Descriptions

Field	Description
4 WRALL	**Write to All Register Banks** — If the WRALL bit is set, all banked registers sharing the same register address will be written simultaneously during a register write. 0 Write only to the bank selected via BKSEL. 1 Write to all register banks.
3 FDFD	**Force Double Fault Detect** — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. 0 Flash array read operations will set the DFDIF flag in the FSTAT register only if a double bit fault is detected. 1 Any Flash array read operation will force the DFDIF flag in the FSTAT register to be set and an interrupt will be generated as long as the DFDIE interrupt enable in the FCNFG register is set.

2.3.2.4 Flash Configuration Register (FCNFG)

The unbanked FCNFG register enables the Flash interrupts and gates the security backdoor writes.

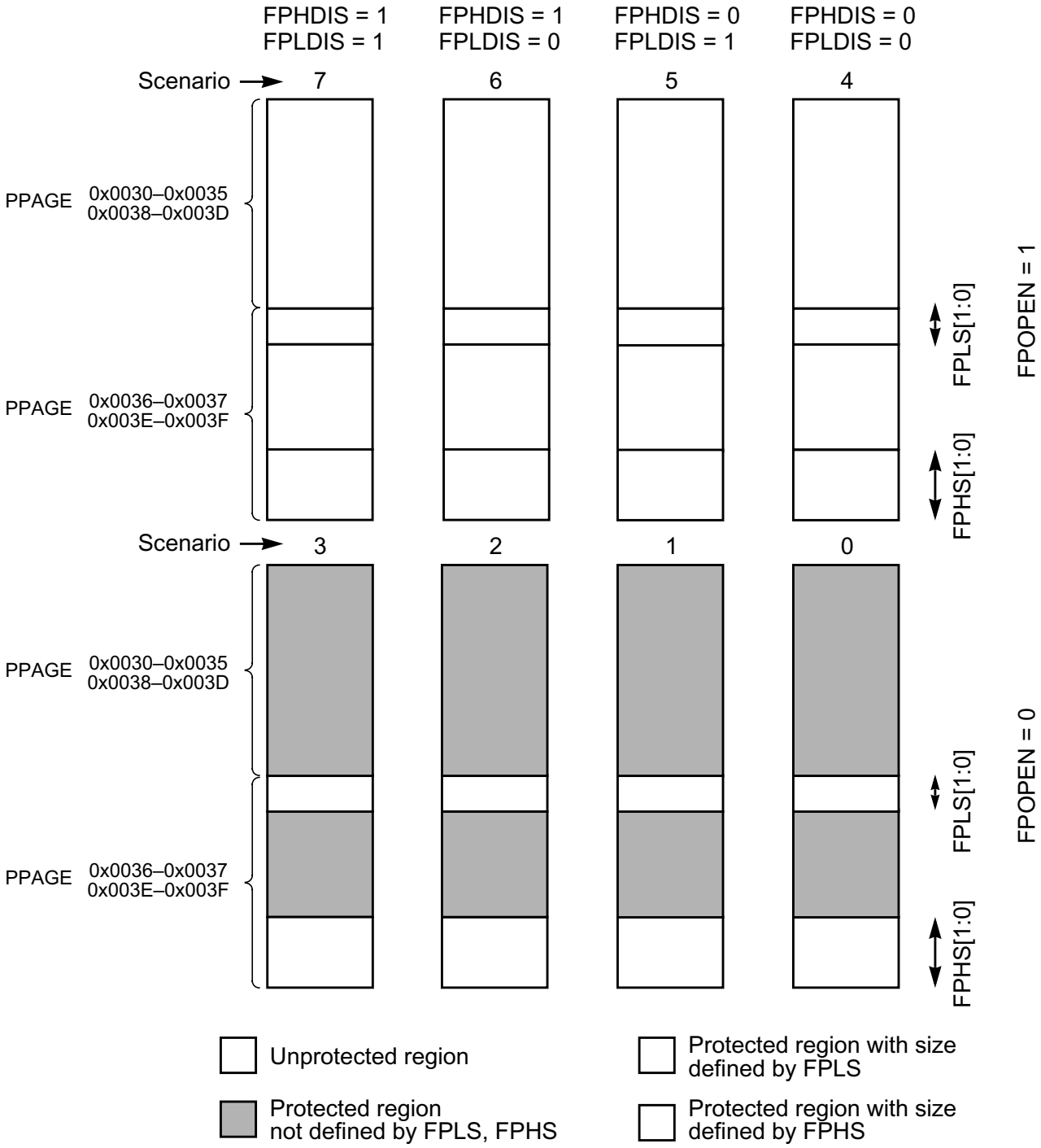

Figure 3-8. Flash Protection Scenarios

3.3.2.6 Flash Protection Restrictions

The general guideline is that Flash protection can only be added and not removed. Table 3-16 specifies all valid transitions between Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored and the FPROT register will remain unchanged. The contents of the

5.3.1.3 Port T Data Direction Register (DDRT)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Figure 5-4. Port T Data Direction Register (DDRT)

Read: Anytime. Write: Anytime.

This register configures each port T pin as either input or output. The TIM forces the I/O state to be an output for each timer port associated with an enabled output compare. In these cases the data direction bits will not change. The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled. The timer input capture always monitors the state of the pin.

Table 5-3. DDRT Field Descriptions

Field	Description
7–0 DDRT[7:0]	**Data Direction Port T** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

5.3.1.4 Port T Reduced Drive Register (RDRT)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset	0	0	0	0	0	0	0	0

Figure 5-5. Port T Reduced Drive Register (RDRT)

Read: Anytime. Write: Anytime.

This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored.

Table 5-4. RDRT Field Descriptions

Field	Description
7–0 RDRT[7:0]	**Reduced Drive Port T** 0 Full drive strength at output. 1 Associated pin drives at about 1/6 of the full drive strength.

5.3.3 Port M Registers

Port M is associated with three Freescale's scalable controller area network (CAN4, CAN1, CAN0) and one serial peripheral interface (SPI0) modules. Each pin is assigned to these modules according to the following priority: CAN1 > CAN0 > CAN4 > SPI0 > general-purpose I/O.

Refer to the SPI block description chapter for information on enabling and disabling the SPI0. Refer to the MSCAN block description chapter for information on enabling and disabling CAN0, CAN1 or CAN4. The SPI0, CAN0 and CAN4 pins can be re-routed. Refer to Section 5.3.3.8, "Module Routing Register (MODRR)".

During reset, port M pins are configured as high-impedance inputs.

5.3.3.1 Port M I/O Register (PTM)

Module Base + 0x0010

	7	6	5	4	3	2	1	0
R W	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
SPI0			SCK0	MOSI0	SS0	MISO0		
CAN4	TXCAN4	RXCAN4	TXCAN4	RXCAN4				
CAN0			TXCAN0	RXCAN0	TXCAN0	RXCAN0	TXCAN0	RXCAN0
CAN1					TXCAN1	RXCAN1		
Reset	0	0	0	0	0	0	0	0

Figure 5-15. Port M I/O Register (PTM)

Read: Anytime. Write: Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

5.3.3.2 Port M Input Register (PTIM)

Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
W								
Reset	u	u	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 5-16. Port M Input Register (PTIM)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

Table 5-17. MODRR Field Descriptions (continued)

Field	Description
3–2 MODRR[3:2]	**CAN4 Routing Bits** — See Table 5-19.
1–0 MODRR[1:0]	**CAN0 Routing Bits** — See Table 5-18.

Table 5-18. CAN0 Routing

MODRR[1]	MODRR[0]	RXCAN0	TXCAN0
0	0	PM0	PM1
0	1	PM2	PM3
1	0	PM4	PM5
1	1	Reserved	

Table 5-19. CAN4 Routing

MODRR[3]	MODRR[2]	RXCAN4	TXCAN4
0	0	PJ6	PJ7
0	1	PM4	PM5
1	0	PM6	PM7
1	1	Reserved	

Table 5-20. SPI0 Routing

MODRR[4]	MISO0	MOSI0	SCK0	SS0
0	PS4	PS5	PS6	PS7
1	PM2	PM4	PM5	PM3

Table 5-21. SPI1 Routing

MODRR[5]	MISO1	MOSI1	SCK1	SS1
0	PP0	PP1	PP2	PP3
1	PH0	PH1	PH2	PH3

Table 5-22. SPI2 Routing

MODRR[6]	MISO2	MOSI2	SCK2	SS2
0	PP4	PP5	PP6	PP7
1	PH4	PH5	PH6	PH7

5.3.6.5 Port J Pull Device Enable Register (PERJ)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
W								
Reset	1	1	—	—	—	—	1	1

= Unimplemented or Reserved

Figure 5-43. Port J Pull Device Enable Register (PERJ)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as wired-OR output. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

Table 5-38. PERJ Field Descriptions

Field	Description
7, 6, 1, 0 PERJ[7:6] PERJ[1:0]	**Pull Device Enable Port J** 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.

5.3.6.6 Port J Polarity Select Register (PPSJ)

Module Base + 0x002D

	7	6	5	4	3	2	1	0
R	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
W								
Reset	0	0	—	—	—	—	0	0

= Unimplemented or Reserved

Figure 5-44. Port J Polarity Select Register (PPSJ)

Read: Anytime. Write: Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

Table 5-39. PPSJ Field Descriptions

Field	Description
7, 6, 1, 0 PPSJ[7:6] PPSJ[1:0]	**Polarity Select Port J** 0 Falling edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-up device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose input or as IIC port. 1 Rising edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-down device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as input.

Table 6-11. Outcome of Clock Loss in Wait Mode

CME	SCME	SCMIE	CRG Actions
0	X	X	Clock failure --> No action, clock loss not detected.
1	0	X	Clock failure --> CRG performs Clock Monitor Reset immediately
1	1	0	Clock failure --> Scenario 1: OSCCLK **recovers** prior to exiting Wait Mode. – MCU remains in Wait Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag. *Some time later OSCCLK recovers.* – CM no longer indicates a failure, – 4096 OSCCLK cycles later Clock Quality Check indicates clock o.k., – SCM deactivated, – PLL disabled depending on PLLWAI, – VREG remains enabled *(never gets disabled in Wait Mode)*. – MCU remains in Wait Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Wait Mode using OSCCLK as system clock (SYSCLK), – Continue normal operation. *or an External Reset is applied.* – Exit Wait Mode using OSCCLK as system clock, – Start reset sequence. Scenario 2: OSCCLK **does not recover** prior to exiting Wait Mode. – MCU remains in Wait Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag, – Keep performing Clock Quality Checks (could continue infinitely) while in Wait Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform additional Clock Quality Checks until OSCCLK is o.k. again. or an External RESET is applied. – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Start reset sequence, – Continue to perform additional Clock Quality Checks until OSCCLK is o.k.again.

8.3.2.11 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Reset	0	0	0	0	0	0	0	0

Figure 8-13. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 8-21. ATDDIEN Field Descriptions

Field	Description
7–0 IEN[7:0]	**ATD Digital Input Enable on channel x (x = 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

8.3.2.12 Port Data Register (PORTAD)

The data port associated with the ATD can be configured as general-purpose I/O or input only, as specified in the device overview. The port pins are shared with the analog A/D inputs AN7–0.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
W								
Reset	1	1	1	1	1	1	1	1
Pin Function	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

= Unimplemented or Reserved

Figure 8-14. Port Data Register (PORTAD)

Read: Anytime

Write: Anytime, no effect

The A/D input channels may be used for general purpose digital input.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

Module Base + 0xXXXD

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 10-35. Transmit Buffer Priority Register (TBPR)

Read: Anytime when TXEx flag is set (see Section 10.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 10.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Anytime when TXEx flag is set (see Section 10.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 10.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

10.3.3.5 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a time stamp to the respective registers in the active transmit or receive buffer right after the EOF of a valid message on the CAN bus (see Section 10.3.2.1, "MSCAN Control Register 0 (CANCTL0)"). In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timer value, which is used for stamping, is taken from a free running internal CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to 0) during initialization mode. The CPU can only read the time stamp registers.

Module Base + 0xXXXE

	7	6	5	4	3	2	1	0
R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
W								
Reset:	x	x	x	x	x	x	x	x

Figure 10-36. Time Stamp Register — High Byte (TSRH)

Module Base + 0xXXXF

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 10-37. Time Stamp Register — Low Byte (TSRL)

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the **Tx output** signal. Setting TE after the stop bit appears on **Tx output signal** causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

NOTE

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

11.4.4 Receiver

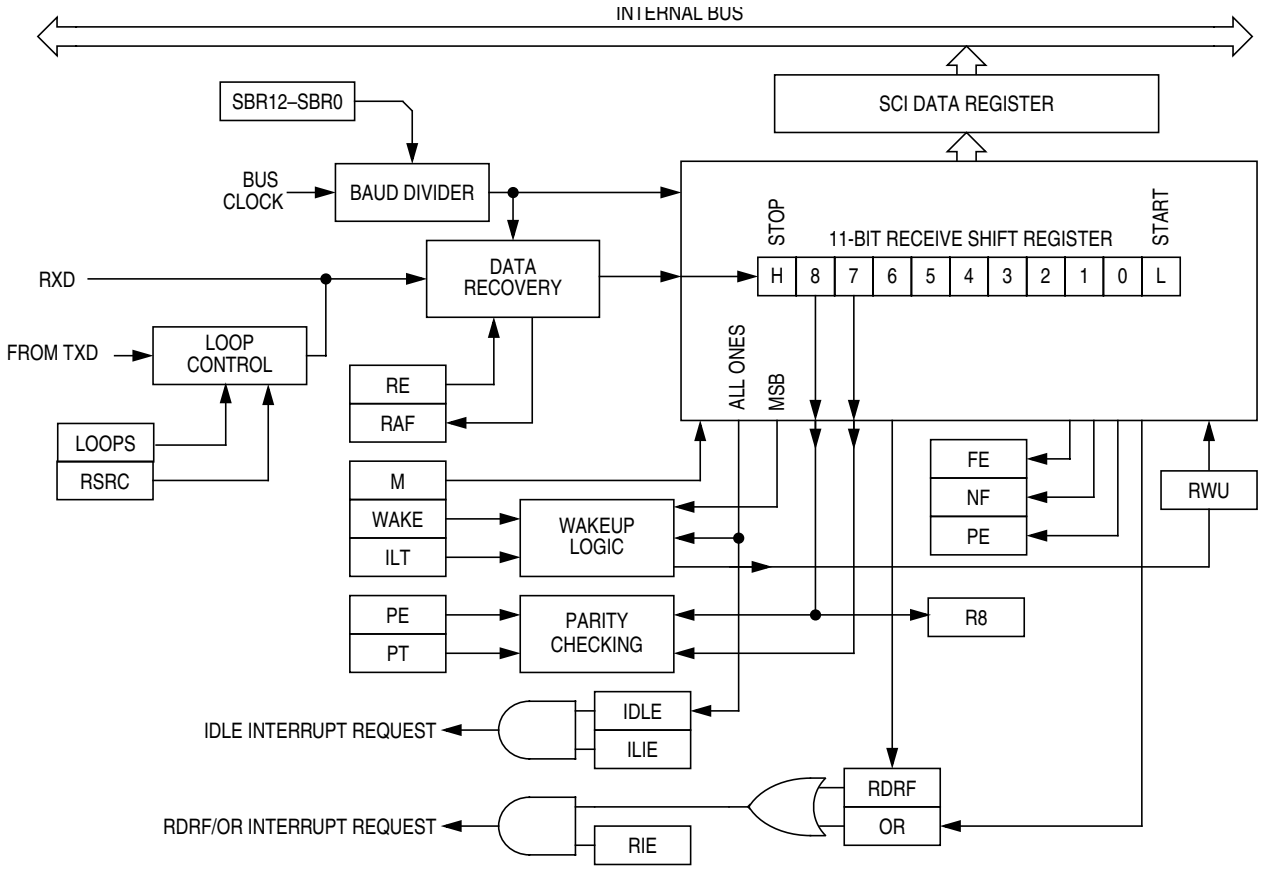

Figure 11-12. SCI Receiver Block Diagram

11.4.4.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

Chapter 12
Serial Peripheral Interface (SPIV3) Block Description

12.1 Introduction

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or the SPI operation can be interrupt driven.

12.1.1 Features

The SPIV3 includes these distinctive features:

- Master mode and slave mode
- Bidirectional mode
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- Control of SPI operation during wait mode

12.1.2 Modes of Operation

The SPI functions in three modes, run, wait, and stop.

- Run Mode
  This is the basic mode of operation.
- Wait Mode
  SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in Run Mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into Run Mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.
- Stop Mode
  The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

This is a high level description only, detailed descriptions of operating modes are contained in Section 12.4, “Functional Description.”

In master mode, with slave select output enabled the $\overline{SS}$ line is always deasserted and reasserted between successive transfers for at least minimum idle time.

12.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the 8-cycle transfer operation.

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

When the third edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the SPI shift register, depending on LSBFE bit. After this edge, the next bit of the master data is coupled out of the serial data output pin of the master to the serial input pin on the slave.

This process continues for a total of 16 edges on the SCK line with data being latched on even numbered edges and shifting taking place on odd numbered edges.

Data reception is double buffered, data is serially shifted into the SPI shift register during the transfer and is transferred to the parallel SPI Data Register after the last bit is shifted in.

After the 16th SCK edge:

- Data that was previously in the SPI Data Register of the master is now in the data register of the slave, and data that was in the data register of the slave is in the master.
- The SPIF flag bit in SPISR is set indicating that the transfer is complete.

Figure 12-10 shows two clocking variations for CPHA = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The $\overline{SS}$ line is the slave select input to the slave. The $\overline{SS}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode

In master mode, if a transmission has completed and a new data byte is available in the SPI Data Register, this byte is send out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low order CAEx bit. The high order CAEx bit has no effect.

Table 13-11 is used to summarize which channels are used to set the various control bits when in 16-bit mode.

Table 13-11. 16-bit Concatenation Mode Summary

CONxx	PWMEx	PPOLx	PCLKx	CAEx	PWMx Output
CON67	PWME7	PPOL7	PCLK7	CAE7	PWM7
CON45	PWME5	PPOL5	PCLK5	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	CAE1	PWM1

13.4.2.8 PWM Boundary Cases

Table 13-12 summarizes the boundary conditions for the PWM regardless of the output mode (left aligned or center aligned) and 8-bit (normal) or 16-bit (concatenation).

Table 13-12. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
$00 (indicates no duty)	>$00	1	Always low
$00 (indicates no duty)	>$00	0	Always high
XX	$00[1] (indicates no period)	1	Always high
XX	$00[1] (indicates no period)	0	Always low
>= PWMPERx	XX	1	Always high
>= PWMPERx	XX	0	Always low

[1] Counter = $00 and does not count.

13.5 Resets

The reset state of each individual bit is listed within the Section 13.3.2, “Register Descriptions” which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters do not count.

Read: Anytime

Write: Anytime

Table 14-3. TIOS Field Descriptions

Field	Description
7:0 IOS[7:0]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding channel acts as an input capture. 1 The corresponding channel acts as an output compare.

14.3.2.2 Timer Compare Force Register (CFORC)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
Reset	0	0	0	0	0	0	0	0

Figure 14-7. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 14-4. CFORC Field Descriptions

Field	Description
7:0 FOC[7:0]	**Force Output Compare Action for Channel 7:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. **Note:** A successful channel 7 output compare overrides any channel 6:0 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

14.3.2.3 Output Compare 7 Mask Register (OC7M)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
Reset	0	0	0	0	0	0	0	0

Figure 14-8. Output Compare 7 Mask Register (OC7M)

Read: Anytime

Write: Anytime

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes (test_mode = 1).

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

14.3.2.6 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-12. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

Table 14-7. TSCR1 Field Descriptions

Field	Description
7 TEN	**Timer Enable** 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator because the ÷64 is generated by the timer prescaler.
6 TSWAI	**Timer Module Stops While in Wait** 0 Allows the timer module to continue running during wait. 1 Disables the timer module when the MCU is in the wait mode. Timer interrupts cannot be used to get the MCU out of wait. TSWAI also affects pulse accumulator.

The BDM hardware commands are listed in Table 16-5.

Table 16-5. Hardware Commands

Command	Opcode (hex)	Data	Description
BACKGROUND	90	None	Enter background mode if firmware is enabled. If enabled, an ACK will be issued when the part enters active background mode.
ACK_ENABLE	D5	None	Enable handshake. Issues an ACK pulse after the command is executed.
ACK_DISABLE	D6	None	Disable handshake. This command does not issue an ACK pulse.
READ_BD_BYTE	E4	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
READ_BD_WORD	EC	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Must be aligned access.
READ_BYTE	E0	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
READ_WORD	E8	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Must be aligned access.
WRITE_BD_BYTE	C4	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
WRITE_BD_WORD	CC	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Must be aligned access.
WRITE_BYTE	C0	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
WRITE_WORD	C8	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Must be aligned access.

NOTE:
If enabled, ACK will occur when data is ready for transmission for all BDM READ commands and will occur after the write is complete for all BDM WRITE commands.

The READ_BD and WRITE_BD commands allow access to the BDM register locations. These locations are not normally in the system memory map but share addresses with the application in memory. To distinguish between physical memory locations that share the same address, BDM memory resources are enabled just for the READ_BD and WRITE_BD access cycle. This allows the BDM to access BDM locations unobtrusively, even if the addresses conflict with the application memory map.

16.4.4 Standard BDM Firmware Commands

Firmware commands are used to access and manipulate CPU resources. The system must be in active BDM to execute standard BDM firmware commands, see Section 16.4.2, “Enabling and Activating BDM.” Normal instruction execution is suspended while the CPU executes the firmware located in the standard BDM firmware lookup table. The hardware command BACKGROUND is the usual way to activate BDM.

As the system enters active BDM, the standard BDM firmware lookup table and BDM registers become visible in the on-chip memory map at 0xFF00–0xFFFF, and the CPU begins executing the standard BDM

The DBG in DBG mode includes these distinctive features:

- Three comparators (A, B, and C)
  - Dual mode, comparators A and B used to compare addresses
  - Full mode, comparator A compares address and comparator B compares data
  - Can be used as trigger and/or breakpoint
  - Comparator C used in LOOP1 capture mode or as additional breakpoint
- Four capture modes
  - Normal mode, change-of-flow information is captured based on trigger specification
  - Loop1 mode, comparator C is dynamically updated to prevent redundant change-of-flow storage.
  - Detail mode, address and data for all cycles except program fetch (P) and free (f) cycles are stored in trace buffer
  - Profile mode, last instruction address executed by CPU is returned when trace buffer address is read
- Two types of breakpoint or debug triggers
  - Break just before a specific instruction will begin execution (tag)
  - Break on the first instruction boundary after a match occurs (force)
- BDM or SWI breakpoint
  - Enter BDM on breakpoint (BDM)
  - Execute SWI on breakpoint (SWI)
- Nine trigger modes for comparators A and B
  - A
  - A or B
  - A then B
  - A and B, where B is data (full mode)
  - A and not B, where B is data (full mode)
  - Event only B, store data
  - A then event only B, store data
  - Inside range, $A \leq address \leq B$
  - Outside range, address $< A$ or address $> B$
- Comparator C provides an additional tag or force breakpoint when capture mode is not configured in LOOP1 mode.
- Sixty-four word (16 bits wide) trace buffer for storing change-of-flow information, event only data and other bus information.
  - Source address of taken conditional branches (long, short, bit-conditional, and loop constructs)
  - Destination address of indexed JMP, JSR, and CALL instruction.
  - Destination address of RTI, RTS, and RTC instructions
  - Vector address of interrupts, except for SWI and BDM vectors