STMicroelectronics - STM32F031C6T6TR Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031c6t6tr

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3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.13 Inter-integrated circuit interface (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripheral can be served by the DMA controller.

Table 7. STM32F031x4/x6 I^2C implementation

I^2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds one universal synchronous/asynchronous receiver/transmitter (USART1) which communicates at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 11. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
6	3	3	3	B5	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	4	4	4	C5	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	16 (3)	0(3)	16 (3)	E1 (3)	15 (3)	VSSA	S		-	Analog ground	
9	5	5	5	D5	5	VDDA	S		-	Analog power supply	
10	6	6	6	B4	6	PA0	I/O	TTa	-	TIM2_CH1_ETR, USART1_CTS	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	7	C4	7	PA1	I/O	TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS	ADC_IN1
12	8	8	8	D4	8	PA2	I/O	TTa	-	TIM2_CH3, USART1_TX	ADC_IN2
13	9	9	9	E5	9	PA3	I/O	TTa	-	TIM2_CH4, USART1_RX	ADC_IN3
14	10	10	10	B3	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK	ADC_IN4
15	11	11	11	C3	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR	ADC_IN5
16	12	12	12	D3	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6

Table 14. STM32F031x4/x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

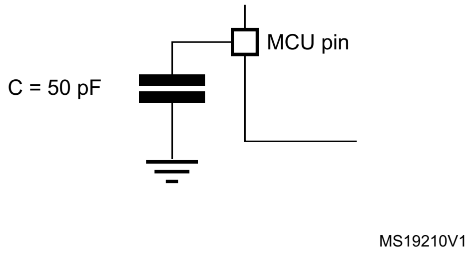


Figure 11. Pin input voltage

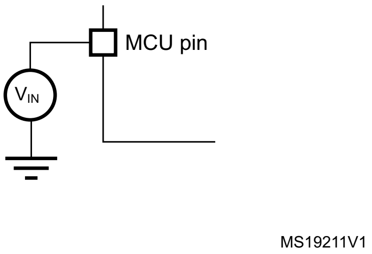


Table 23. Typical and maximum current consumption from V_{DD} at 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	10.7	11.7(2)	11.9	12.5(2)	2.4	2.6(2)	2.7	2.9(2)	mA
			32 MHz	7.1	7.8	8.1	8.2	1.6	1.7	1.9	1.9	
			24 MHz	5.5	6.3	6.4	6.4	1.3	1.4	1.5	1.5	
		HSE bypass, PLL off	8 MHz	1.8	2.0	2.0	2.1	0.4	0.4	0.5	0.5	
			1 MHz	0.2	0.5	0.5	0.5	0.1	0.1	0.1	0.1	
		HSI clock, PLL on	48 MHz	10.8	11.9	12.1	12.6	2.4	2.7	2.7	2.9	
			32 MHz	7.3	8.0	8.4	8.5	1.7	1.9	1.9	2.0	
			24 MHz	5.5	6.2	6.5	6.5	1.3	1.5	1.5	1.6	
		HSI clock, PLL off	8 MHz	1.9	2.2	2.3	2.4	0.5	0.5	0.5	0.6	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 24. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	$V_{DDA} = 2.4$ V				$V_{DDA} = 3.6$ V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSE bypass, PLL on	48 MHz	150	170(3)	178	182(3)	164	183(3)	195	198(3)	µA
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent of clock frequencies.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 27. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical run mode		Typical Sleep mode		unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	-
I_{DD}	Current from V_{DD} supply	48MHz	20.2	12.3	11.1	2.9	mA
		36 MHz	15.3	9.5	8.4	2.4	
		32 MHz	13.6	8.6	7.5	2.2	
		24 MHz	10.5	6.7	5.9	1.8	
		16 MHz	7.2	4.7	4.1	1.4	
		8 MHz	3.8	2.7	2.3	0.9	
		4 MHz	2.4	1.8	1.7	0.9	
		2 MHz	1.6	1.3	1.2	0.8	
		1 MHz	1.2	1.1	1.0	0.8	
		500 kHz	1.0	1.0	0.9	0.8	
I_{DDA}	Current from V_{DDA} supply	48MHz	155				uA
		36 MHz	117				
		32 MHz	105				
		24 MHz	83				
		16 MHz	60				
		8 MHz	2.2				
		4 MHz	2.2				
		2 MHz	2.2				
		1 MHz	2.2				
		500 kHz	2.2				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 46: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 36. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	–4.2(3)	-	5.1(3)	%
		T_A = –10 to 85 °C	–3.2(3)	-	3.1(3)	%
		T_A = 0 to 70 °C	–2.5(3)	-	2.3(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 19. HSI14 oscillator accuracy characterization results

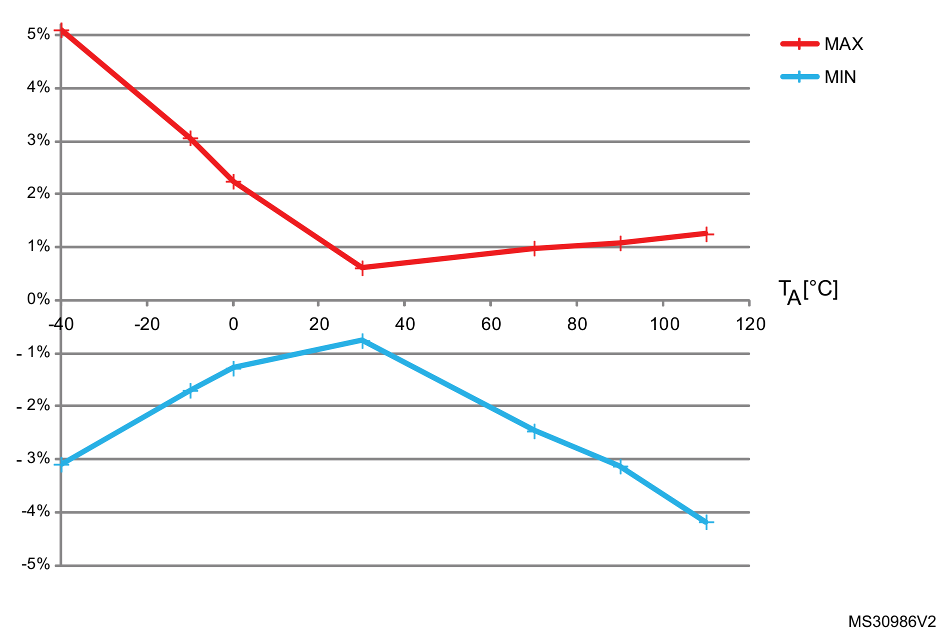


Table 46. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = - V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 45: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 20* for standard I/Os, and in *Figure 21* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Input/output AC characteristics

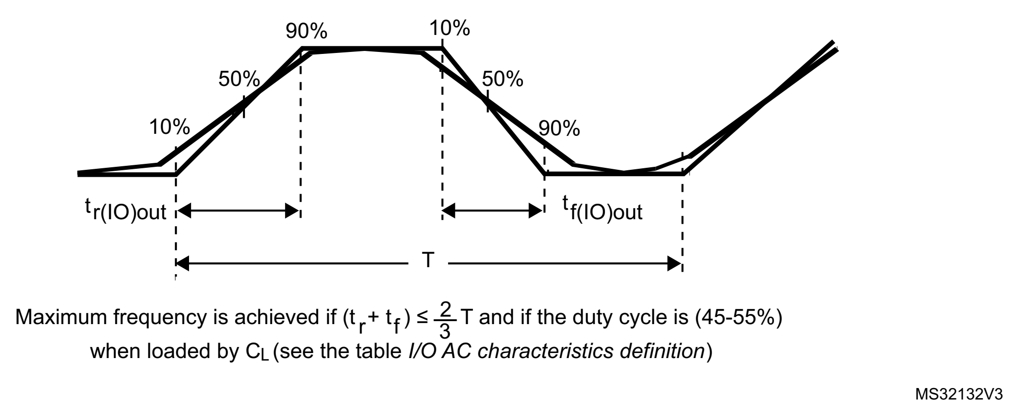
The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 48*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 48. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	30	
			C_L = 50 pF, $V_{DDIOx} < 2.7$ V	-	20	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, $V_{DDIOx} < 2.7$ V	-	12	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, $V_{DDIOx} < 2.7$ V	-	12	
Fm+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 22*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq \frac{2}{3}T$ and if the duty cycle is (45-55%) when loaded by C_L (see the table *I/O AC characteristics definition*)

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

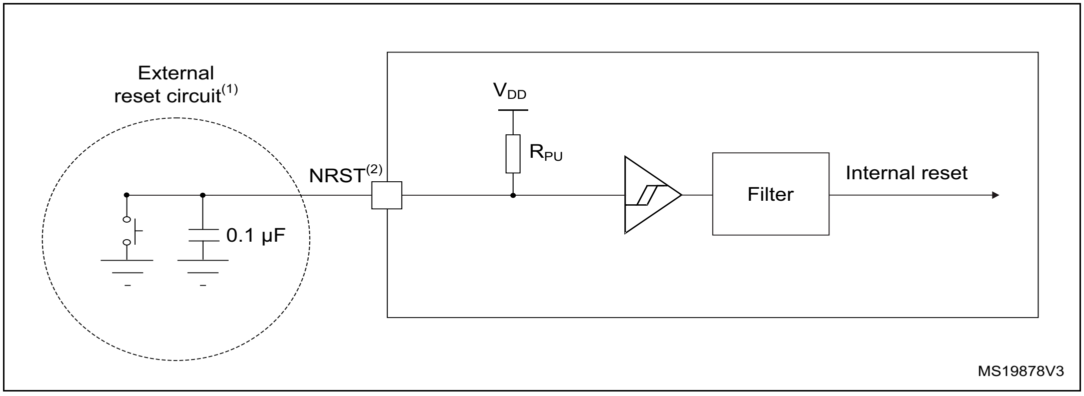
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 V_{DD}+0.07[1]	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445 V_{DD}+0.398[1]	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100[1]	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300[3]	-	-	ns
		$2.0 < V_{DD} < 3.6$	500[3]	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 23. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 49: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 18: General operating conditions*.

Note: *It is recommended to perform a calibration after each power-up.*

Table 50. ADC characteristics

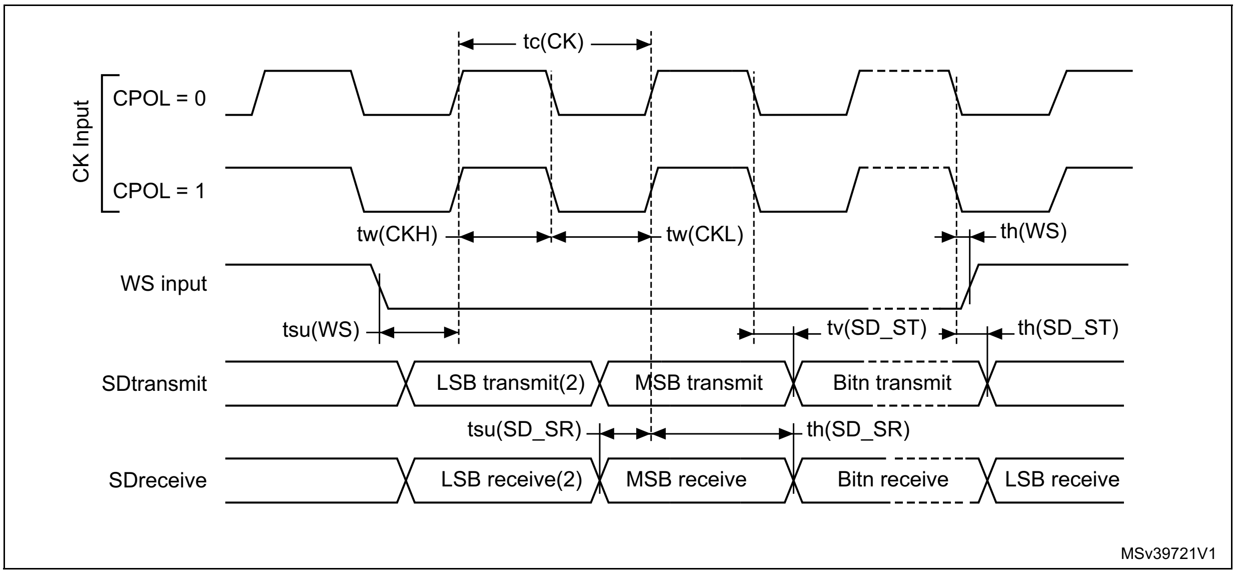
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	V_{DDA} = 3.3 V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12-bit resolution	0.043	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 51* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$

Table 60. I^{2}S characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$[2]	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$[2]		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$[2]	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$[2]		Slave transmitter	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

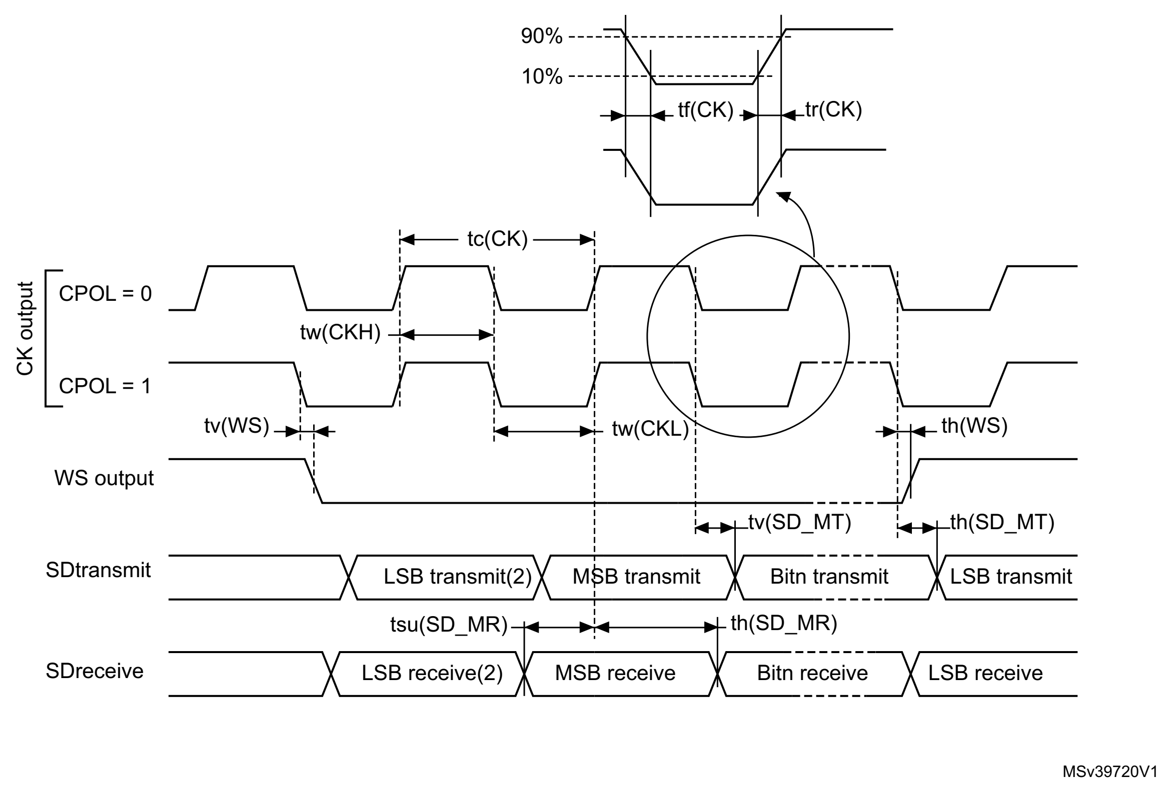
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 29. I^{2}S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 30. I^{2}S master timing diagram (Philips protocol)



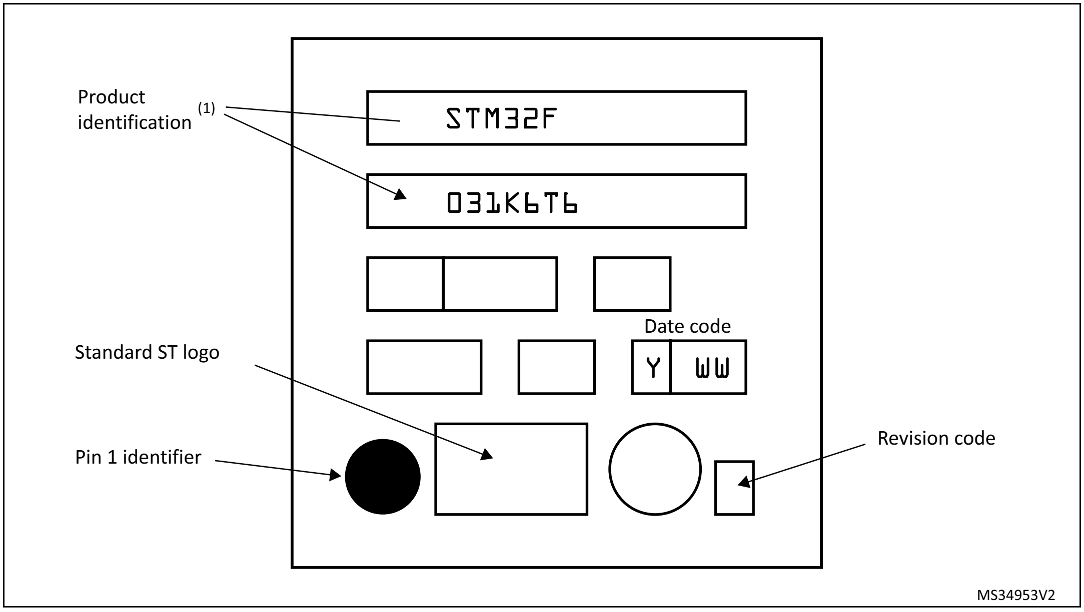
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 36. LQFP32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFQFPN32 package information

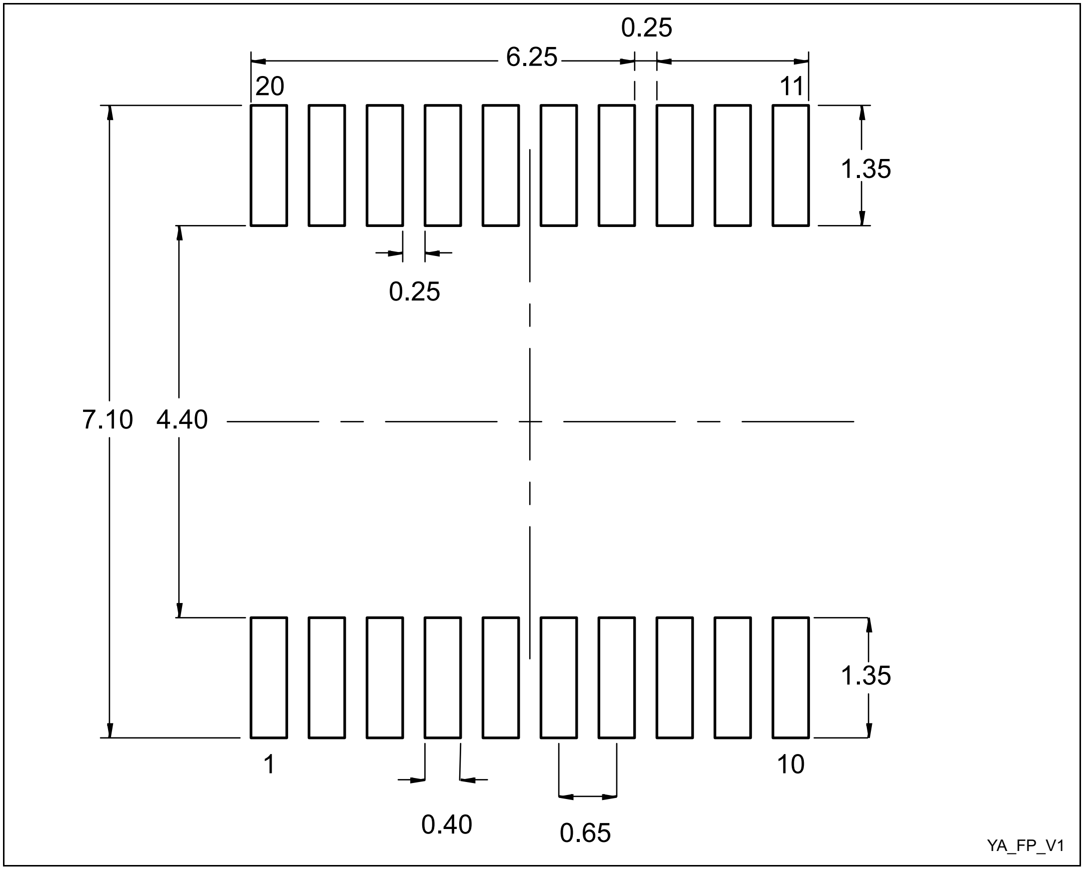
UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.

Table 67. TSSOP20 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 47. Recommended footprint for TSSOP20 package



1. Dimensions are expressed in millimeters.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 69. Ordering information scheme

Example: STM32 F 031 G 6 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

031 = STM32F031xx

Pin count

F = 20 pins
E = 25 pins
G = 28 pins
K = 32 pins
C = 48 pins

User code memory size

4 = 16 Kbyte
6 = 32 Kbyte

Package

P = TSSOP
U = UFQFPN
T = LQFP
Y = WLCSP

Temperature range

6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Options

xxx = code ID of programmed parts (includes packing type)
TR = tape and reel packing
blank = tray packing

Table 70. Document revision history (continued)

Date	Revision	Changes
28-Aug-2015	3 (continued)	Added WLCSP25 package, updates in the following: – *Table 1: Device summary*, – *Section 2: Description*, – *Table 2: STM32F031x4/x6 family device features and peripheral counts*, – *Section 4: Pinouts and pin description*: addition of *Figure 7: WLCSP25 25-ball package ballout (bump side)* and update of *Table 11: Pin definitions*, – *Table 18: General operating conditions*, – *Section 7: Package information* with the addition of *Section 7.5: WLCSP25 package information*, – *Table 68: Package thermal characteristics*.
16-Dec-2015	4	**Cover page:** – number of timers added in the title – *Table 1: Device summary* - STM32F031x4 added ***Section 2: Description*****:** – *Figure 1: Block diagram* updated ***Section 3: Functional overview*****:** – *Figure 2: Clock tree* updated – *Section 3.5.4: Low-power modes* - added explicit inf. on peripherals configurable to operate with HSI – *Section 3.10.2: Internal voltage reference (V_{REFINT})* - removed information on comparators – *Section 3.11.2: General-purpose timers (TIM2, 3, 14, 16, 17)* - number of gen-purpose timers corrected – *Section Table 7.: STM32F031x4/x6 I^{2}C implementation* - added 20mA output drive current ***Section 4: Pinouts and pin description*****:** – Package pinout figures updated (look and feel) – *Figure 7: WLCSP25 package pinout* - **now presented in top view** – *Table 11: Pin definitions* - notes 3 and 6 added ***Section 5: Memory mapping*****:** – added information on memory mapping difference of STM32F031x4 from STM32F031x6 ***Section 6: Electrical characteristics***: – *Table 22: Embedded internal reference voltage*: removed -40°-to-85° condition and associated note for V_{REFINT} – *Table 25* and *Table 26* values rounded to 1 decimal – *Table 46: I/O static characteristics* - removed note – *Table 50: ADC characteristics* - updated some parameter values, test conditions and added footnotes (3) and (4)

Table 70. Document revision history (continued)

Date	Revision	Changes
16-Dec-2015	4 (continued)	– *Section 6.3.16: 12-bit ADC characteristics* - changed introductory sentence – *Table 60: I^{2}S characteristics*: table reorganized, $t_{v(SD\_ST)}$ max value updated ***Section 7: Package information*:** – *Figure 41: Recommended footprint for UFQFPN28 package* updated ***Section 8: Part numbering*:** – added tray packing to options
06-Jan-2017	5	***Section 6: Electrical characteristics*:** – *Table 34: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 22: Embedded internal reference voltage* - V_{REFINT} values – *Figure 26: SPI timing diagram - slave mode and CPHA = 0* and *Figure 27: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information*:** – The name of the section changed from the previous “Part numbering”