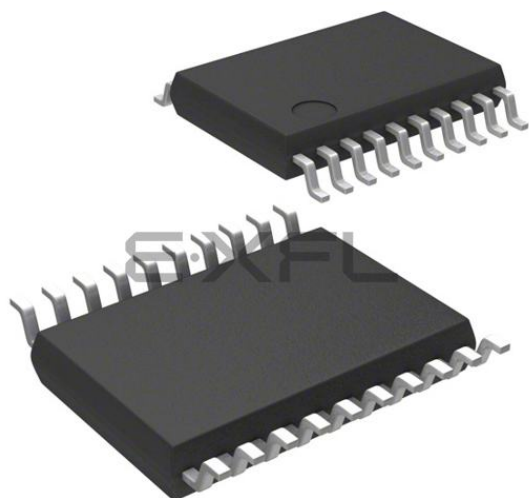




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031f6p7

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1 Introduction

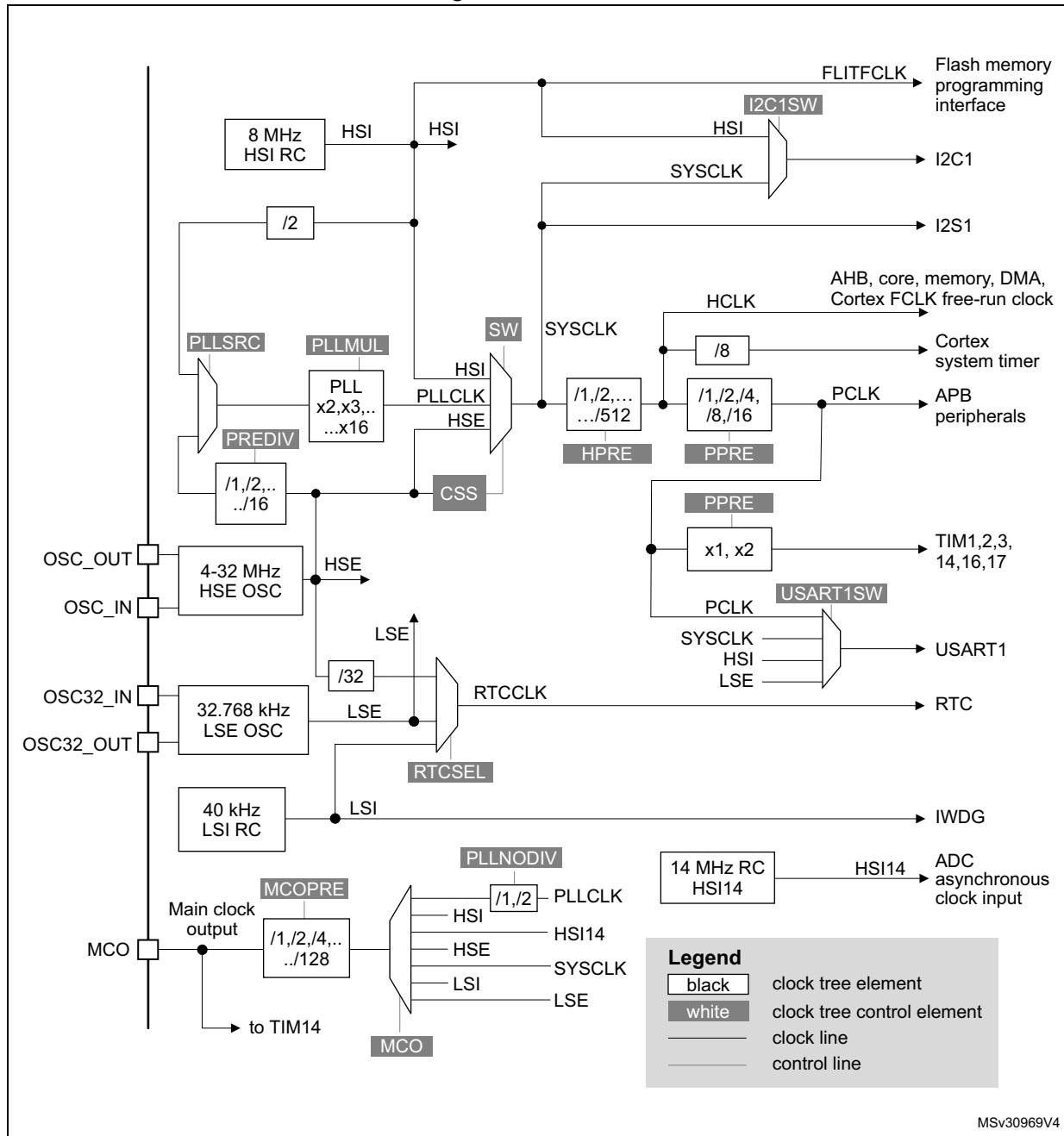
This datasheet provides the ordering information and mechanical device characteristics of the STM32F031x4/x6 microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.



Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.13 Inter-integrated circuit interface (I²C)

The I²C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

Table 11. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
6	3	3	3	B5	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	4	4	4	C5	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	16 (3)	0 ⁽³⁾	16 (3)	E1 (3)	15 (3)	VSSA	S		-	Analog ground	
9	5	5	5	D5	5	VDDA	S		-	Analog power supply	
10	6	6	6	B4	6	PA0	I/O	TTa	-	TIM2_CH1_ETR, USART1_CTS	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	7	C4	7	PA1	I/O	TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS	ADC_IN1
12	8	8	8	D4	8	PA2	I/O	TTa	-	TIM2_CH3, USART1_TX	ADC_IN2
13	9	9	9	E5	9	PA3	I/O	TTa	-	TIM2_CH4, USART1_RX	ADC_IN3
14	10	10	10	B3	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK	ADC_IN4
15	11	11	11	C3	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR	ADC_IN5
16	12	12	12	D3	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6

5 Memory mapping

To the difference of STM32F031x6 memory map in [Figure 9](#), the two bottom code memory spaces of STM32F031x4 end at 0x0000 3FFF and 0x0800 3FFF, respectively.

Figure 9. STM32F031x6 memory map

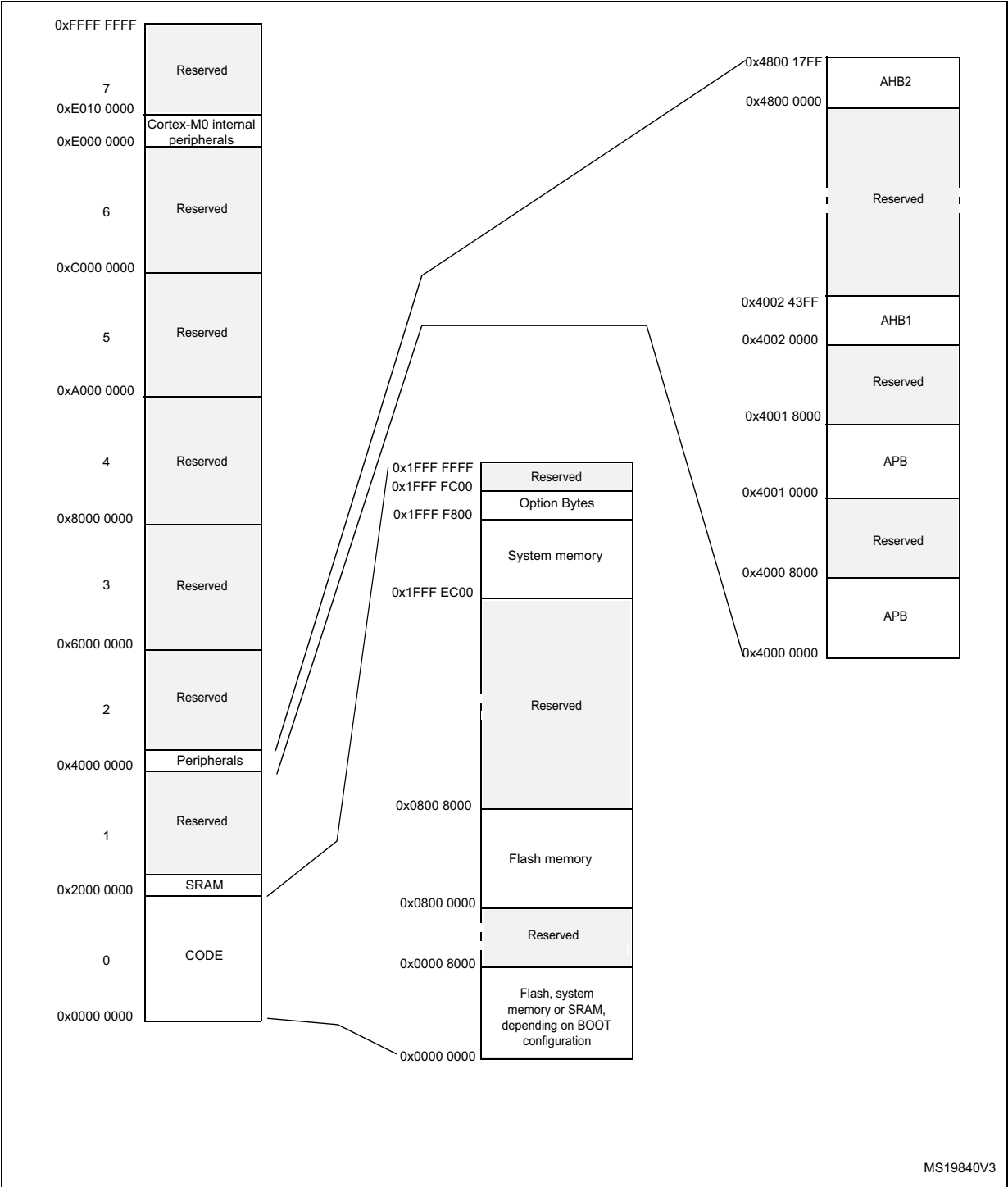


Table 14. STM32F031x4/x6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5800 - 0x4000 6FFF	6KB	Reserved
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 3400 - 0x4000 53FF	8KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

Table 25. Typical and maximum current consumption in Stop and Standby modes

Sym- bol	Para- meter	Conditions	Typ @V _{DD} (V _{DD} = V _{DDA})						Max ⁽¹⁾			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	15	15.1	15.3	15.5	15.7	16	18 ⁽²⁾	38	55 ⁽²⁾	μA
		Regulator in low-power mode, all oscillators OFF	3.2	3.3	3.4	3.5	3.7	4	5.5 ⁽²⁾	22	41 ⁽²⁾	
	Supply current in Standby mode	LSI ON and IWDG ON	0.8	1.0	1.1	1.2	1.4	1.5	-	-	-	
		LSI OFF and IWDG OFF	0.7	0.8	0.9	1.0	1.1	1.3	2 ⁽²⁾	2.5	3 ⁽²⁾	
I _{DDA}	Supply current in Stop mode	V _{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
			Regulator in low-power mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
	Supply current in Standby mode	V _{DDA} monitoring ON	LSI ON and IWDG ON	2.3	2.5	2.7	2.9	3.1	3.3	-	-	-
			LSI OFF and IWDG OFF	1.8	1.9	2	2.2	2.3	2.5	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
	Supply current in Stop mode	V _{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-
			Regulator in low-power mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-
	Supply current in Standby mode	V _{DDA} monitoring OFF	LSI ON and IWDG ON	1.5	1.6	1.7	1.8	1.9	2.0	-	-	-
			LSI OFF and IWDG OFF	1	1.0	1.1	1.1	1.2	1.2	-	-	-

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 29: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

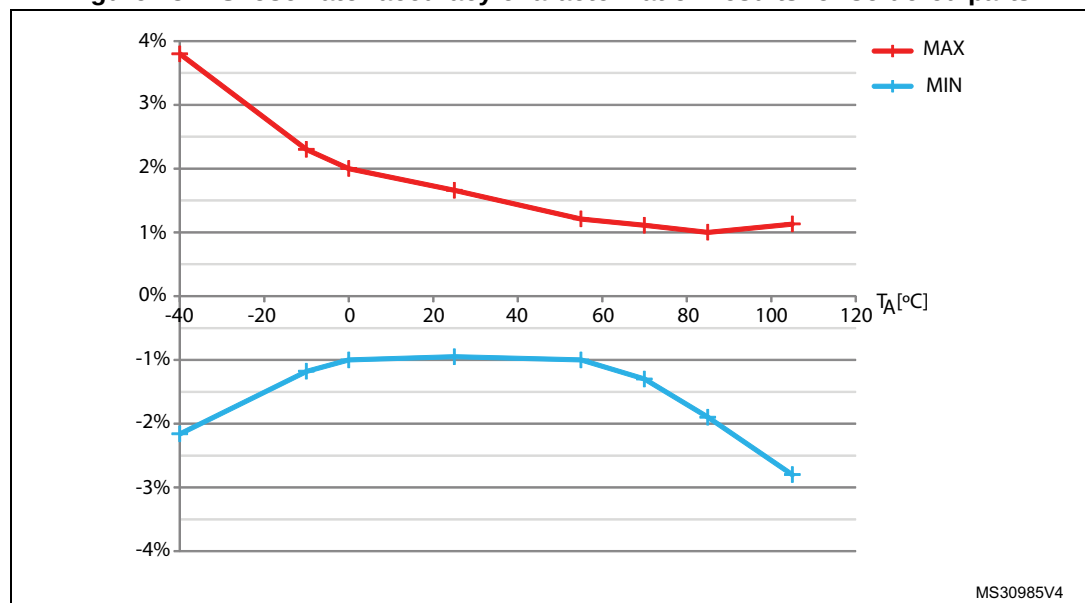
High-speed internal (HSI) RC oscillator

Table 35. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC _{HSI}	Accuracy of the HSI oscillator	$T_A = -40$ to 105°C	-2.8 ⁽³⁾	-	3.8 ⁽³⁾	%
		$T_A = -10$ to 85°C	-1.9 ⁽³⁾	-	2.3 ⁽³⁾	
		$T_A = 0$ to 85°C	-1.9 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 0$ to 70°C	-1.3 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 0$ to 55°C	-1 ⁽³⁾	-	2 ⁽³⁾	
		$T_A = 25^\circ\text{C}$ ⁽⁴⁾	-1	-	1	
$t_{\text{su(HSI)}}$	HSI oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
$I_{\text{DDA(HSI)}}$	HSI oscillator power consumption	-	-	80	100 ⁽²⁾	μA

1. $V_{\text{DDA}} = 3.3\text{ V}$, $T_A = -40$ to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 18. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 37. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DDA(LSI)}^{(2)}$	LSI oscillator power consumption	-	0.75	1.2	μ A

1. $V_{DDA} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in [Table 38](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 18: General operating conditions](#).

Table 38. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f_{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μ s
Jitter _{PLL}	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT} .

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
t_{prog}	16-bit programming time	$T_A = -40$ to $+105$ °C	40	53.5	60	μ s
t_{ERASE}	Page (1 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 46. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽³⁾	$V_{IN} = -V_{DDIOx}$	25	40	55	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 45: I/O current injection susceptibility](#).
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 20](#) for standard I/Os, and in [Figure 21](#) for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 20. TC and TTa I/O input characteristics

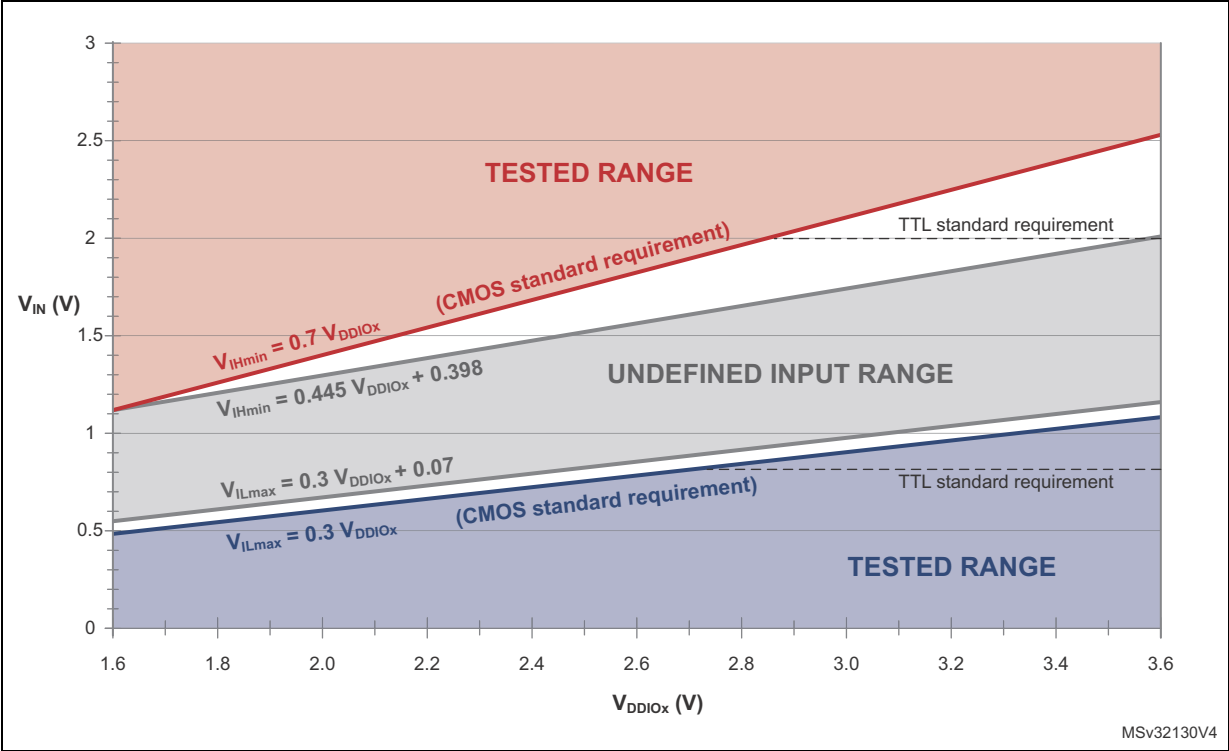
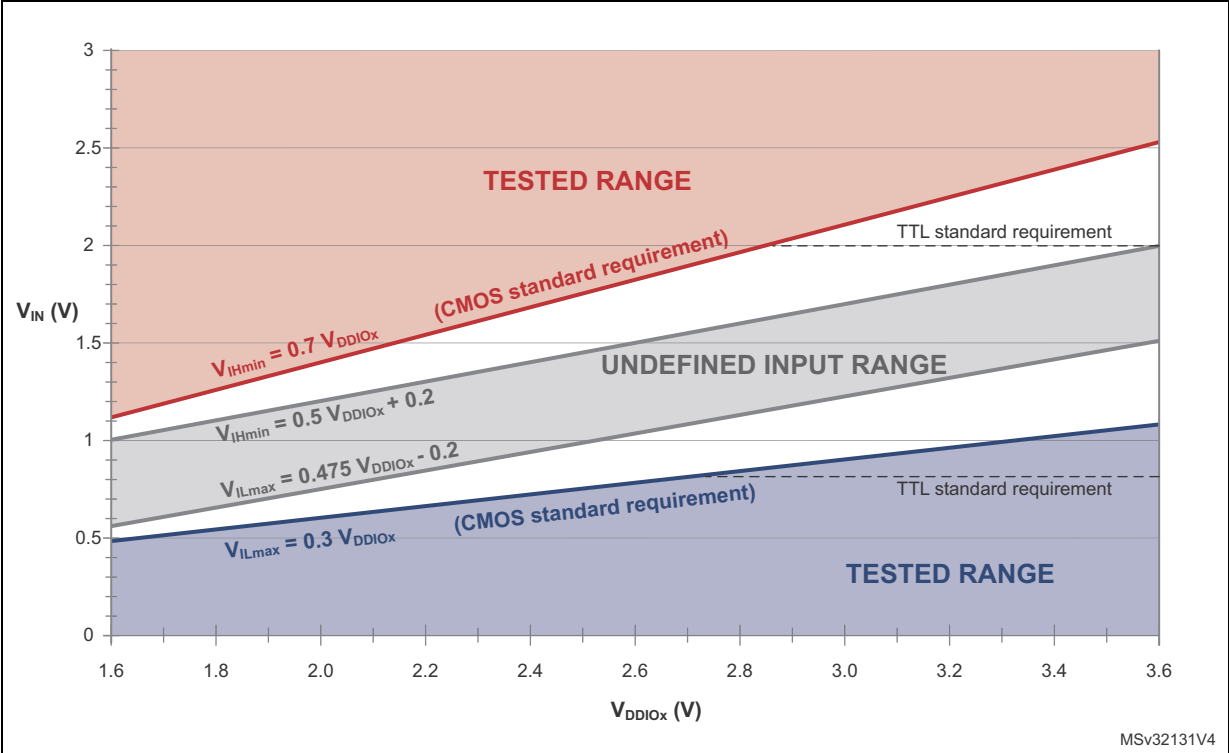


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/- 8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 15: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 15: Voltage characteristics](#)).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 18: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 47. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 6 \text{ mA}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
$V_{OLFm+}^{(3)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
		$ I_{IO} = 10 \text{ mA}$	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 15: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.

Table 51. R_{AIN} max for $f_{ADC} = 14$ MHz (continued)

T_s (cycles)	t_s (μs)	R_{AIN} max (k Ω) ⁽¹⁾
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 52. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽⁴⁾	Unit
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ k Ω $V_{DDA} = 3$ V to 3.6 V $T_A = 25$ °C	± 1.3	± 2	LSB
EO	Offset error		± 1	± 1.5	
EG	Gain error		± 0.5	± 1.5	
ED	Differential linearity error		± 0.7	± 1	
EL	Integral linearity error		± 0.8	± 1.5	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ k Ω $V_{DDA} = 2.7$ V to 3.6 V $T_A = -40$ to 105 °C	± 3.3	± 4	LSB
EO	Offset error		± 1.9	± 2.8	
EG	Gain error		± 2.8	± 3	
ED	Differential linearity error		± 0.7	± 1.3	
EL	Integral linearity error		± 1.2	± 1.7	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ k Ω $V_{DDA} = 2.4$ V to 3.6 V $T_A = 25$ °C	± 3.3	± 4	LSB
EO	Offset error		± 1.9	± 2.8	
EG	Gain error		± 2.8	± 3	
ED	Differential linearity error		± 0.7	± 1.3	
EL	Integral linearity error		± 1.2	± 1.7	

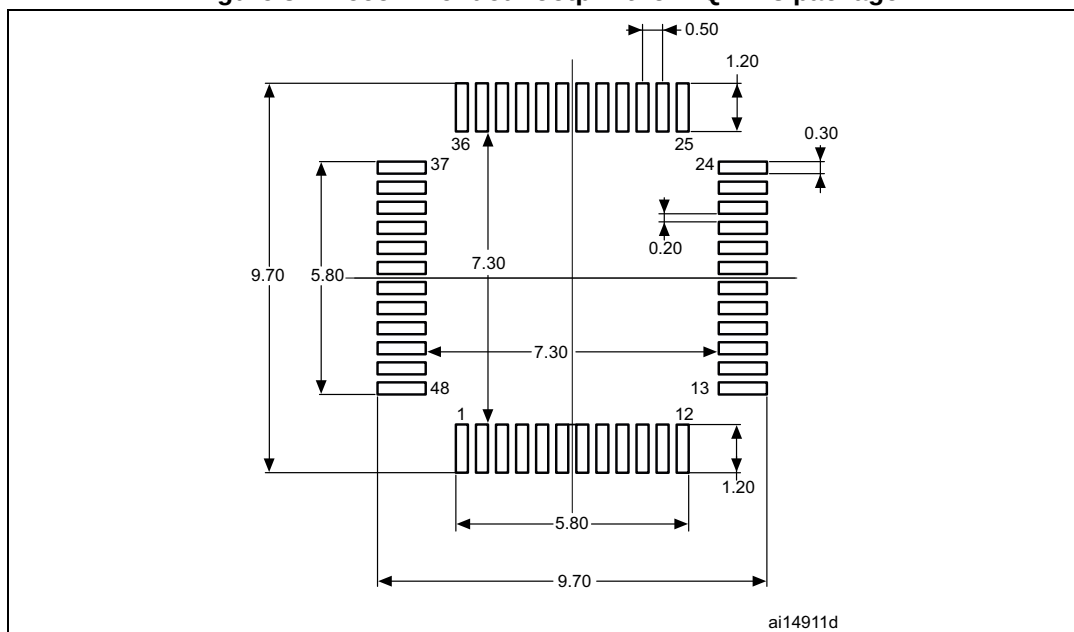
- ADC DC accuracy values are measured after internal calibration.
- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.14](#) does not affect the ADC accuracy.
- Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
- Data based on characterization results, not tested in production.

Table 61. LQFP48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. Recommended footprint for LQFP48 package



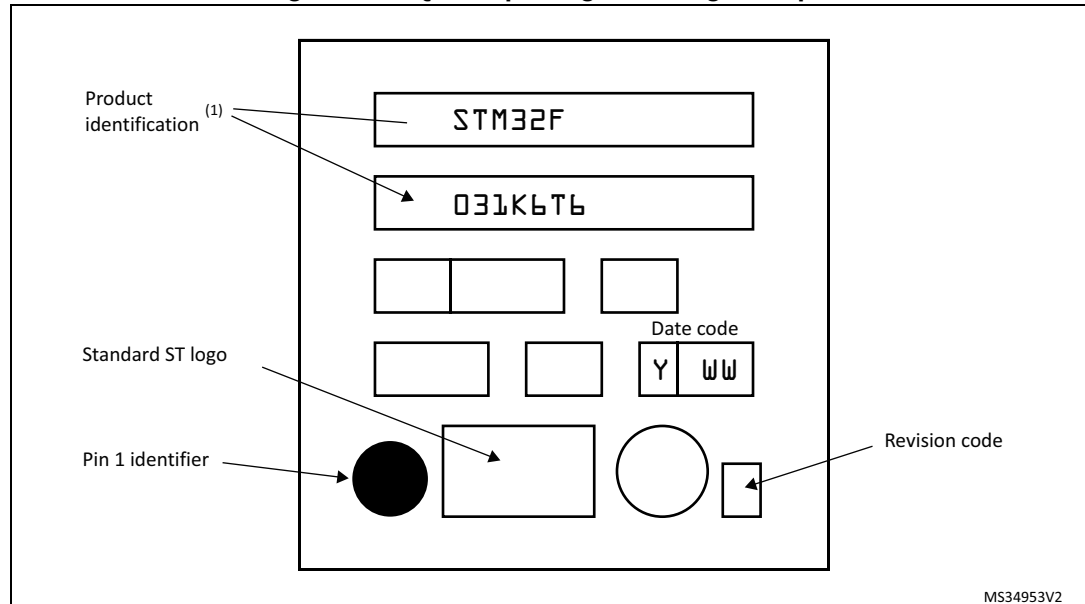
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 36. LQFP32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFQFPN32 package information

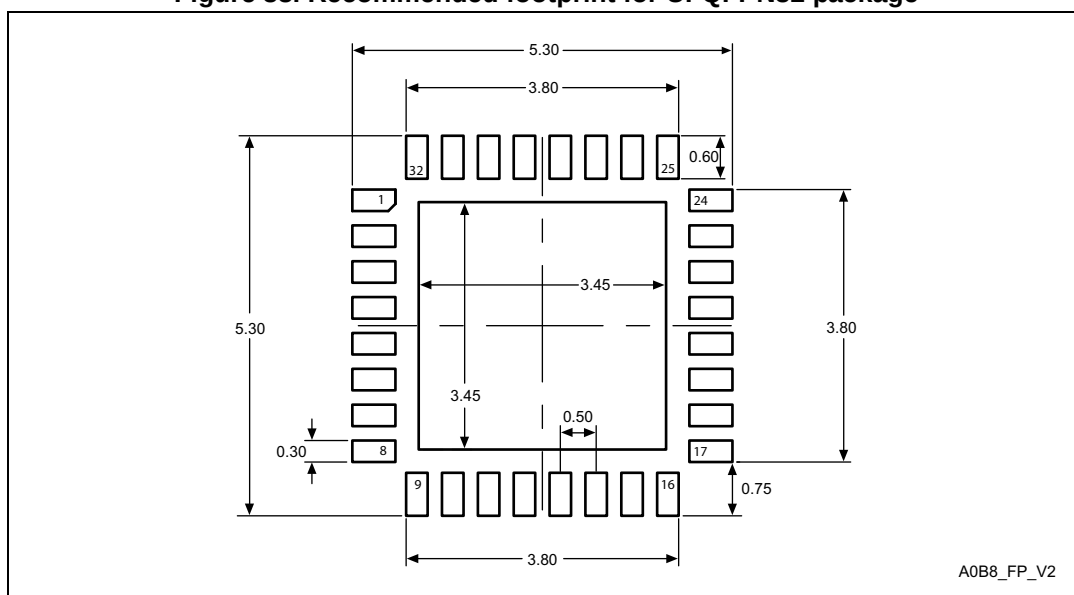
UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.

Table 63. UFQFPN32 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for UFQFPN32 package

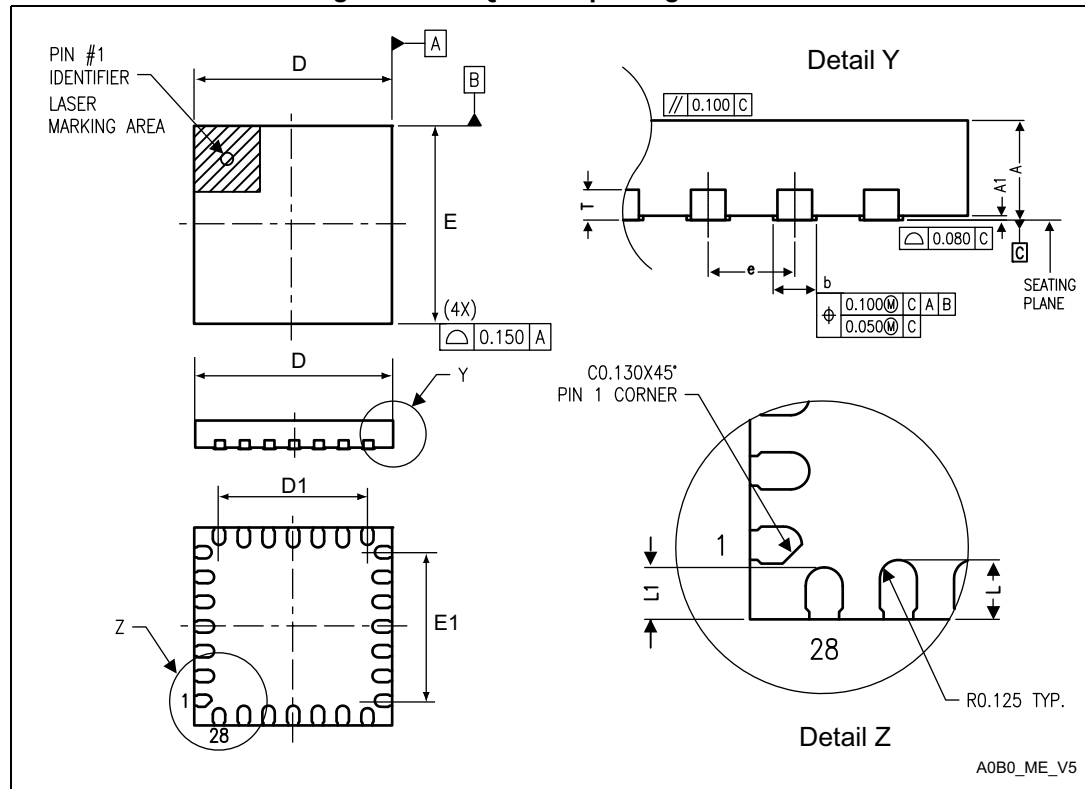


1. Dimensions are expressed in millimeters.

7.4 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 40. UFQFPN28 package outline



1. Drawing is not to scale.

Table 64. UFQFPN28 package mechanical data⁽¹⁾

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-