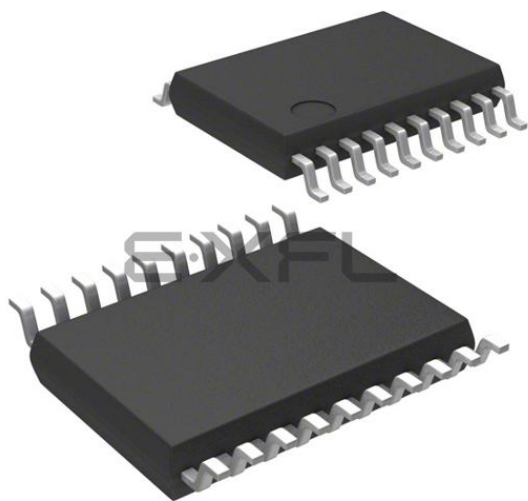




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031f6p7tr

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2 Description

The STM32F031x4/x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 4 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I²C, one SPI/ I²S and one USART), one 12-bit ADC, five 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F031x4/x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F031x4/x6 microcontrollers include devices in six different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F031x4/x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Table 2. STM32F031x4/x6 family device features and peripheral counts

Peripheral		STM32F031Fx		STM32F031Ex	STM32F031Gx		STM32F031Kx		STM32F031Cx	
Flash memory (Kbyte)		16	32	32	16	32	16	32	16	32
SRAM (Kbyte)		4								
Timers	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32-bit)								
Comm. interfaces	SPI [I ² S] ⁽¹⁾	1 [1]								
	I ² C	1								
	USART	1								
12-bit ADC (number of channels)		1 (9 ext. + 3 int.)	1 (10 ext. + 3 int.)							
GPIOs		15	20	23	25 (on LQFP32) 27 (on UFQFPN32)		39			
Max. CPU frequency		48 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperature		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C								
Packages		TSSOP20		WLCSP25	UFQFPN28		LQFP32 UFQFPN32		LQFP48	

1. The SPI interface can be used either in SPI mode or in I²S audio mode.

3 Functional overview

Figure 1 shows the general block diagram of the STM32F031x4/x6 devices.

3.1 ARM[®]-Cortex[®]-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F031x4/x6 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - 16 to 32 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

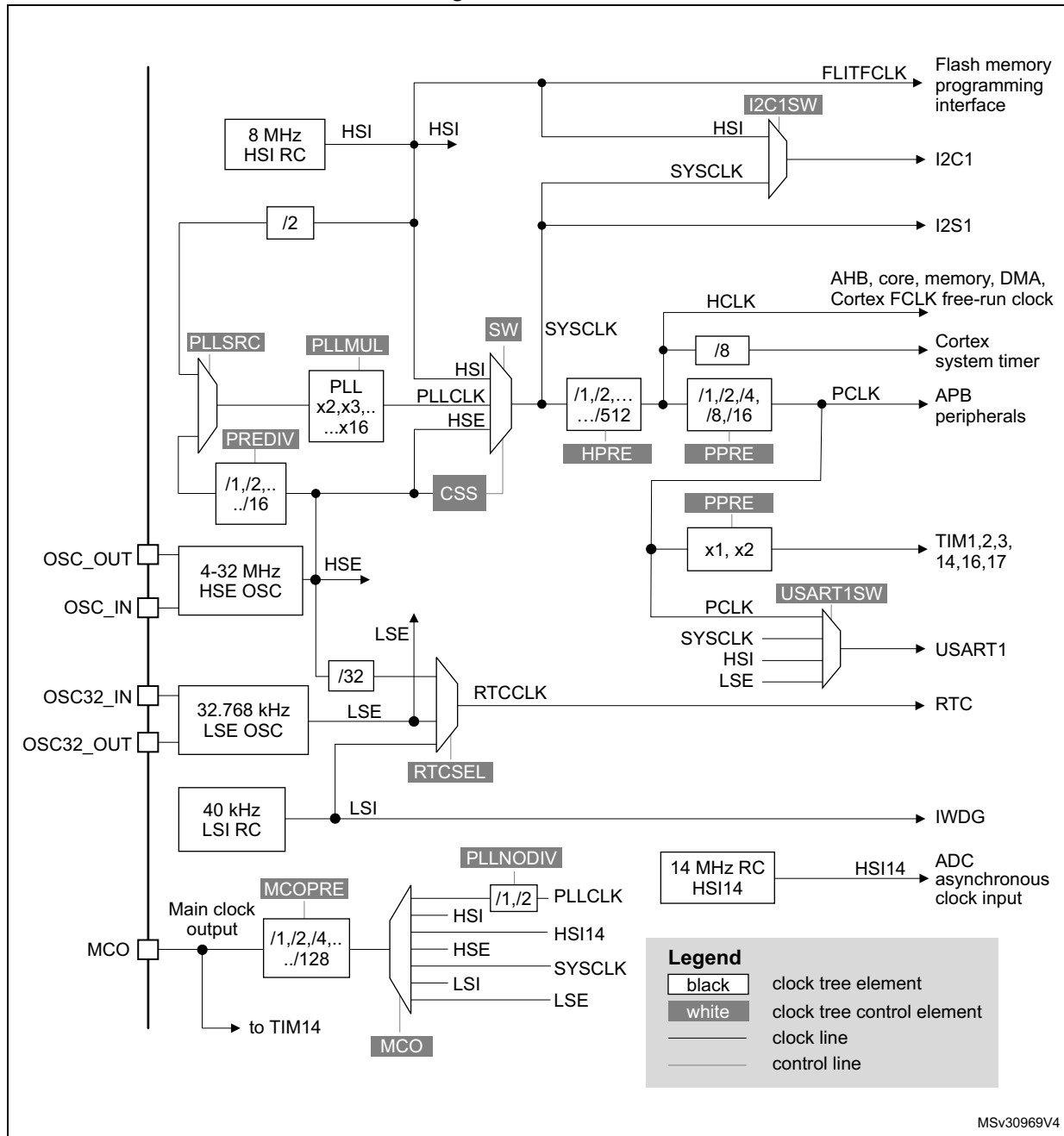
3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.11 Timers and watchdogs

The STM32F031x4/x6 devices include up to five general-purpose timers and an advanced control timer.

[Table 5](#) compares the features of the different timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.11.2 General-purpose timers (TIM2, 3, 14, 16, 17)

There are five synchronizable general-purpose timers embedded in the STM32F031x4/x6 devices (see [Table 5](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

Table 6. Comparison of I²C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripheral can be served by the DMA controller.

Table 7. STM32F031x4/x6 I²C implementation

I ² C features ⁽¹⁾	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds one universal synchronous/asynchronous receiver/transmitter (USART1) which communicates at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin description

Figure 3. LQFP48 package pinout

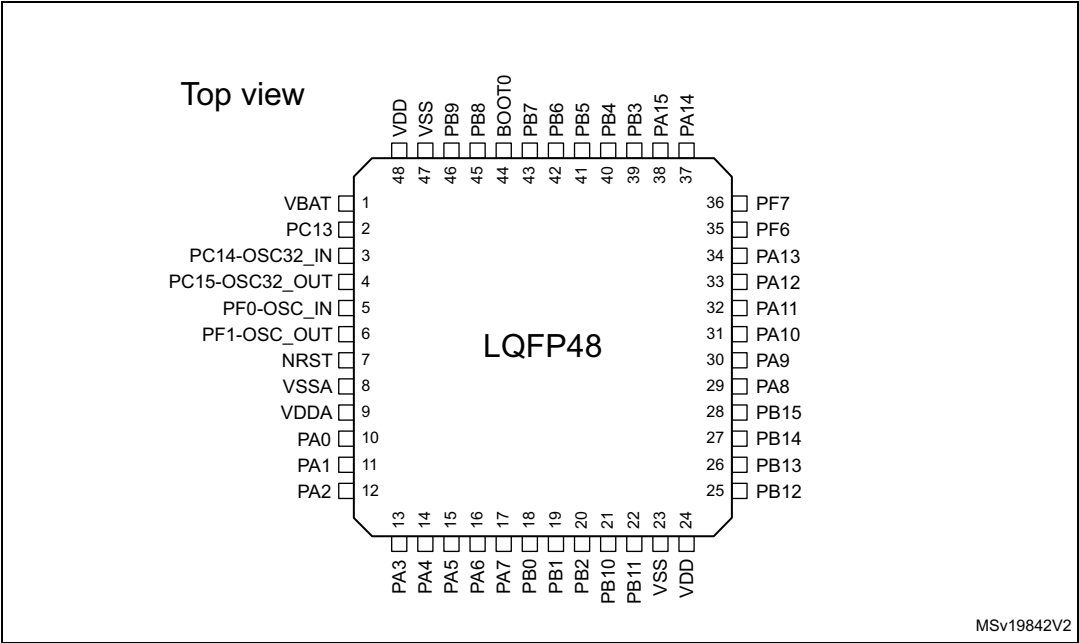


Figure 4. LQFP32 package pinout

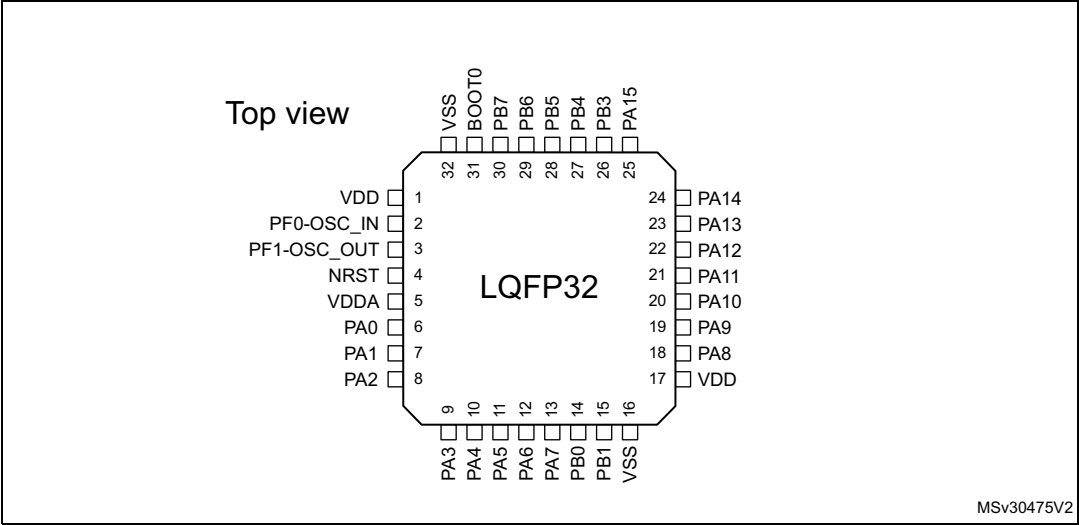


Table 11. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
30	19	19	19	C1	17	PA9	I/O	FTf	-	USART1_TX, TIM1_CH2, I2C1_SCL	-
31	20	20	20	B1	18	PA10	I/O	FTf	-	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA	-
32	21	21	-	-	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT	-
33	22	22	-	-	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT	-
34	23	23	21	A1	19	PA13 (SWDIO)	I/O	FT	(5)	IR_OUT, SWDIO	-
35	-	-	-	-	-	PF6	I/O	FTf	-	I2C1_SCL	-
36	-	-	-	-	-	PF7	I/O	FTf	-	I2C1_SDA	-
37	24	24	22	A2	20	PA14 (SWCLK)	I/O	FT	(5)	USART1_TX, SWCLK	-
38	25	25	23	-	-	PA15	I/O	FT	(6)	SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX	-
39	26	26	24	-	-	PB3	I/O	FT	(6)	SPI1_SCK, I2S1_CK, TIM2_CH2, EVENTOUT	-
40	27	27	25	-	-	PB4	I/O	FT	(6)	SPI1_MISO, I2S1_MCK, TIM3_CH1, EVENTOUT	-

Table 14. STM32F031x4/x6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5800 - 0x4000 6FFF	6KB	Reserved
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 3400 - 0x4000 53FF	8KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 36. HSI14 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI14)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC _{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$	-4.2 ⁽³⁾	-	5.1 ⁽³⁾	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}$	-3.2 ⁽³⁾	-	3.1 ⁽³⁾	%
		$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	-2.5 ⁽³⁾	-	2.3 ⁽³⁾	%
		$T_A = 25 \text{ }^\circ\text{C}$	-1	-	1	%
$t_{\text{su(HSI14)}}$	HSI14 oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
$I_{\text{DDA(HSI14)}}$	HSI14 oscillator power consumption	-	-	100	150 ⁽²⁾	μA

1. $V_{\text{DDA}} = 3.3 \text{ V}$, $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$ unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 19. HSI14 oscillator accuracy characterization results

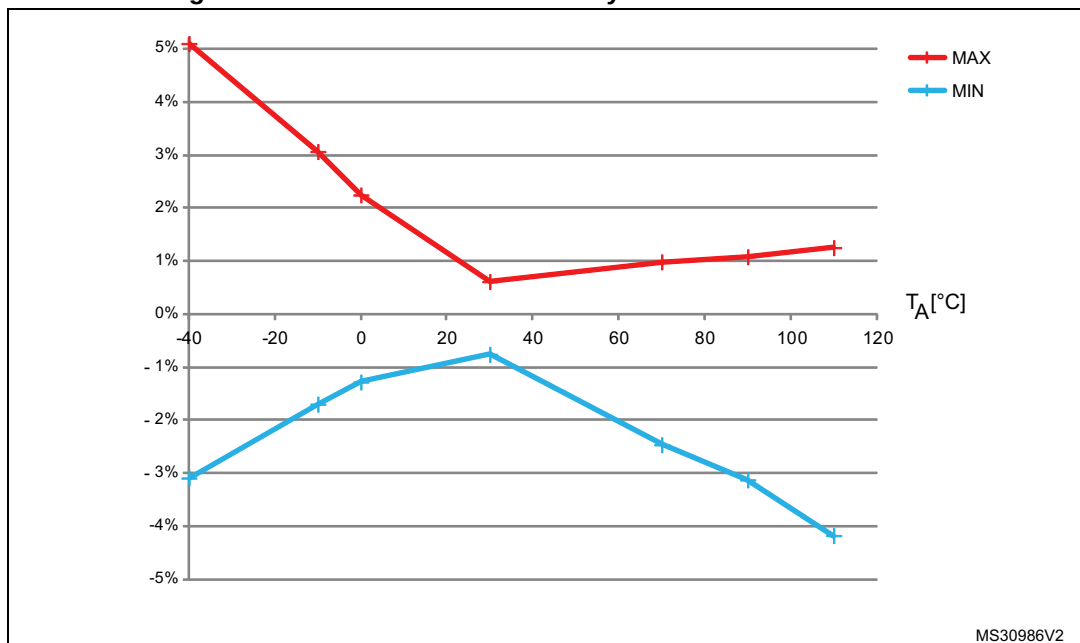


Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT and FTf pins	–5	NA	
	Injected current on all TTa, TC and RESET pins	–5	+5	

6.3.14 I/O port characteristics

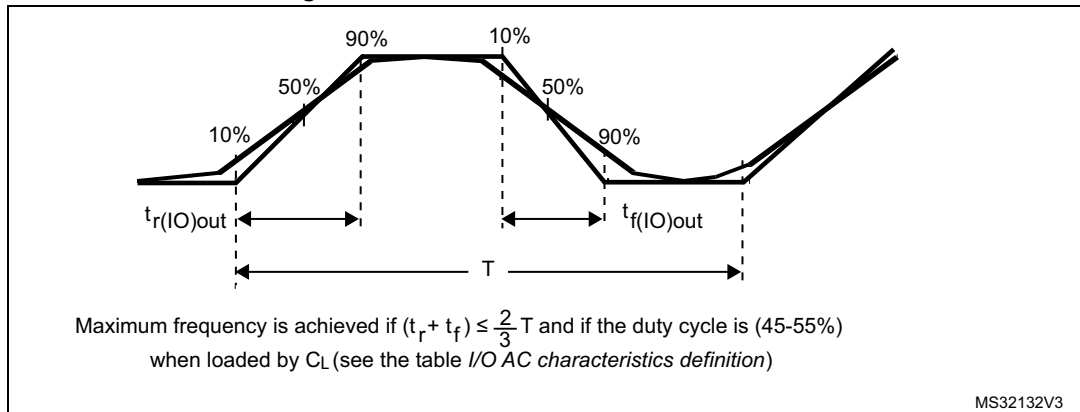
General input/output characteristics

Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under the conditions summarized in [Table 18: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DDIOx} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DDIOx} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DDIOx} - 0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3 V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 V_{DDIOx} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DDIOx} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DDIOx} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7 V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	
I_{lkg}	Input leakage current ⁽²⁾	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	± 0.1	μA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \leq V_{IN} \leq 5 V$	-	-	10	

Figure 22. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 18: General operating conditions](#).

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 V_{DD} + 0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445 V_{DD} + 0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_F(NRST)$	NRST input filtered pulse	-	-	-	$100^{(1)}$	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	$300^{(3)}$	-	-	ns
		$2.0 < V_{DD} < 3.6$	$500^{(3)}$	-	-	

1. Data based on design simulation only. Not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

3. Data based on design simulation only. Not tested in production.

Table 50. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$W_{\text{LATENCY}}^{(2)(4)}$	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
$t_{\text{latr}}^{(2)}$	Trigger conversion latency	$f_{\text{ADC}} = f_{\text{PCLK}}/2 = 14 \text{ MHz}$	0.196			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/2$	5.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{PCLK}}/4 = 12 \text{ MHz}$	0.219			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/4$	10.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{HSI14}} = 14 \text{ MHz}$	0.179	-	0.250	μs
$\text{Jitter}_{\text{ADC}}$	ADC jitter on trigger conversion	$f_{\text{ADC}} = f_{\text{HSI14}}$	-	1	-	$1/f_{\text{HSI14}}$
$t_{\text{S}}^{(2)}$	Sampling time	$f_{\text{ADC}} = 14 \text{ MHz}$	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{\text{ADC}}$
$t_{\text{STAB}}^{(2)}$	Stabilization time	-	14			$1/f_{\text{ADC}}$
$t_{\text{CONV}}^{(2)}$	Total conversion time (including sampling time)	$f_{\text{ADC}} = 14 \text{ MHz}$, 12-bit resolution	1	-	18	μs
		12-bit resolution	14 to 252 (t_{S} for sampling + 12.5 for successive approximation)			$1/f_{\text{ADC}}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I_{DDA} and 60 μA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

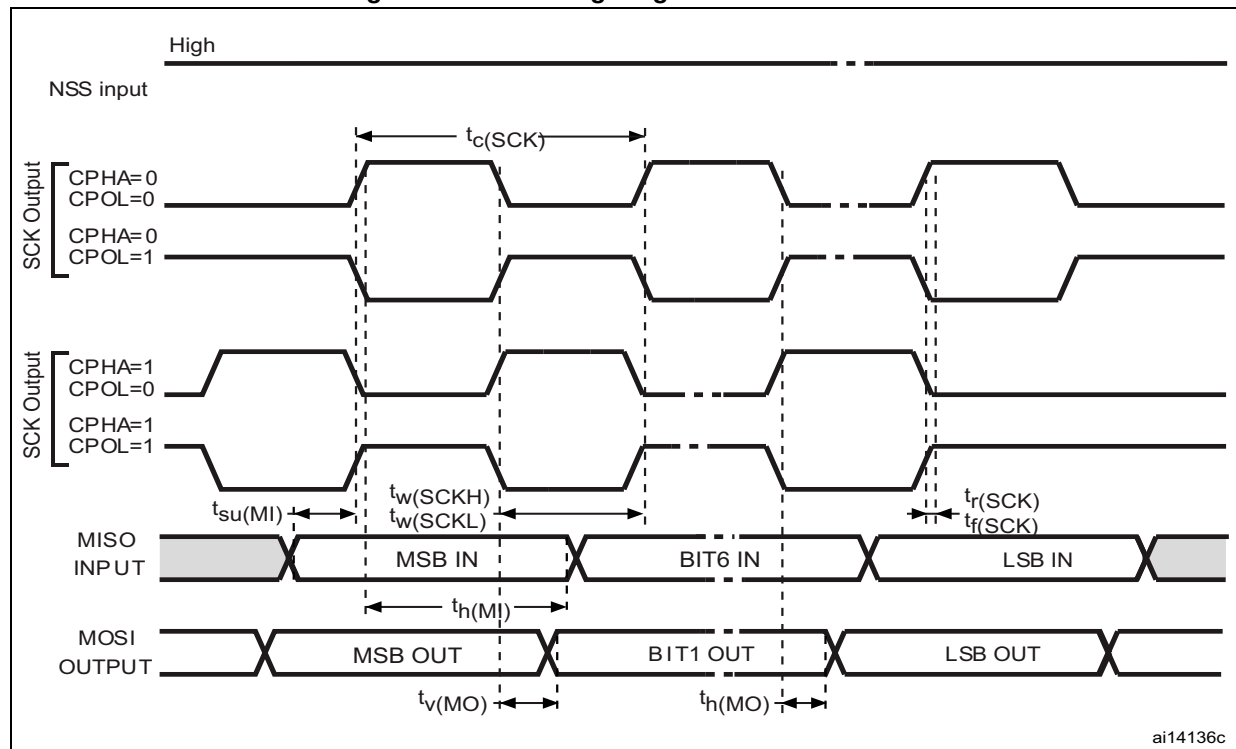
$$R_{\text{AIN}} < \frac{T_{\text{S}}}{f_{\text{ADC}} \times C_{\text{ADC}} \times \ln(2^{N+2})} - R_{\text{ADC}}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here $N = 12$ (from 12-bit resolution).

Table 51. R_{AIN} max for $f_{\text{ADC}} = 14 \text{ MHz}$

T_{S} (cycles)	t_{S} (μs)	R_{AIN} max ($\text{k}\Omega$) ⁽¹⁾
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

Figure 28. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

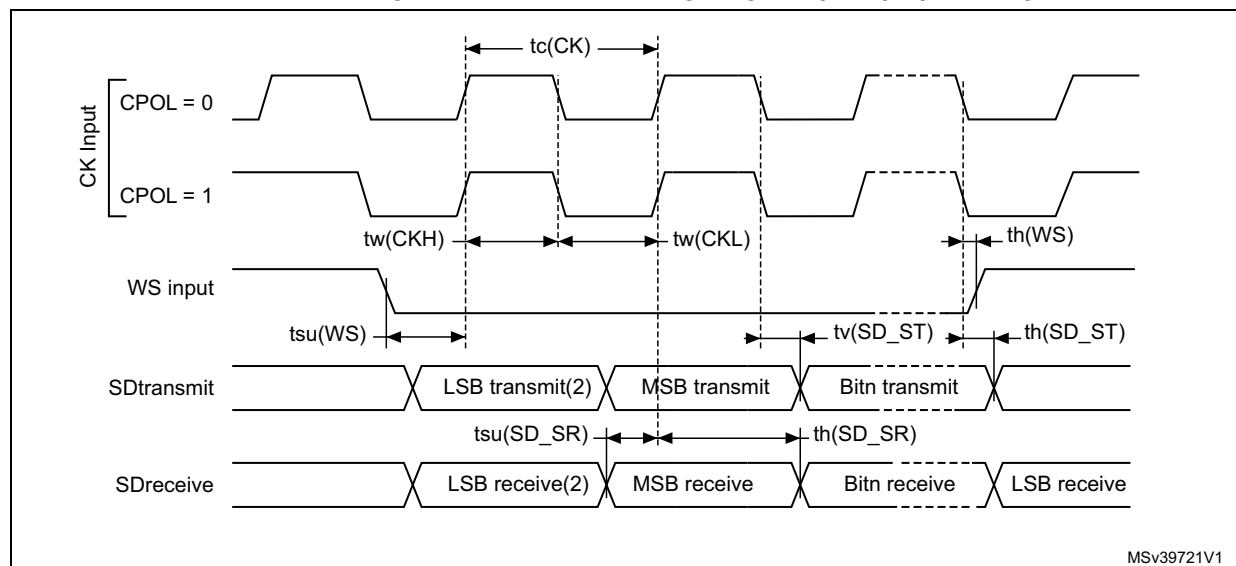
Table 60. I²S characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I ² S clock rise time	Capacitive load $C_L = 15$ pF	-	10	ns
$t_{f(CK)}$	I ² S clock fall time		-	12	
$t_{w(CKH)}$	I ² S clock high time	Master $f_{PCLK} = 16$ MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I ² S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I ² S slave input clock duty cycle	Slave mode	25	75	%

Table 60. I²S characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su}(SD_MR)$	Data input setup time	Master receiver	6	-	ns
$t_{su}(SD_SR)$		Slave receiver	2	-	
$t_h(SD_MR)^{(2)}$	Data input hold time	Master receiver	4	-	
$t_h(SD_SR)^{(2)}$		Slave receiver	0.5	-	
$t_v(SD_MT)^{(2)}$	Data output valid time	Master transmitter	-	4	
$t_v(SD_ST)^{(2)}$		Slave transmitter	-	20	
$t_h(SD_MT)$	Data output hold time	Master transmitter	0	-	
$t_h(SD_ST)$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

Figure 29. I²S slave timing diagram (Philips protocol)

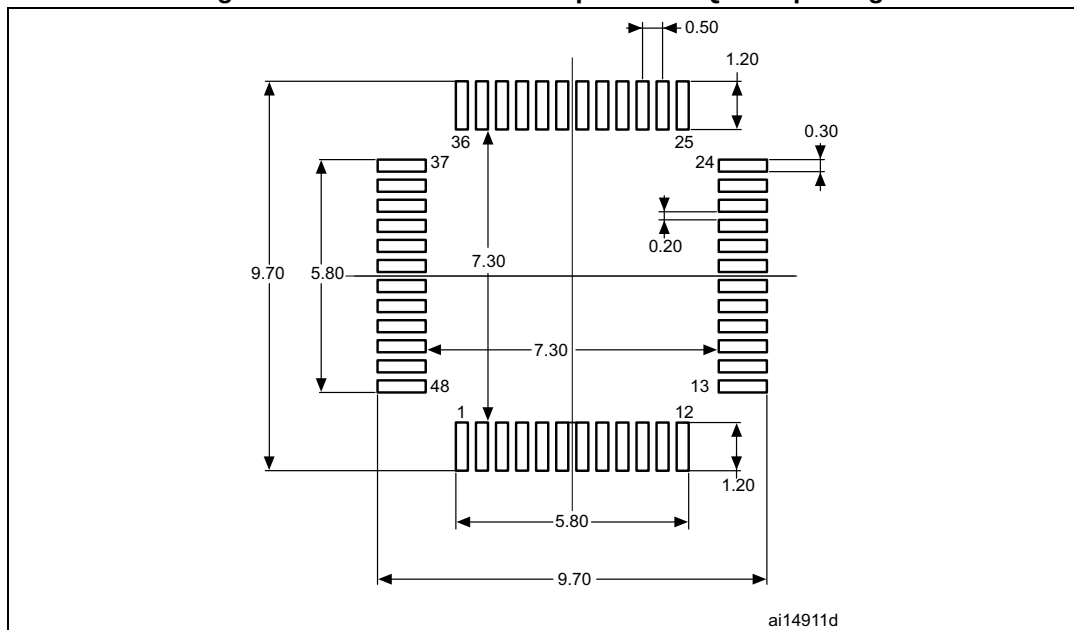
1. Measurement points are done at CMOS levels: $0.3 \times V_{DDIOx}$ and $0.7 \times V_{DDIOx}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 61. LQFP48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. Recommended footprint for LQFP48 package

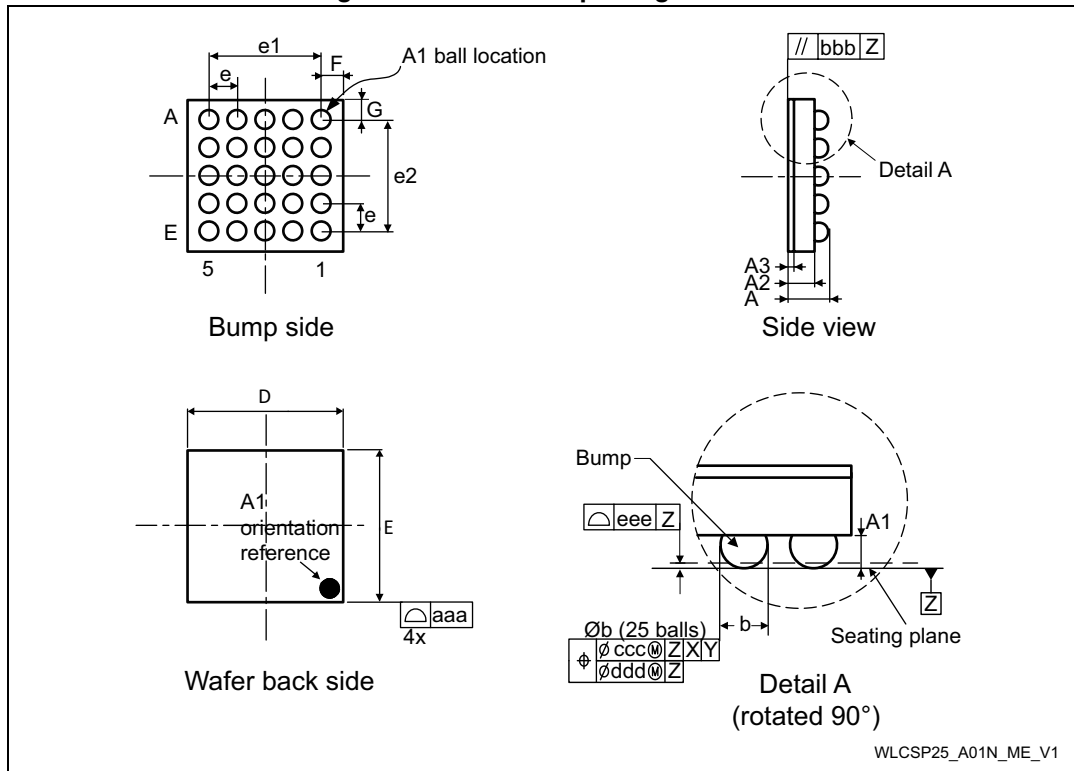


1. Dimensions are expressed in millimeters.

7.5 WLCSP25 package information

WLCSP25 is a 25-ball, 2.423 x 2.325 mm, 0.4 mm pitch wafer level chip scale package.

Figure 43. WLCSP25 package outline



1. Drawing is not to scale.

Table 65. WLCSP25 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ^{(3) (4)}	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.388	2.423	2.458	0.0940	0.0954	0.0968
E	2.29	2.325	2.36	0.0902	0.0915	0.0929
e	-	0.400	-	-	0.0157	-
e1	-	1.600	-	-	0.0630	-
e2	-	1.600	-	-	0.0630	-
F	-	0.4115	-	-	0.0162	-
G	-	0.3625	-	-	0.0143	-

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

[illegible]