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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031g4u7tr

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F031x4/x6 microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M0 core, please refer to the Cortex[®]-M0 Technical Reference Manual, available from the www.arm.com website.



SWCLK SWDIO as AF POWER Serial Wire Debug V_{DD} = 2 to 3.6 V V_{SS} VOLT.REG 3.3 V to 1.8 V ldo Flash GPL Flash Ol memory interface Up to 32 KB CORTEX-M0 CPU 32-bit f_{MAX} = 48 MHz SUPPLY SUPERVISION POR ◀ NRST SRAM 4 KB SRAM controller matrix Reset ◀ $V_{DDA} \ V_{SSA}$ POR/PDR Int 🗲 NVIC Bus HSI14 PVD RC 14 MHz HSI RC 8 MHz **♦** @ V_{DD} PLLCLK PLL LSI RC 40 kHz GP DMA 5 channels XTAL OSC 4-32 MHz OSC_IN OSC_OUT Ind. Window WDG RESET & CLOCK CONTROL ₹. PA[15:0] GPIO port A V_{BAT} = 1.65 to 3.6 V @ V_{BAT} OSC32_IN OSC32_OUT GPIO port B AHB decoder System and peripheral clocks XTAL32 kHz PB[15:0] 1 TAMPER-RTC (ALARM OUT) PC[15:13] GPIO port C Backup RTC reg PF[7:6,1:0] < GPIO port F CRC RTC interface 4 channels 3 compl. channels BRK, ETR input as AF PWM TIMER 1 AHB 4 ch., ETR as AF APB TIMER 2 32-bit 4 ch., ETR as AF TIMER 3 EXT. IT WKUP 39 AF TIMER 14 1 channel as AF MOSI/SD 1 channel TIMER 16 1 compl, BRK as AF MISO/MCK SCK/CK NSS/WS as AF SPI1/I2S1 Window WDG 1 channel 1 compl, BRK as AF TIMER 17 → IR_OUT as AF DBGMCU Temp. sensor 10x SYSCFG IF 12-bit ADC RX, TX,CTS, RTS, CK as AF AD input USART1 V_{DDA} V_{SSA} SCL, SDA, SMBA (20 mA FM+) as AF I2C1 @ V_{DDA} Power domain of analog blocks : V_{DDA} V_{BAT} V_{DD} MSv30246V4

Figure 1. Block diagram



4 Pinouts and pin description

Figure 3. LQFP48 package pinout

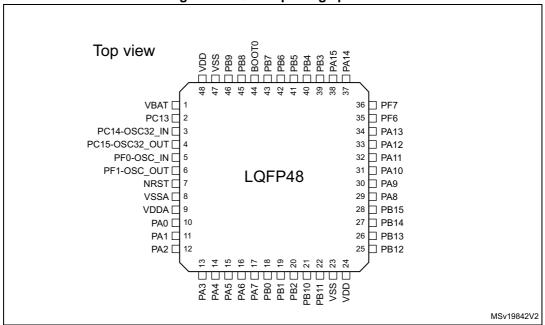


Figure 4. LQFP32 package pinout

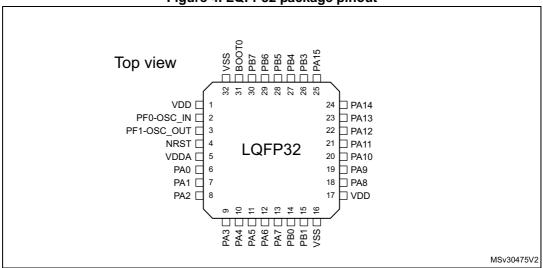


Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-
PB2	-	-	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	-
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-
PB8	-	I2C1_SCL	TIM16_CH1	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	-	I2C1_SCL	TIM2_CH3	-
PB11	EVENTOUT	I2C1_SDA	TIM2_CH4	-
PB12	SPI1_NSS	EVENTOUT	TIM1_BKIN	-
PB13	SPI1_SCK	-	TIM1_CH1N	-
PB14	SPI1_MISO	-	TIM1_CH2N	-
PB15	SPI1_MOSI	-	TIM1_CH3N	-

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	
ΣI _{VSS}	Total current out of sum of all VSS ground lines (sink) ⁽¹⁾	-120	
I _{VDD(PIN)}	Maximum current into each VDD power pin (source) ⁽¹⁾	100	
I _{VSS(PIN)}	Maximum current out of each VSS ground pin (sink) ⁽¹⁾	-100	
	Output current sunk by any I/O and control pin	25	
I _{IO(PIN)}	Output current source by any I/O and control pin	-25	
71	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
$\Sigma I_{IO(PIN)}$	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	mA
	Injected current on B, FT and FTf pins	-5/+0 ⁽⁴⁾	
$I_{INJ(PIN)}^{(3)}$	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	1
ΣΙ _{ΙΝJ(PIN)}	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

- All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the
 permitted range.
- 2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
- 3. A positive injection is induced by V_{IN} > V_{DDIOx} while a negative injection is induced by V_{IN} < V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 15: Voltage characteristics* for the maximum allowed input voltage values.
- 4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
- On these I/Os, a positive injection is induced by V_{IN} > V_{DDA}. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below *Table 52: ADC accuracy*.
- When several inputs are submitted to a current injection, the maximum ΣI_{INJ(PIN)} is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C



Table 25. Typical and maximum current consumption in Stop and Standby modes

Sum	Para-				Typ @V _{DD} (V _{DD} = V _{DDA})					Max ⁽¹⁾)					
Sym- bol			Conditions		2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Unit			
	Supply current		gulator in run de, all oscillators F	15	15.1	15.3	15.5	15.7	16	18 ⁽²⁾	38	55 ⁽²⁾				
I _{DD}	in Stop mode	Regulator in low- power mode, all oscillators OFF		3.2	3.3	3.4	3.5	3.7	4	5.5 ⁽²⁾	22	41 ⁽²⁾				
	Supply current	LSI ON	ON and IWDG	0.8	1.0	1.1	1.2	1.4	1.5	-	-	-				
	in Standby mode	Standby	LSI OF	OFF and IWDG F	0.7	0.8	0.9	1.0	1.1	1.3	2 ⁽²⁾	2.5	3 ⁽²⁾			
	Supply current in Stop mode	current	current	current	NO	Regulator in run mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾	
			monitoring (Regulator in low- power mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾	μA		
	Supply current in Standby mode	Supply current	V _{DDA} m	LSI ON and IWDG ON	2.3	2.5	2.7	2.9	3.1	3.3	-	-	-			
			LSI OFF and IWDG OFF	1.8	1.9	2	2.2	2.3	2.5	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾				
I _{DDA}	Supply current in Stop mode)FF	Regulator in run mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-		
		monitoring O	Regulator in low- power mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-				
	Supply	V _{DDA} mc	LSI ON and IWDG ON	1.5	1.6	1.7	1.8	1.9	2.0	-	i	-				
	in Standby mode	Λ	LSI OFF and IWDG OFF	1	1.0	1.1	1.1	1.2	1.2	-	-	-				

^{1.} Data based on characterization results, not tested in production unless otherwise specified.

^{2.} Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 27. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

			Typical ı	run mode	Typical S	unit	
Symbol	Parameter	f _{HCLK}	Peripheral s enabled	Peripheral s disabled	Peripheral s enabled	Peripheral s disabled	-
		48MHz	20.2	12.3	11.1	2.9	
		36 MHz	15.3	9.5	8.4	2.4	
		32 MHz	13.6	8.6	7.5	2.2	
		24 MHz	10.5	6.7	5.9	1.8	
,	Current from V _{DD}	16 MHz	7.2	4.7	4.1	1.4	mA
I _{DD}	supply	8 MHz	3.8	2.7	2.3	0.9	IIIA
		4 MHz	2.4	1.8	1.7	0.9	
		2 MHz	1.6	1.3	1.2	0.8	
		1 MHz	1.2	1.1	1.0	0.8	
		500 kHz	1.0	1.0	0.9	0.8	
		48MHz		15	55		
		36 MHz		1′	17		
		32 MHz		10	05		
		24 MHz		8	3		
١,	Current from V _{DDA}	16 MHz		6	0		uA
I _{DDA}	supply	8 MHz		2	.2		uA
		4 MHz		2	.2		
		2 MHz		2	.2		
		1 MHz		2	.2	_	
		500 kHz		2	.2		

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 46: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt



Table 28. Switching output I/O current consumption

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Тур	Unit
			4 MHz	0.07	
		V _{DDIOx} = 3.3 V	8 MHz	0.15	
		$C = C_{INT}$	16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
			4 MHz	0.18	
		V _{DDIOx} = 3.3 V	8 MHz	0.37	
		C _{EXT} = 0 pF	16 MHz	0.76	
		$C = C_{INT} + C_{EXT} + C_{S}$	24 MHz	1.39	
	I/O current consumption		48 MHz	2.188	
			4 MHz	0.32	mA
		$V_{DDIOx} = 3.3 \text{ V}$ $C_{EXT} = 10 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_{S}$	8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
I _{SW}			48 MHz	4.442	
'500		$V_{DDIOx} = 3.3 \text{ V}$ $C_{EXT} = 22 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_{S}$	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
			4 MHz	0.64	
		$V_{DDIOx} = 3.3 \text{ V}$	8 MHz	1.25	
		$C_{EXT} = 33 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	3.24	
		INT EXT 0	24 MHz	5.02	
		V _{DDIOx} = 3.3 V	4 MHz	0.81	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.7	
		$C = C_{INT} + C_{EXT} + C_{S}$ $C = C_{int}$	16 MHz	3.67	
		V _{DDIOx} = 2.4 V	4 MHz	0.66	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.43	
		$C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	2.45	
		C = C _{int}	24 MHz	4.97	

^{1.} C_S = 7 pF (estimated value).



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 29*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 15: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 29*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 29. Peripheral current consumption

	Peripheral	Typical consumption at 25 °C	Unit
	BusMatrix ⁽¹⁾	3.8	
	DMA1	6.3	
	SRAM	0.7	
	Flash memory interface	15.2	
AHB	CRC	1.61	∧ /٨/Ы⇒
АПБ	GPIOA	9.4	µA/MHz
	GPIOB	11.6	
	GPIOC	1.9	
	GPIOF	0.8	
	All AHB peripherals	47.5	

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{END}	Endurance	$T_A = -40 \text{ to } +105 ^{\circ}\text{C}$	10	kcycle
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 85 °C	30	
		1 kcycle ⁽²⁾ at T _A = 105 °C	10	Year
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

Table 40. Flash memory endurance and data retention

- 1. Data based on characterization results, not tested in production.
- 2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Level/ **Parameter Symbol Conditions Class** $V_{DD} = 3.3 \text{ V, LQFP48, T}_{A} = +25 \text{ °C,}$ Voltage limits to be applied on any I/O pin $f_{HCLK} = 48 \text{ MHz},$ 2B V_{FESD} to induce a functional disturbance conforming to IEC 61000-4-2 Fast transient voltage burst limits to be $V_{DD} = 3.3 \text{ V, LQFP48, } T_A = +25^{\circ}\text{C,}$ f_{HCLK} = 48 MHz, applied through 100 pF on V_{DD} and V_{SS} 4B V_{EFTB} pins to induce a functional disturbance conforming to IEC 61000-4-4

Table 41. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOX}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 15: Voltage characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 47. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾	-	0.4	.,
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	V _{DDIOx} -0.4	-	V
V _{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾	-	0.4	.,
V _{OH}	Output high level voltage for an I/O pin	I _{IO} = 8 mA V _{DDIOx} ≥ 2.7 V	2.4	-	V
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	V _{DDIOx} ≥ 2.7 V	V _{DDIOx} -1.3	-	\ \ \
V _{OL} ⁽³⁾	Output low level voltage for an I/O pin	I _{IO} = 6 mA	-	0.4	V
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	IIIOI – O IIIA	V _{DDIOx} -0.4	-	V
V _{OLFm+} ⁽³⁾	Output low level voltage for an FTf I/O pin in Fm+ mode	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \ge 2.7 \text{ V}$	-	0.4	V
02	Tim mode	I _{IO} = 10 mA	-	0.4	V

The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 15:
 Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

^{2.} TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

^{3.} Data based on characterization results. Not tested in production.

Table 58. I²C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit	
t _{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns	

- 1. Guaranteed by design, not tested in production.
- 2. Spikes with widths below t_{AF(min)} are filtered.
- 3. Spikes with widths above $t_{\text{AF}(\text{max})}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 59* for SPI or in *Table 60* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 18: General operating conditions*.

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 59. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit	
f _{SCK} 1/t _{c(SCK)}	CDI alask fraguanav	Master mode -		18	MHz	
	SPI clock frequency	Slave mode -		18	IVI□∠	
t _{r(SCK)}	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns	
t _{su(NSS)}	NSS setup time	Slave mode	4Tpclk	-		
t _{h(NSS)}	NSS hold time	Slave mode	2Tpclk + 10	-		
t _{w(SCKH)}	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1		
t _{su(MI)}	Data input setup time	Master mode	4	-		
t _{su(SI)}		Slave mode	5	-		
t _{h(MI)}	Data input hold time	Master mode	4	-		
t _{h(SI)}	Data input hold time	Slave mode	5	-		
t _{a(SO)} ⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20 MHz	0	3Tpclk		
t _{dis(SO)} (3)	Data output disable time	Slave mode	0	18		
t _{v(SO)}	Data output valid time	Slave mode (after enable edge)	-	22.5		
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	6		
t _{h(SO)}	Data output hold time	Slave mode (after enable edge)	11.5	-		
t _{h(MO)}	Data output noid time	Master mode (after enable edge)	2	-		
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%	

- 1. Data based on characterization results, not tested in production.
- 2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
- 3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z



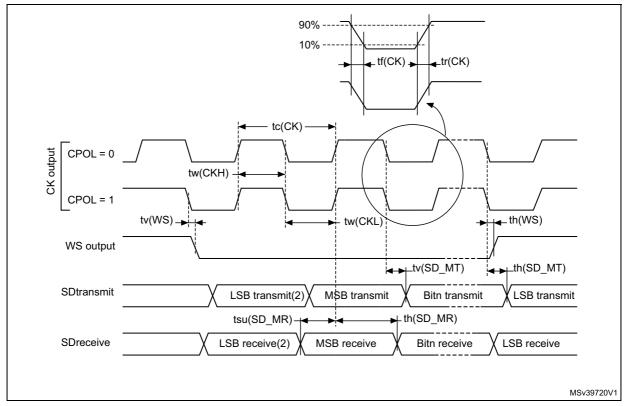


Figure 30. I²S master timing diagram (Philips protocol)

- 1. Data based on characterization results, not tested in production.
- LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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Table 63. UFQFPN32 package mechanical data

Symbol	millimeters		inches ⁽¹⁾			
	Min	Тур	Max	Min	Тур	Max
Α	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
Е	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
е	-	0.500	-	-	0.0197	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

5.30 3.80 3.80 3.80 3.80 3.80 3.80 AOB8_FP_V2

Figure 38. Recommended footprint for UFQFPN32 package

1. Dimensions are expressed in millimeters.

1. Values in inches are converted from mm and rounded to 4 decimal digits.

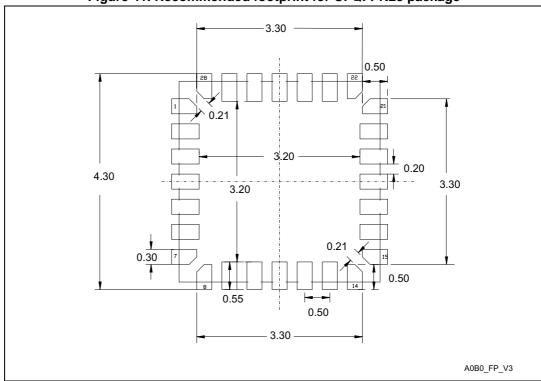


Figure 41. Recommended footprint for UFQFPN28 package

1. Dimensions are expressed in millimeters.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

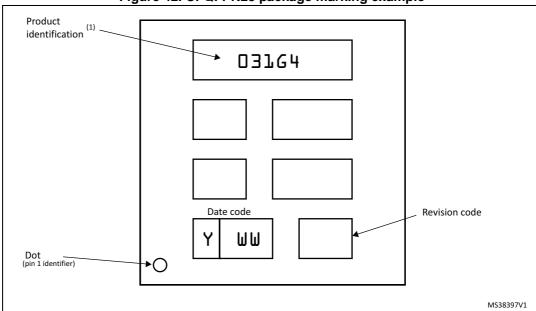


Figure 42. UFQFPN28 package marking example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F031x4/x6 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 80 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

```
P_{INTmax} = 50 \text{ mA} \times 3.5 \text{ V} = 175 \text{ mW}
```

 $P_{IOmax = 20} \times 8 \text{ mA} \times 0.4 \text{ V} + 8 \times 20 \text{ mA} \times 1.3 \text{ V} = 272 \text{ mW}$

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

$$P_{Dmax} = 175 + 272 = 447 \text{ mW}$$

Using the values obtained in *Table 68* T_{Jmax} is calculated as follows:

```
    For LQFP48, 55 °C/W
```

$$T_{\text{lmax}} = 80 \,^{\circ}\text{C} + (55 \,^{\circ}\text{C/W} \times 447 \,^{\circ}\text{mW}) = 80 \,^{\circ}\text{C} + 24.585 \,^{\circ}\text{C} = 104.585 \,^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105$ °C) see *Table 18: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Section 8: Ordering information).

Note:

With this given $P_{Dmax we}$ can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

```
Suffix 6: T_{Amax} = T_{Jmax} - (55^{\circ}\text{C/W} \times 447 \text{ mW}) = 105\text{-}24.585 = 80.415 ^{\circ}\text{C}
Suffix 7: T_{Amax} = T_{Jmax} - (55^{\circ}\text{C/W} \times 447 \text{ mW}) = 125\text{-}24.585 = 100.415 ^{\circ}\text{C}
```

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

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