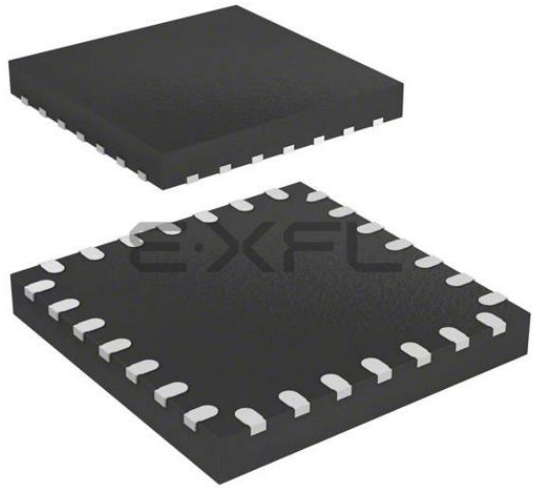

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031g6u7

2 Description

The STM32F031x4/x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 4 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I^2C, one SPI/ I^2S and one USART), one 12-bit ADC,
five 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F031x4/x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F031x4/x6 microcontrollers include devices in six different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F031x4/x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Table 2. STM32F031x4/x6 family device features and peripheral counts

Peripheral		STM32F031Fx		STM32F031Ex	STM32F031Gx		STM32F031Kx		STM32F031Cx	
Flash memory (Kbyte)		16	32	32	16	32	16	32	16	32
SRAM (Kbyte)		4								
Timers	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32-bit)								
Comm. interfaces	SPI [I^2S](1)	1 [1]								
	I^2C	1								
	USART	1								
12-bit ADC (number of channels)		1 (9 ext. + 3 int.)		1 (10 ext. + 3 int.)						
GPIOs		15		20	23		25 (on LQFP32) 27 (on UFQFPN32)		39	
Max. CPU frequency		48 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperature		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C								
Packages		TSSOP20		WLCSP25	UFQFPN28		LQFP32 UFQFPN32		LQFP48	

1. The SPI interface can be used either in SPI mode or in I^2S audio mode.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F031x4/x6 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1 or USART1.

  USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

TIM2, TIM3

STM32F031x4/x6 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM16 and TIM17

Both timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

They each have a single channel for input capture/output compare, PWM or one-pulse mode output.

TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.11.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

4 Pinouts and pin description

Figure 3. LQFP48 package pinout

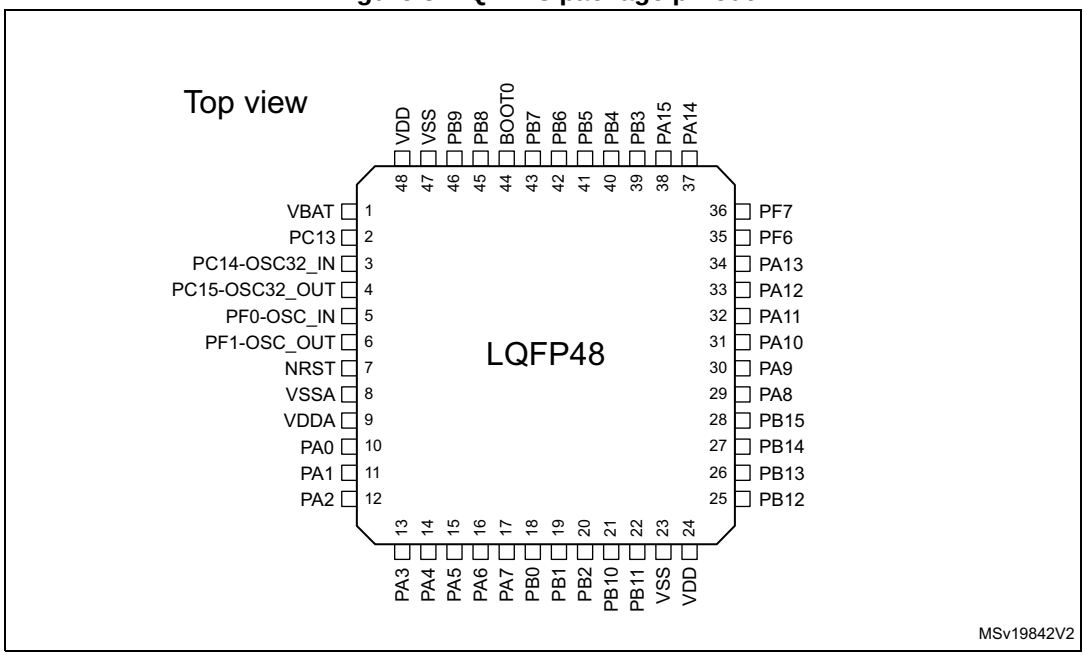


Figure 4. LQFP32 package pinout

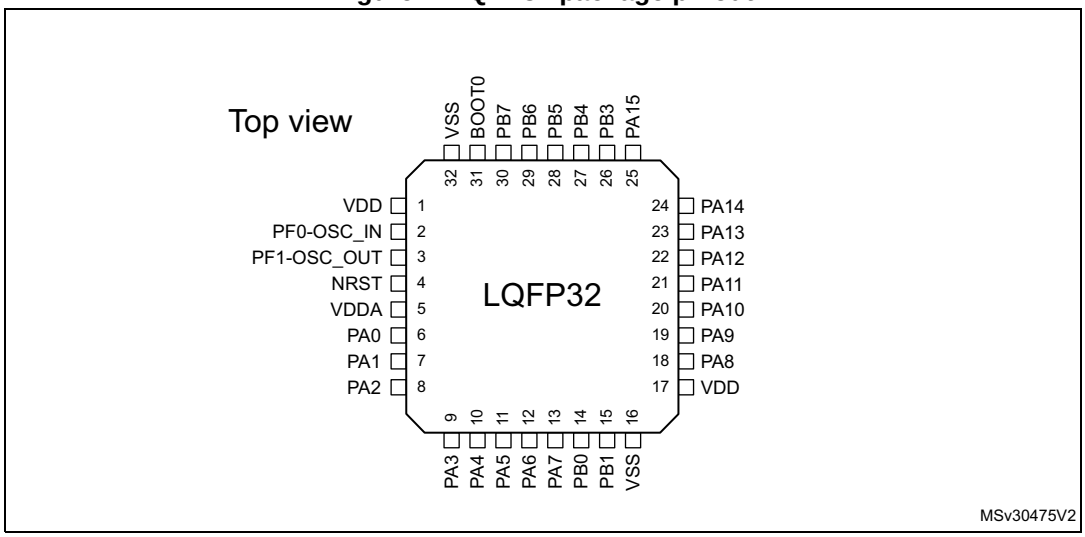


Figure 5. UFQFPN32 package pinout

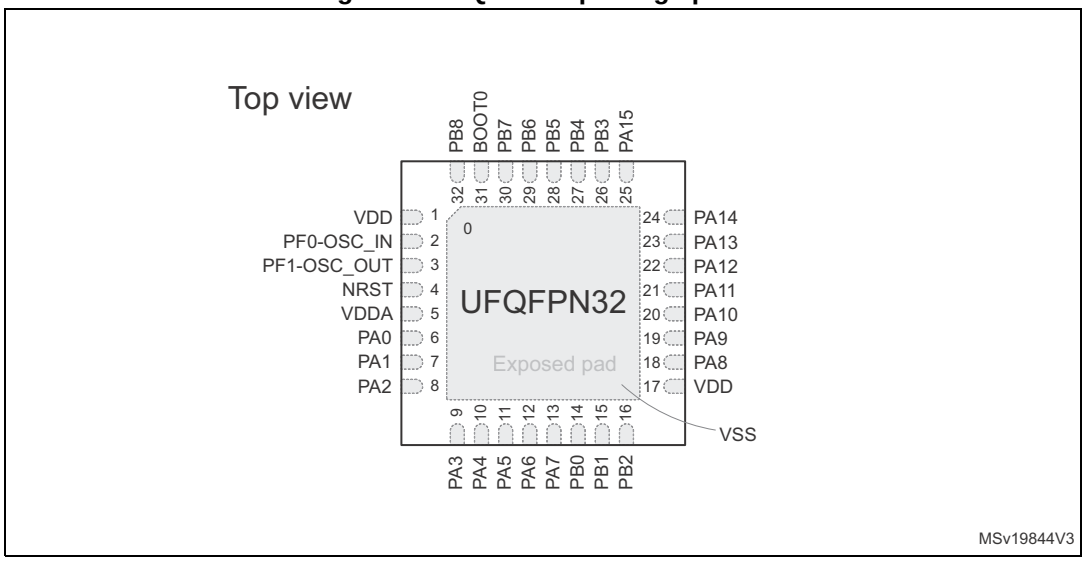


Figure 6. UFQFPN28 package pinout

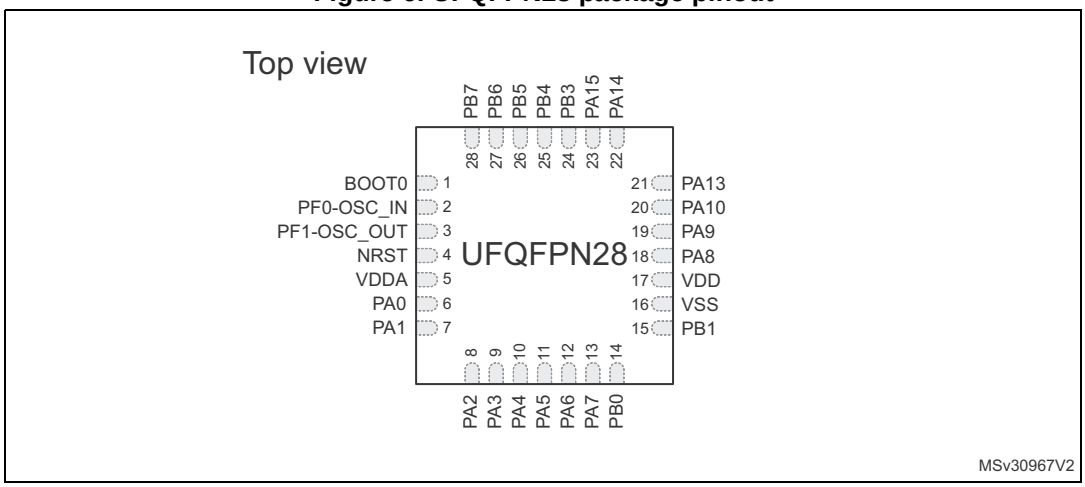


Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input-only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		FTf	5 V-tolerant I/O, FM+ capable
		TTa	3.3 V-tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. Pin definitions

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	-	-	-	-	-	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	-	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	-	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT
5	2	2	2	A5	2	PF0-OSC_IN (PF0)	I/O	FT	-	-	OSC_IN

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART1_CTS	TIM2_CH1_ ETR	-	-	-	-	-
PA1	EVENTOUT	USART1_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	USART1_TX	TIM2_CH3	-	-	-	-	-
PA3	-	USART1_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART1_CK	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	-	TIM2_CH1_ ETR	-	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	-	USART1_TX	TIM1_CH2	-	I2C1_SCL	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	-	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	-
PA14	SWCLK	USART1_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART1_RX	TIM2_CH1_ ETR	EVENTOUT	-	-	-	-

Table 14. STM32F031x4/x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 29: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Low-speed internal (LSI) RC oscillator

Table 37. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 38. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = - 40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (1 KB) erase time	T_A = - 40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = - 40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT and FTf pins	–5	NA	
	Injected current on all TTa, TC and RESET pins	–5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the conditions summarized in *Table 18: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}+0.07(1)	V
		FT and FTf I/O	-	-	0.475 V_{DDIOx}–0.2(1)	
		BOOT0	-	-	0.3 V_{DDIOx}–0.3(1)	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DDIOx}	
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DDIOx}+0.398(1)	-	-	V
		FT and FTf I/O	0.5 V_{DDIOx}+0.2(1)	-	-	
		BOOT0	0.2 V_{DDIOx}+0.95(1)	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DDIOx}	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 15: Voltage characteristics*).

Output voltage levels

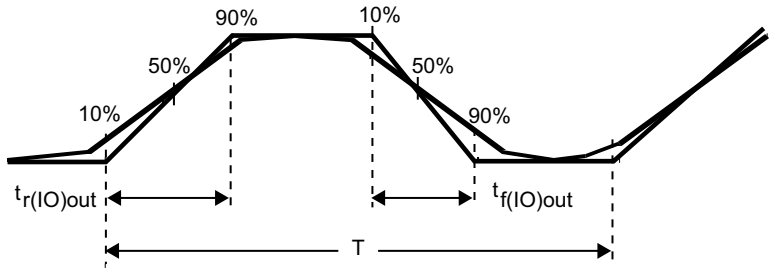
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 47. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 15: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq \frac{2}{3}T$ and if the duty cycle is (45-55%)
when loaded by C_L (see the table *I/O AC characteristics definition*)

MS32132V3

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

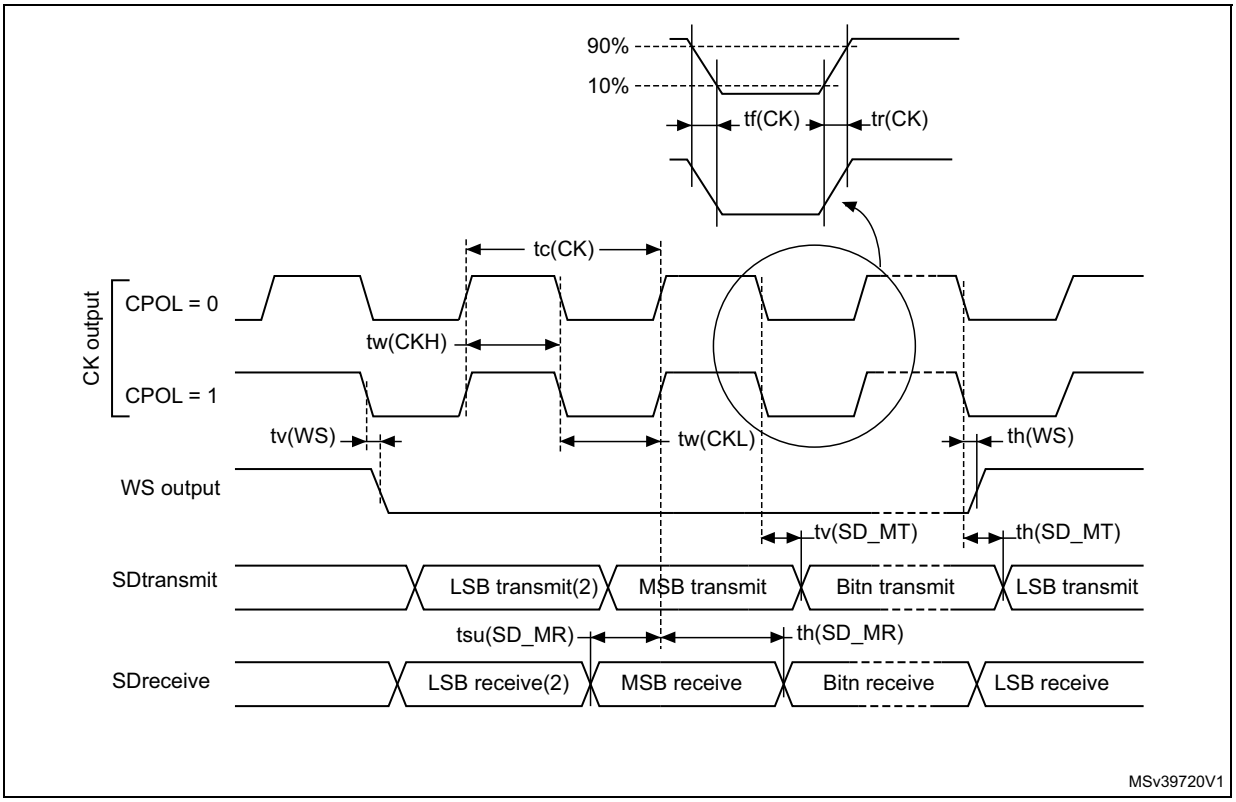
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	$100^{(1)}$	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	$300^{(3)}$	-	-	ns
		$2.0 < V_{DD} < 3.6$	$500^{(3)}$	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 30. I²S master timing diagram (Philips protocol)

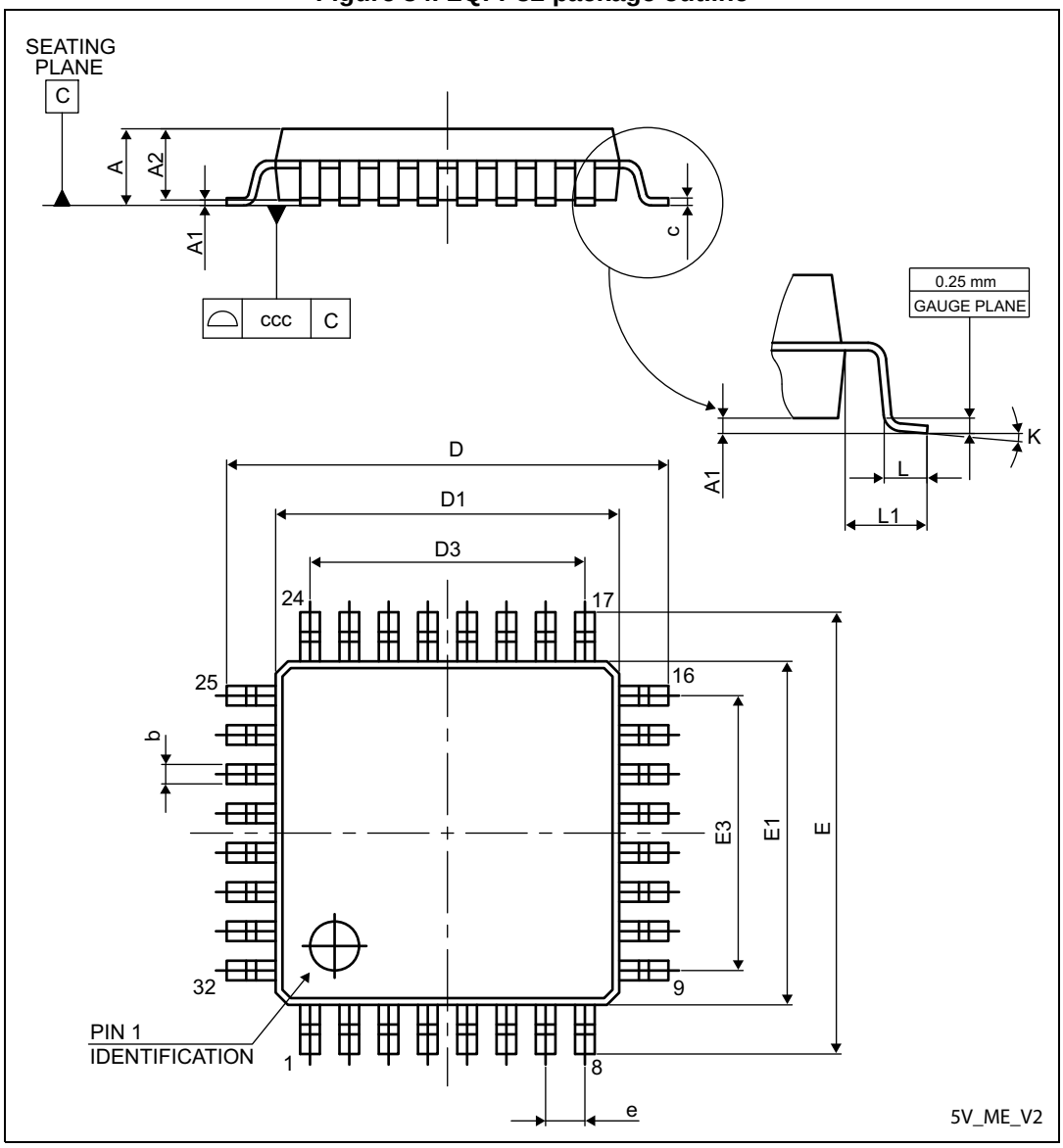


1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 34. LQFP32 package outline

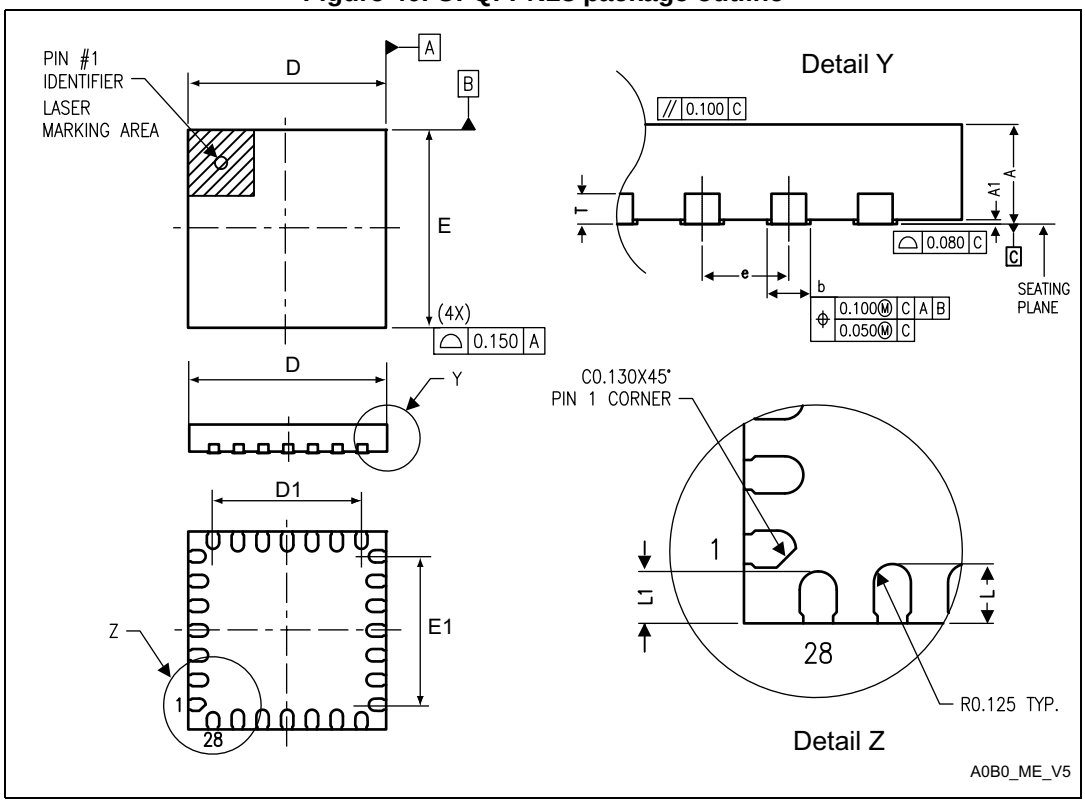


1. Drawing is not to scale.

7.4 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 40. UFQFPN28 package outline



1. Drawing is not to scale.

Table 64. UFQFPN28 package mechanical data(1)

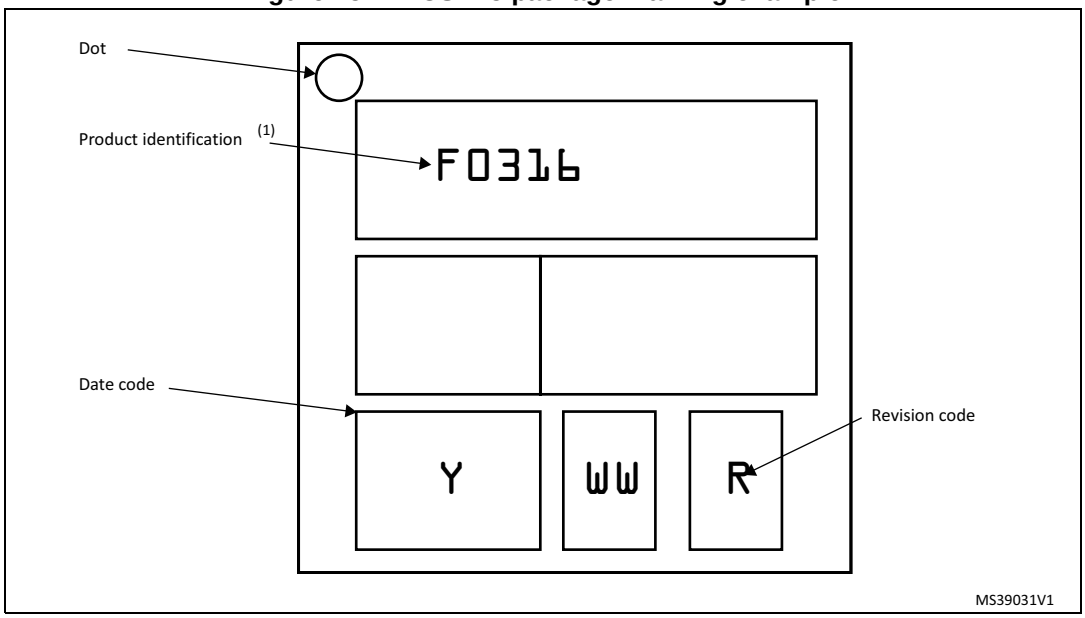
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 45. WLCSP25 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 68* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

T_{Jmax} = 100 °C + (55 °C/W × 134 mW) = 100 °C + 7.37 °C = 107.37 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Table 70. Document revision history (continued)

Date	Revision	Changes
28-Aug-2015	3 (continued)	Added WLCSP25 package, updates in the following: – *Table 1: Device summary*, – *Section 2: Description*, – *Table 2: STM32F031x4/x6 family device features and peripheral counts*, – *Section 4: Pinouts and pin description*: addition of *Figure 7: WLCSP25 25-ball package ballout (bump side)* and update of *Table 11: Pin definitions*, – *Table 18: General operating conditions*, – *Section 7: Package information* with the addition of *Section 7.5: WLCSP25 package information*, – *Table 68: Package thermal characteristics*.
16-Dec-2015	4	**Cover page:** – number of timers added in the title – *Table 1: Device summary* - STM32F031x4 added ***Section 2: Description*:** – *Figure 1: Block diagram* updated ***Section 3: Functional overview*:** – *Figure 2: Clock tree* updated – *Section 3.5.4: Low-power modes* - added explicit inf. on peripherals configurable to operate with HSI – *Section 3.10.2: Internal voltage reference (V_{REFINT})* - removed information on comparators – *Section 3.11.2: General-purpose timers (TIM2, 3, 14, 16, 17)* - number of gen-purpose timers corrected – *Section Table 7.: STM32F031x4/x6 I^2C implementation* - added 20mA output drive current ***Section 4: Pinouts and pin description*:** – Package pinout figures updated (look and feel) – *Figure 7: WLCSP25 package pinout* - **now presented in top view** – *Table 11: Pin definitions* - notes 3 and 6 added ***Section 5: Memory mapping*:** – added information on memory mapping difference of STM32F031x4 from STM32F031x6 ***Section 6: Electrical characteristics*:** – *Table 22: Embedded internal reference voltage*: removed -40°-to-85° condition and associated note for V_{REFINT} – *Table 25* and *Table 26* values rounded to 1 decimal – *Table 46: I/O static characteristics* - removed note – *Table 50: ADC characteristics* - updated some parameter values, test conditions and added footnotes (3) and (4)

Table 70. Document revision history (continued)

Date	Revision	Changes
16-Dec-2015	4 (continued)	– *Section 6.3.16: 12-bit ADC characteristics* - changed introductory sentence – *Table 60: I^2S characteristics*: table reorganized, $t_{v(SD\_ST)}$ max value updated ***Section 7: Package information*:** – *Figure 41: Recommended footprint for UFQFPN28 package* updated ***Section 8: Part numbering*:** – added tray packing to options
06-Jan-2017	5	***Section 6: Electrical characteristics*:** – *Table 34: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 22: Embedded internal reference voltage* - V_{REFINT} values – *Figure 26: SPI timing diagram - slave mode and CPHA = 0* and *Figure 27: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information*:** – The name of the section changed from the previous “Part numbering”