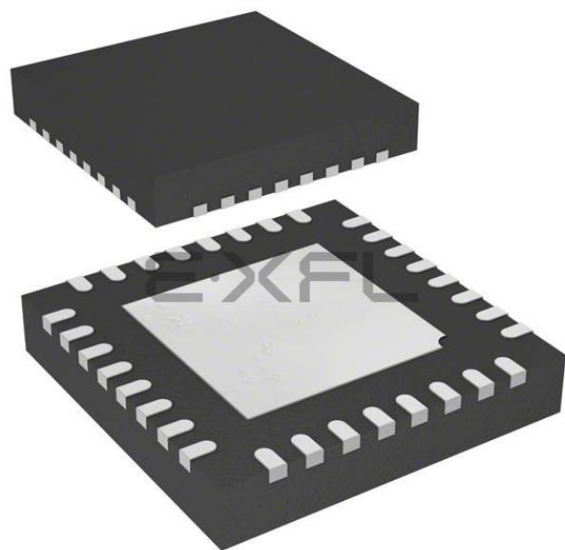




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f031k6u6tr

List of tables

Table 1.	Device summary	1
Table 2.	STM32F031x4/x6 family device features and peripheral counts	9
Table 3.	Temperature sensor calibration values	16
Table 4.	Internal voltage reference calibration values	16
Table 5.	Timer feature comparison	17
Table 6.	Comparison of I ² C analog and digital filters	20
Table 7.	STM32F031x4/x6 I ² C implementation	20
Table 8.	STM32F031x4/x6 USART implementation	21
Table 9.	STM32F031x4/x6 SPI/I2S implementation	21
Table 10.	Legend/abbreviations used in the pinout table	26
Table 11.	Pin definitions	26
Table 12.	Alternate functions selected through GPIOA_AFR registers for port A	31
Table 13.	Alternate functions selected through GPIOB_AFR registers for port B	32
Table 14.	STM32F031x4/x6 peripheral register boundary addresses	34
Table 15.	Voltage characteristics	39
Table 16.	Current characteristics	40
Table 17.	Thermal characteristics	40
Table 18.	General operating conditions	41
Table 19.	Operating conditions at power-up / power-down	42
Table 20.	Embedded reset and power control block characteristics	42
Table 21.	Programmable voltage detector characteristics	42
Table 22.	Embedded internal reference voltage	43
Table 23.	Typical and maximum current consumption from V _{DD} at 3.6 V	44
Table 24.	Typical and maximum current consumption from the V _{DDA} supply	45
Table 25.	Typical and maximum current consumption in Stop and Standby modes	46
Table 26.	Typical and maximum current consumption from the V _{BAT} supply	47
Table 27.	Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal	48
Table 28.	Switching output I/O current consumption	50
Table 29.	Peripheral current consumption	51
Table 30.	Low-power mode wakeup timings	53
Table 31.	High-speed external user clock characteristics	53
Table 32.	Low-speed external user clock characteristics	54
Table 33.	HSE oscillator characteristics	55
Table 34.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	56
Table 35.	HSI oscillator characteristics	58
Table 36.	HSI14 oscillator characteristics	59
Table 37.	LSI oscillator characteristics	60
Table 38.	PLL characteristics	60
Table 39.	Flash memory characteristics	60
Table 40.	Flash memory endurance and data retention	61
Table 41.	EMS characteristics	61
Table 42.	EMI characteristics	62
Table 43.	ESD absolute maximum ratings	63
Table 44.	Electrical sensitivities	63
Table 45.	I/O current injection susceptibility	64
Table 46.	I/O static characteristics	64
Table 47.	Output voltage characteristics	67

List of figures

Figure 1.	Block diagram	10
Figure 2.	Clock tree	14
Figure 3.	LQFP48 package pinout	23
Figure 4.	LQFP32 package pinout	23
Figure 5.	UFQFPN32 package pinout	24
Figure 6.	UFQFPN28 package pinout	24
Figure 7.	WLCSP25 package pinout	25
Figure 8.	TSSOP20 package pinout	25
Figure 9.	STM32F031x6 memory map	33
Figure 10.	Pin loading conditions	36
Figure 11.	Pin input voltage	36
Figure 12.	Power supply scheme	37
Figure 13.	Current consumption measurement scheme	38
Figure 14.	High-speed external clock source AC timing diagram	54
Figure 15.	Low-speed external clock source AC timing diagram	54
Figure 16.	Typical application with an 8 MHz crystal	56
Figure 17.	Typical application with a 32.768 kHz crystal	57
Figure 18.	HSI oscillator accuracy characterization results for soldered parts	58
Figure 19.	HSI14 oscillator accuracy characterization results	59
Figure 20.	TC and TTa I/O input characteristics	66
Figure 21.	Five volt tolerant (FT and FTf) I/O input characteristics	66
Figure 22.	I/O AC characteristics definition	69
Figure 23.	Recommended NRST pin protection	70
Figure 24.	ADC accuracy characteristics	73
Figure 25.	Typical connection diagram using the ADC	73
Figure 26.	SPI timing diagram - slave mode and CPHA = 0	77
Figure 27.	SPI timing diagram - slave mode and CPHA = 1	77
Figure 28.	SPI timing diagram - master mode	78
Figure 29.	I ² S slave timing diagram (Philips protocol)	79
Figure 30.	I ² S master timing diagram (Philips protocol)	80
Figure 31.	LQFP48 package outline	81
Figure 32.	Recommended footprint for LQFP48 package	82
Figure 33.	LQFP48 package marking example	83
Figure 34.	LQFP32 package outline	84
Figure 35.	Recommended footprint for LQFP32 package	85
Figure 36.	LQFP32 package marking example	86
Figure 37.	UFQFPN32 package outline	87
Figure 38.	Recommended footprint for UFQFPN32 package	88
Figure 39.	UFQFPN32 package marking example	89
Figure 40.	UFQFPN28 package outline	90
Figure 41.	Recommended footprint for UFQFPN28 package	91
Figure 42.	UFQFPN28 package marking example	92
Figure 43.	WLCSP25 package outline	93
Figure 44.	Recommended footprint for WLCSP25 package	94
Figure 45.	WLCSP25 package marking example	95
Figure 46.	TSSOP20 package outline	96
Figure 47.	Recommended footprint for TSSOP20 package	97
Figure 48.	TSSOP20 package marking example	98

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F031x4/x6 microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.



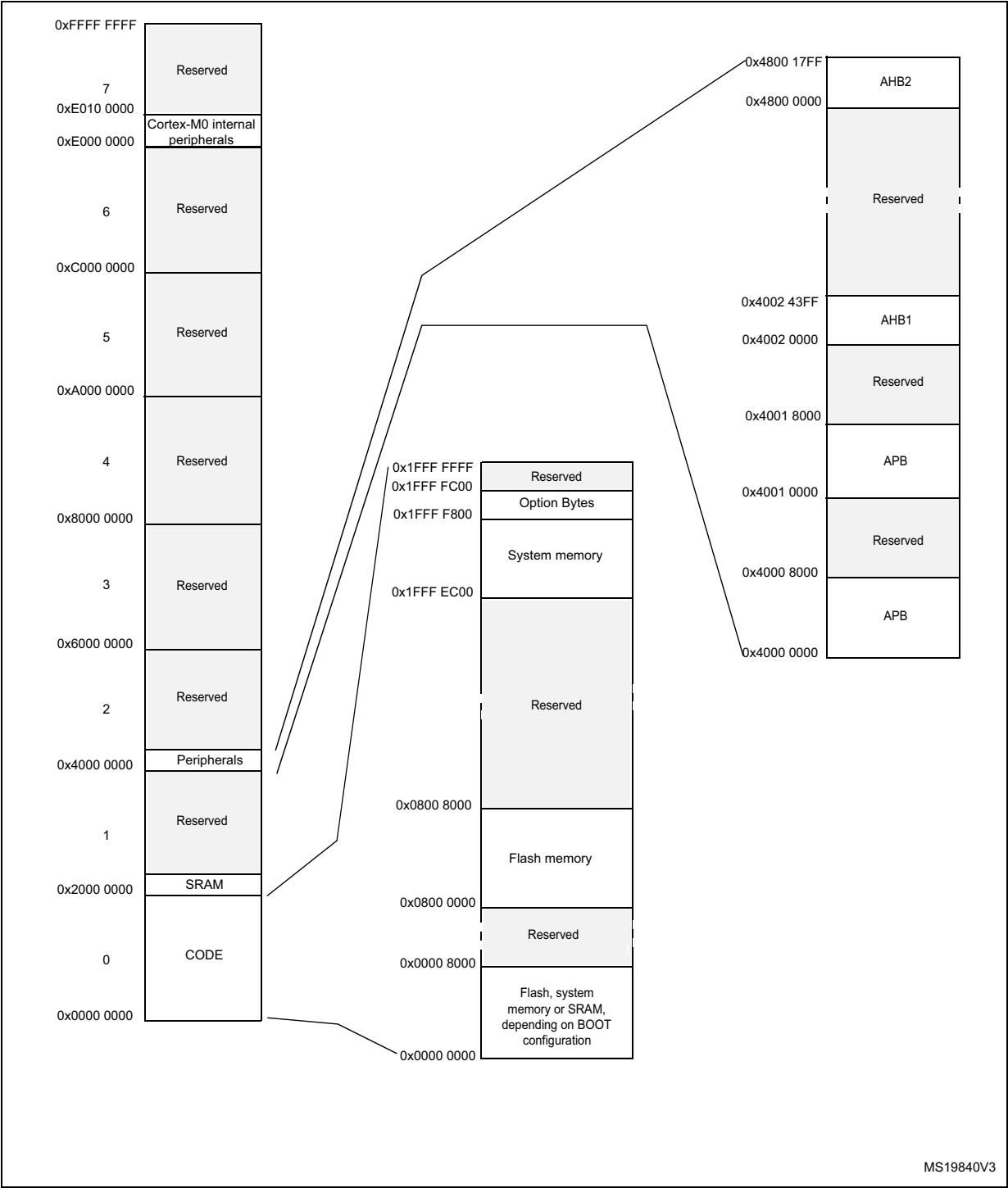
Table 11. Pin definitions (continued)

Pin number						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	LQFP32	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
6	3	3	3	B5	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	4	4	4	C5	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	16 (3)	0 ⁽³⁾	16 (3)	E1 (3)	15 (3)	VSSA	S		-	Analog ground	
9	5	5	5	D5	5	VDDA	S		-	Analog power supply	
10	6	6	6	B4	6	PA0	I/O	TTa	-	TIM2_CH1_ETR, USART1_CTS	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	7	C4	7	PA1	I/O	TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS	ADC_IN1
12	8	8	8	D4	8	PA2	I/O	TTa	-	TIM2_CH3, USART1_TX	ADC_IN2
13	9	9	9	E5	9	PA3	I/O	TTa	-	TIM2_CH4, USART1_RX	ADC_IN3
14	10	10	10	B3	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK	ADC_IN4
15	11	11	11	C3	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR	ADC_IN5
16	12	12	12	D3	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6

5 Memory mapping

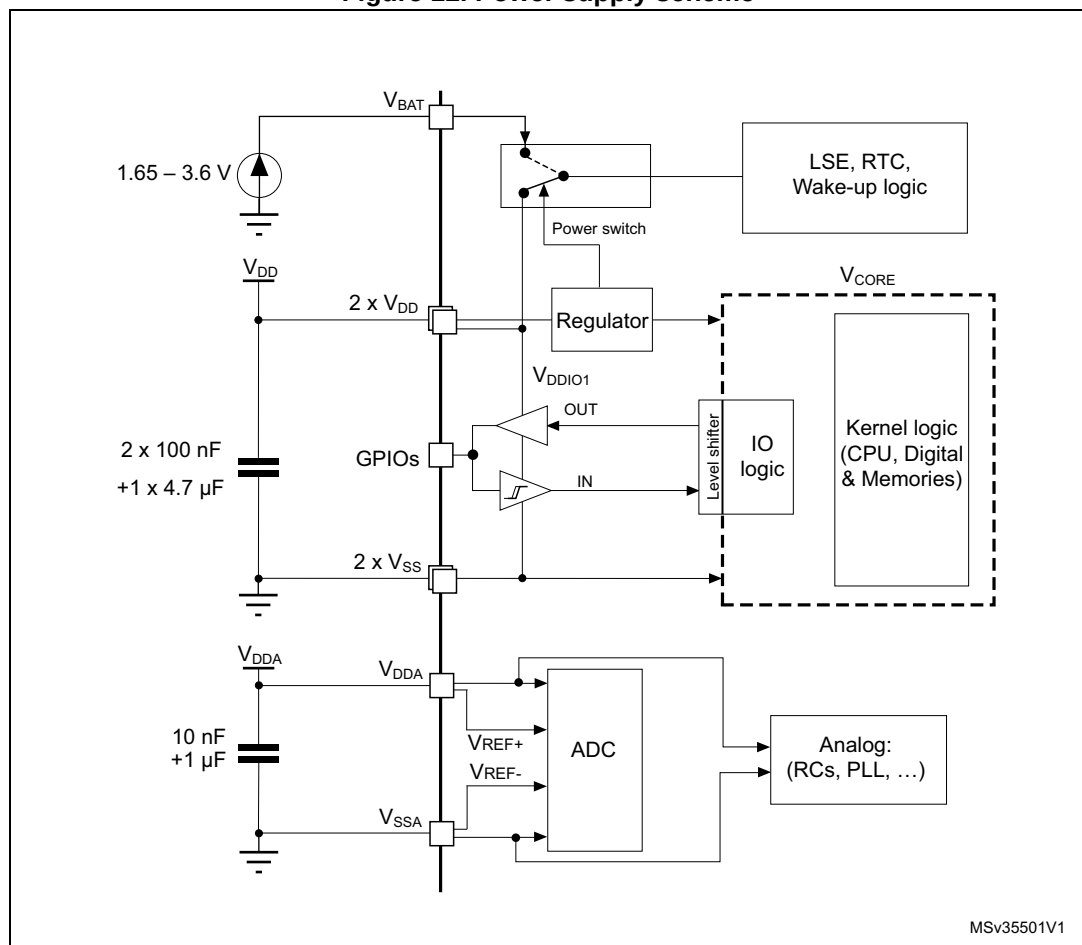
To the difference of STM32F031x6 memory map in [Figure 9](#), the two bottom code memory spaces of STM32F031x4 end at 0x0000 3FFF and 0x0800 3FFF, respectively.

Figure 9. STM32F031x6 memory map



6.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.3 Operating conditions

6.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.0	3.6	V
V_{DDA}	Analog operating voltage (ADC not used)	Must have a potential equal to or higher than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	$V_{DDIOx}+0.3$	V
		TTa I/O	-0.3	$V_{DDA}+0.3^{(1)}$	
		FT and FTf I/O	-0.3	5.5 ⁽¹⁾	
		BOOT0	0	5.5	
P_D	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 ⁽²⁾	LQFP48	-	364	mW
		UFQFPN32	-	526	
		LQFP32	-	357	
		UFQFPN28	-	169	
		WLCSP25	-	267	
		TSSOP20	-	182	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low power dissipation ⁽³⁾	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	°C
		Low power dissipation ⁽³⁾	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C
		Suffix 7 version	-40	125	

1. For operation with a voltage higher than $V_{DDIOx} + 0.3\text{ V}$, the internal pull-up resistor must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See [Section 7.7: Thermal characteristics](#).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.7: Thermal characteristics](#)).

6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 19](#) are derived from tests performed under the ambient temperature condition summarized in [Table 18](#).

Table 25. Typical and maximum current consumption in Stop and Standby modes

Sym- bol	Para- meter	Conditions	Typ @V _{DD} (V _{DD} = V _{DDA})						Max ⁽¹⁾			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	15	15.1	15.3	15.5	15.7	16	18 ⁽²⁾	38	55 ⁽²⁾	μA
		Regulator in low-power mode, all oscillators OFF	3.2	3.3	3.4	3.5	3.7	4	5.5 ⁽²⁾	22	41 ⁽²⁾	
	Supply current in Standby mode	LSI ON and IWDG ON	0.8	1.0	1.1	1.2	1.4	1.5	-	-	-	
		LSI OFF and IWDG OFF	0.7	0.8	0.9	1.0	1.1	1.3	2 ⁽²⁾	2.5	3 ⁽²⁾	
I _{DDA}	Supply current in Stop mode	V _{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
			Regulator in low-power mode, all oscillators OFF	1.9	2	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
	Supply current in Standby mode	V _{DDA} monitoring ON	LSI ON and IWDG ON	2.3	2.5	2.7	2.9	3.1	3.3	-	-	-
			LSI OFF and IWDG OFF	1.8	1.9	2	2.2	2.3	2.5	3.5 ⁽²⁾	3.5	4.5 ⁽²⁾
	Supply current in Stop mode	V _{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-
			Regulator in low-power mode, all oscillators OFF	1.1	1.2	1.2	1.2	1.3	1.4	-	-	-
	Supply current in Standby mode	V _{DDA} monitoring OFF	LSI ON and IWDG ON	1.5	1.6	1.7	1.8	1.9	2.0	-	-	-
			LSI OFF and IWDG OFF	1	1.0	1.1	1.1	1.2	1.2	-	-	-

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

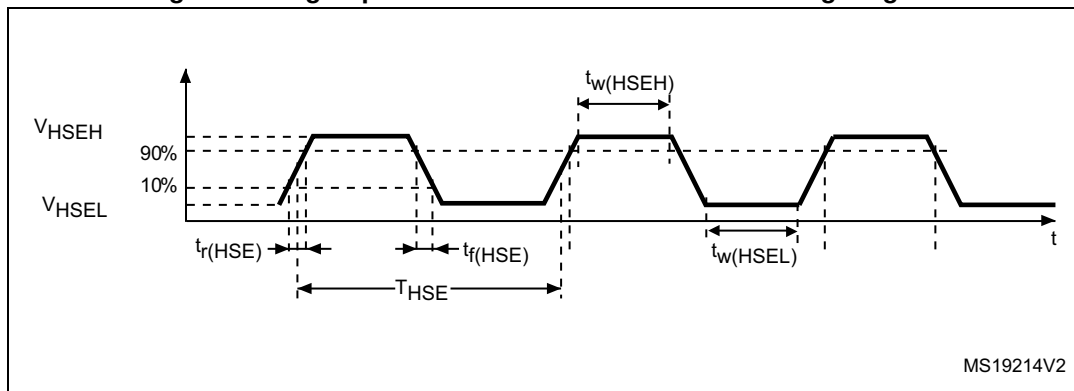
Table 29. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge ⁽²⁾	2.6	μA/MHz
	SYSCFG	1.7	
	ADC ⁽³⁾	4.2	
	TIM1	17.1	
	SPI1	9.6	
	USART1	17.4	
	TIM16	8.2	
	TIM17	8.0	
	DBG (MCU Debug Support)	0.5	
	TIM2	17.4	
	TIM3	12.8	
	TIM14	6.0	
	WWDG	1.5	
	I2C1	5.1	
	PWR	1.2	
	All APB peripherals	110.9	

1. The BusMatrix automatically is active when at least one master is ON (CPU or DMA1).
2. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC is not included. Refer to the tables of characteristics in the subsequent sections.

1. Guaranteed by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

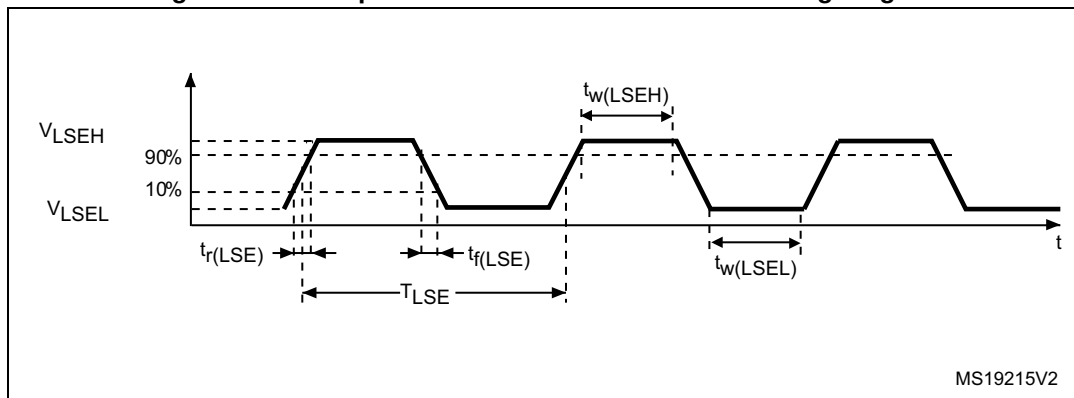
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 15](#).

Table 32. Low-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7 V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 15. Low-speed external clock source AC timing diagram



High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 36. HSI14 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1 ⁽²⁾	%
DuCy _(HSI14)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC _{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$	-4.2 ⁽³⁾	-	5.1 ⁽³⁾	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}$	-3.2 ⁽³⁾	-	3.1 ⁽³⁾	%
		$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	-2.5 ⁽³⁾	-	2.3 ⁽³⁾	%
		$T_A = 25 \text{ }^\circ\text{C}$	-1	-	1	%
$t_{\text{su(HSI14)}}$	HSI14 oscillator startup time	-	1 ⁽²⁾	-	2 ⁽²⁾	μs
$I_{\text{DDA(HSI14)}}$	HSI14 oscillator power consumption	-	-	100	150 ⁽²⁾	μA

1. $V_{\text{DDA}} = 3.3 \text{ V}$, $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$ unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 19. HSI14 oscillator accuracy characterization results

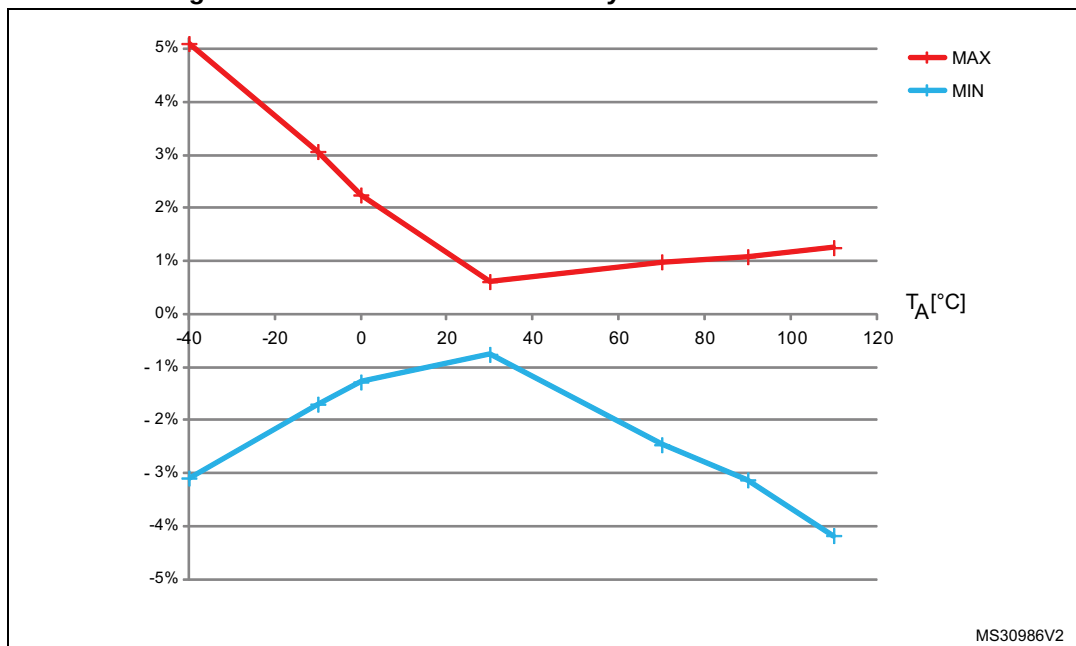


Table 40. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
N _{END}	Endurance	T _A = -40 to +105 °C	10	kcycle
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 85 °C	30	Year
		1 kcycle ⁽²⁾ at T _A = 105 °C	10	
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 41](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

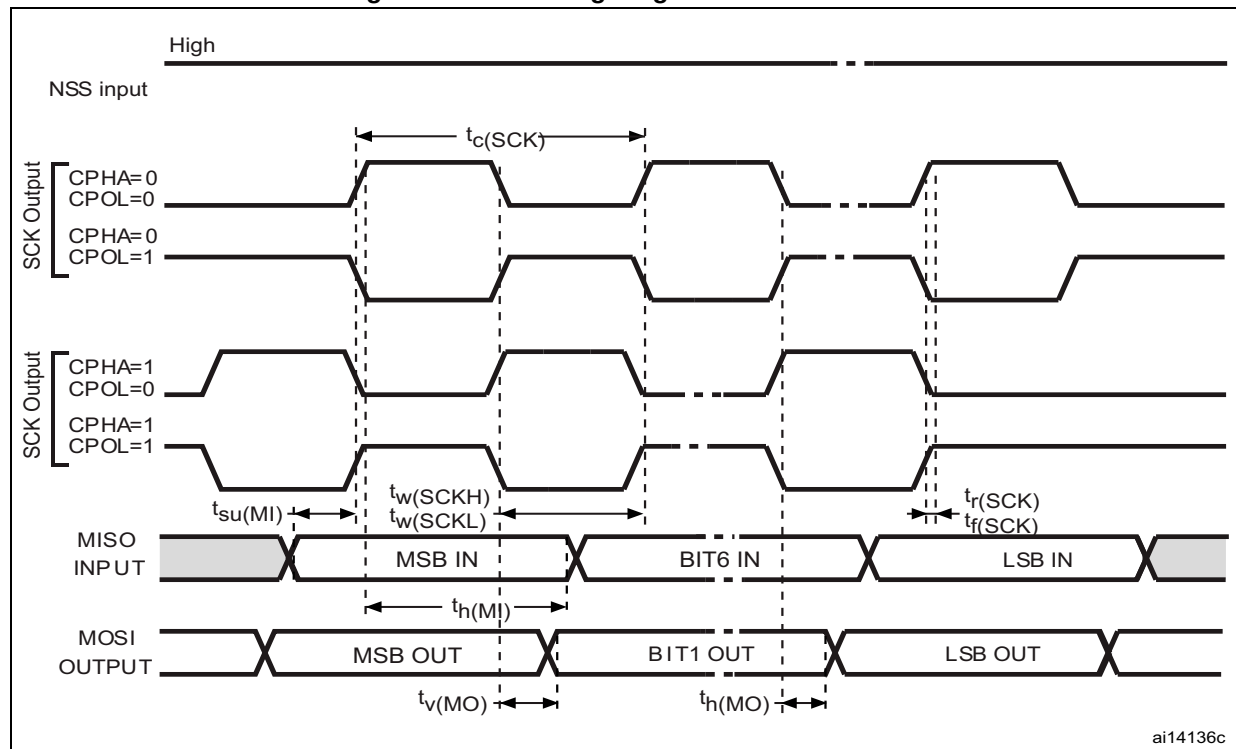
Symbol	Parameter	Conditions	Level/Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V _{DD} = 3.3 V, LQFP48, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance	V _{DD} = 3.3 V, LQFP48, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Figure 28. SPI timing diagram - master mode

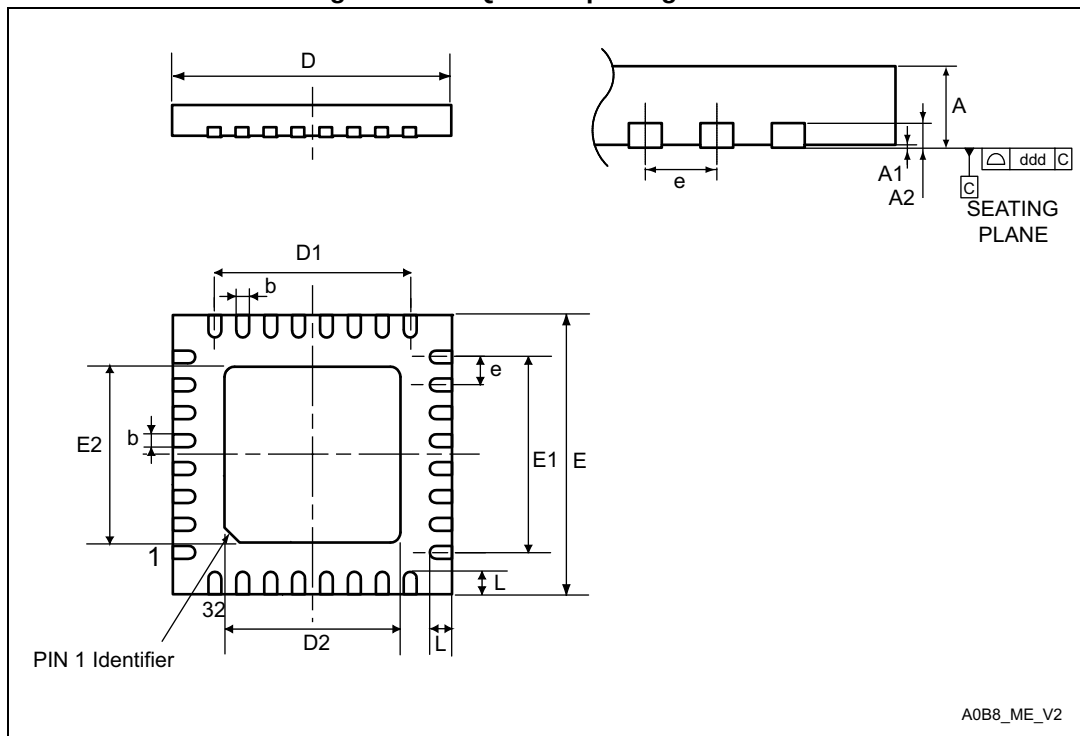


1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Table 60. I²S characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I ² S clock rise time	Capacitive load $C_L = 15$ pF	-	10	ns
$t_{f(CK)}$	I ² S clock fall time		-	12	
$t_{w(CKH)}$	I ² S clock high time	Master $f_{PCLK} = 16$ MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I ² S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I ² S slave input clock duty cycle	Slave mode	25	75	%

Figure 37. UFQFPN32 package outline



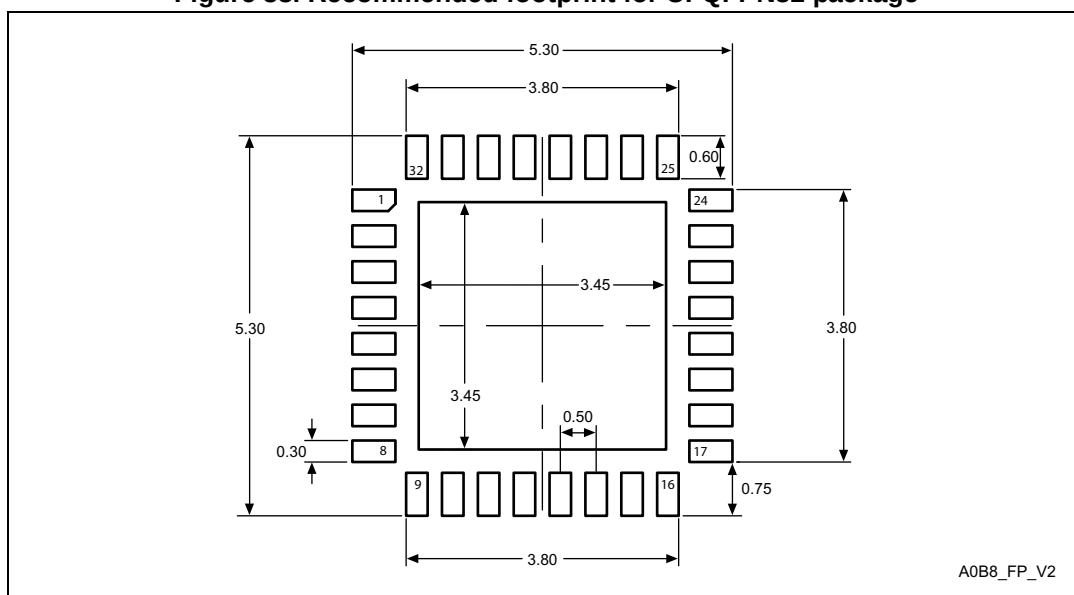
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table: Pin definitions*.

Table 63. UFQFPN32 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for UFQFPN32 package



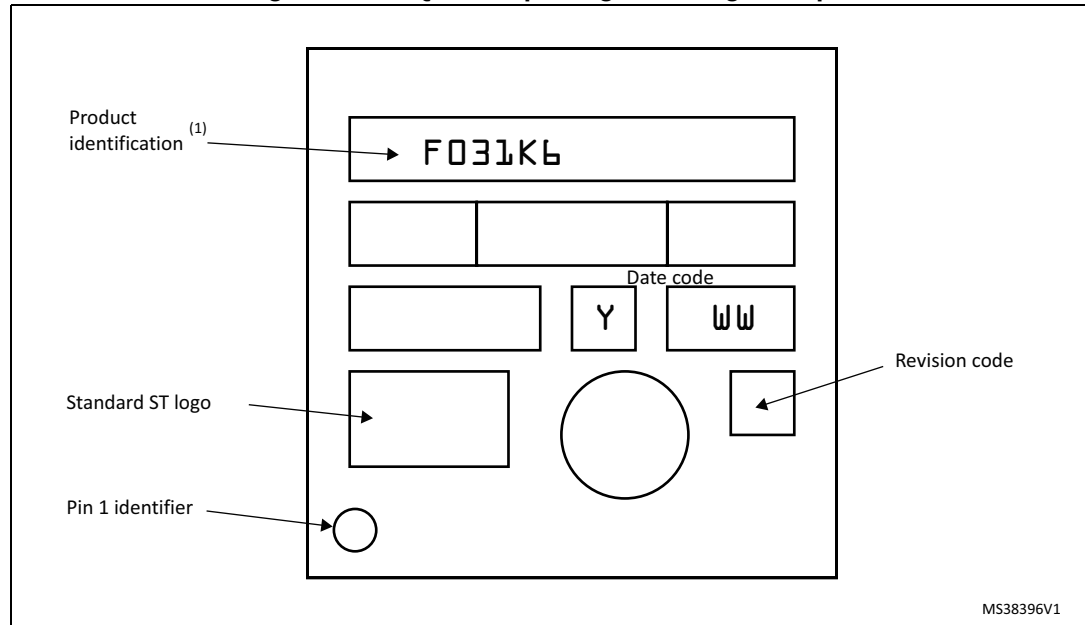
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. UFQFPN32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 65. WLCSP25 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

Figure 44. Recommended footprint for WLCSP25 package

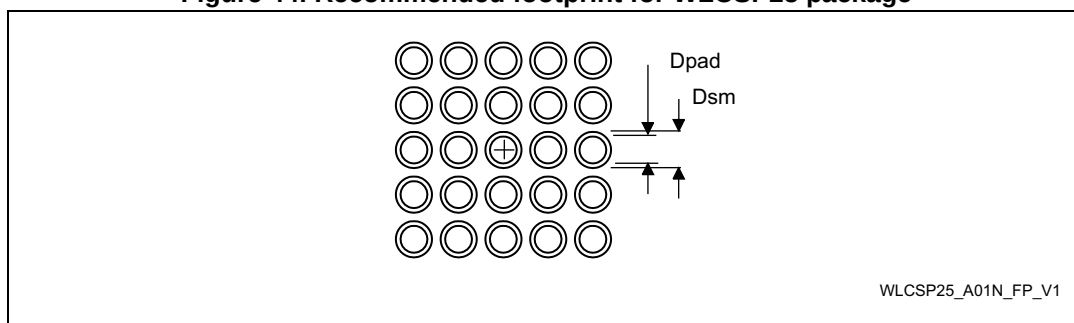


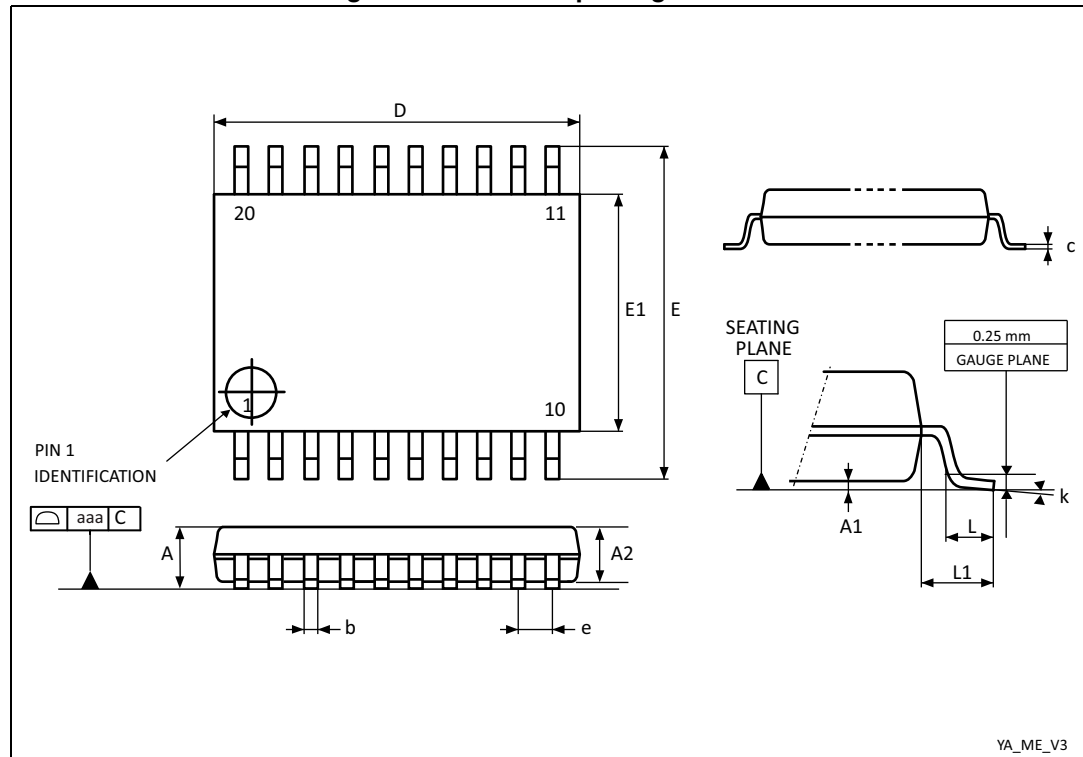
Table 66. WLCSP25 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

7.6 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small-outline, 6.5 x 4.4 mm, 0.65 mm pitch, package.

Figure 46. TSSOP20 package outline



1. Drawing is not to scale.

Table 67. TSSOP20 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D ⁽²⁾	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 ⁽³⁾	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F031x4/x6 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 80\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 68](#) T_{Jmax} is calculated as follows:

– For LQFP48, $55\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 80\text{ }^{\circ}\text{C} + (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 80\text{ }^{\circ}\text{C} + 24.585\text{ }^{\circ}\text{C} = 104.585\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$) see [Table 18: General operating conditions](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Ordering information](#)).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 105 - 24.585 = 80.415\text{ }^{\circ}\text{C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 125 - 24.585 = 100.415\text{ }^{\circ}\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved