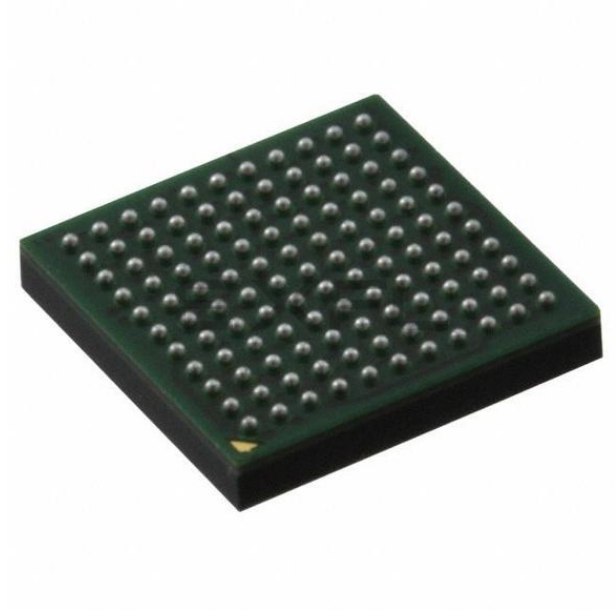


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b; D/A 2x6b, 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-XFBGA
Supplier Device Package	121-XFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk82fn256vdc15

Ordering Information

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM	
MK82FN256VDC15	256 KB	256 KB	87
MK82FN256VLL15	256 KB	256 KB	66
MK82FN256CAx15R [1]	256 KB	256 KB	87
MK82FN256VLQ15[2]	256 KB	256 KB	102

1. The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.
2. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Related Resources

Type	Description	Resource
Product Selector	The Product Selector lets you find the right Kinetis part for your design.	K-Series Product Selector
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	K8x Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K82P121M150SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_1N03P[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 100-pin: 98ASS23308W[1] • XFBGA 121-pin: 98ASA00595D[1] • LQFP 144-pin: 98ASS23177W[2] • WLCSP 121-pin: Under development[2]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. This package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 7. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					2
	• @ 25°C	—	28	31.55	mA	
	• @ 105°C	—	39.6	50.10		
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					3, 4
	• @ 25°C	—	54	57.55	mA	
	• @ 105°C	—	70	80.50		
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V					5
	• @ 25°C	—	25.1	28.65	mA	
	• @ 105°C	—	37.8	48.30		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					6
	• @ 25°C	—	38	40.70	mA	
	• @ 105°C	—	51.7	65.04		
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					7, 8
	• @ 25°C	—	48	50.70	mA	
	• @ 105°C	—	63.7	77.04		
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0V					
	• @ 25°C	—	34.5	37.2	mA	
	• @ 105°C	—	50.3	63.64		
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled					9
	• @ 25°C	—	14.2	19.87	mA	
	• @ 105°C	—	26.2	35.66		
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks enabled					9
		—	24.4	30.07	mA	

Table continues on the next page...

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15pf (1.8V) and 35pf (3V) on output pins. Input slew: 1ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 22. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

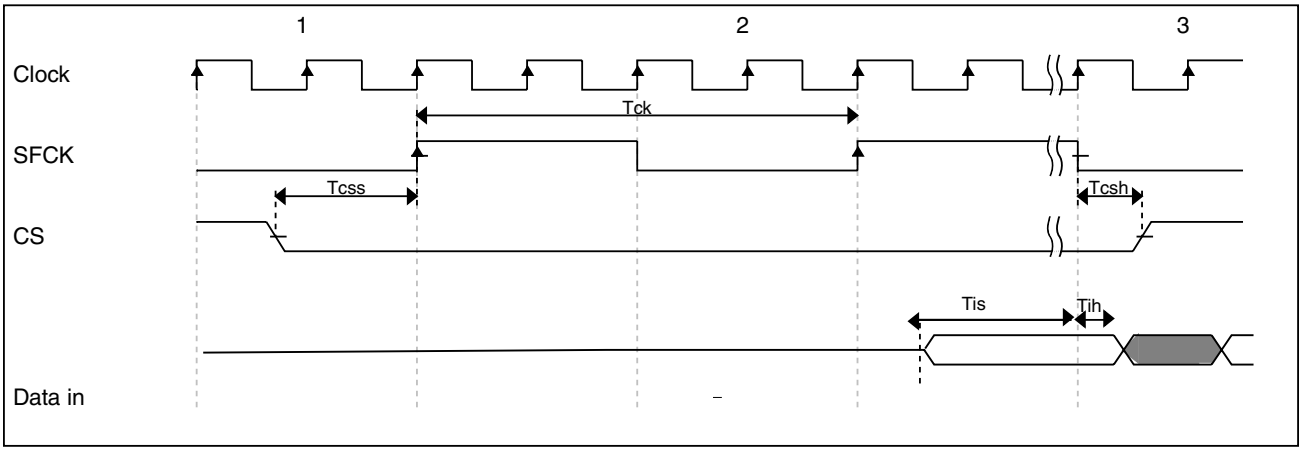


Figure 14. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

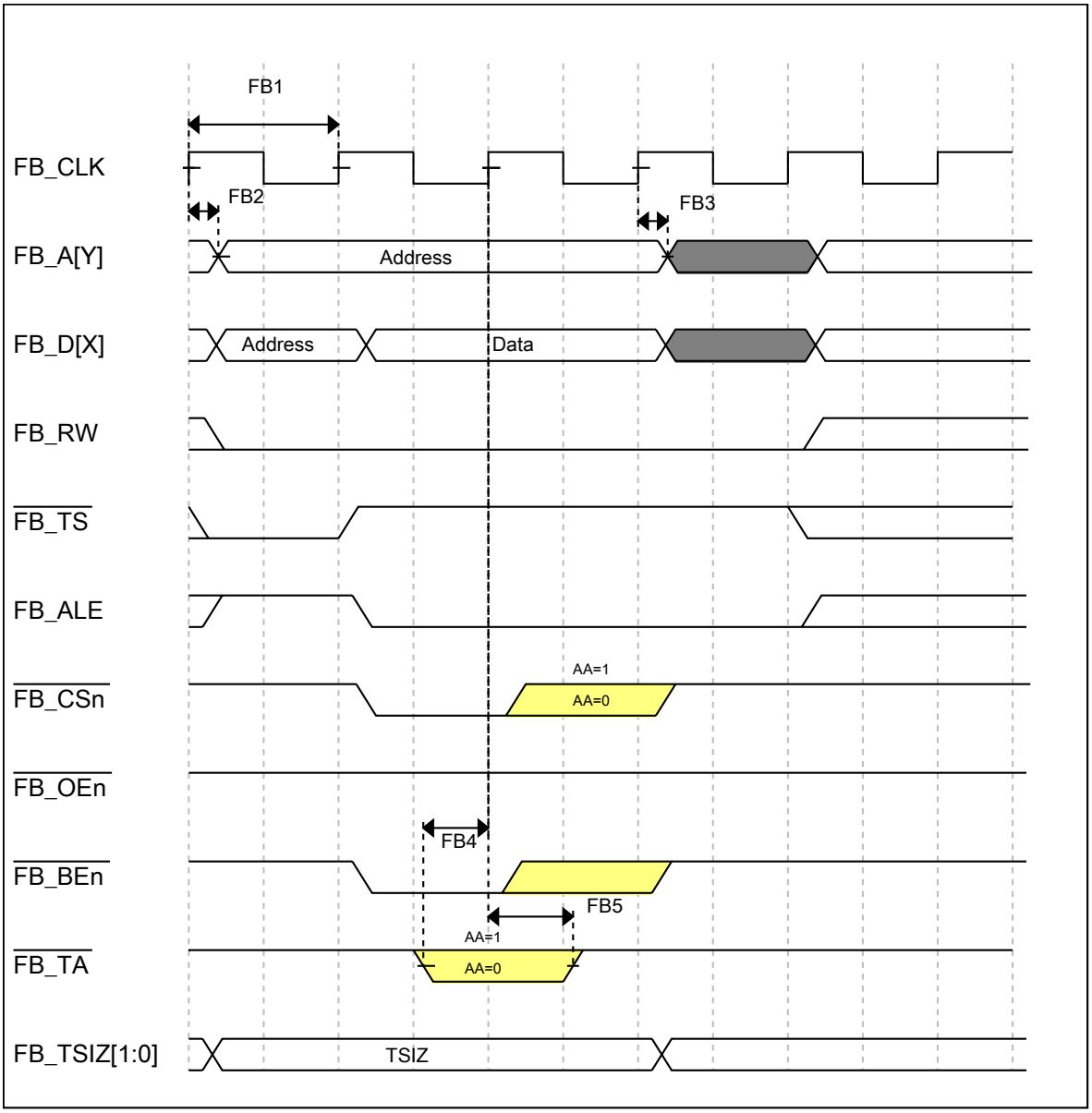


Figure 21. FlexBus write timing diagram

3.3.4 SDRAM controller specifications

Following figure shows SDRAM read cycle.

3. D7 and D8 are for write cycles only.

Table 36. SDRAM Timing (Limited voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.1	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	7.3	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	11.1	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz
3. D7 and D8 are for write cycles only.

Following figure shows an SDRAM write cycle.

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

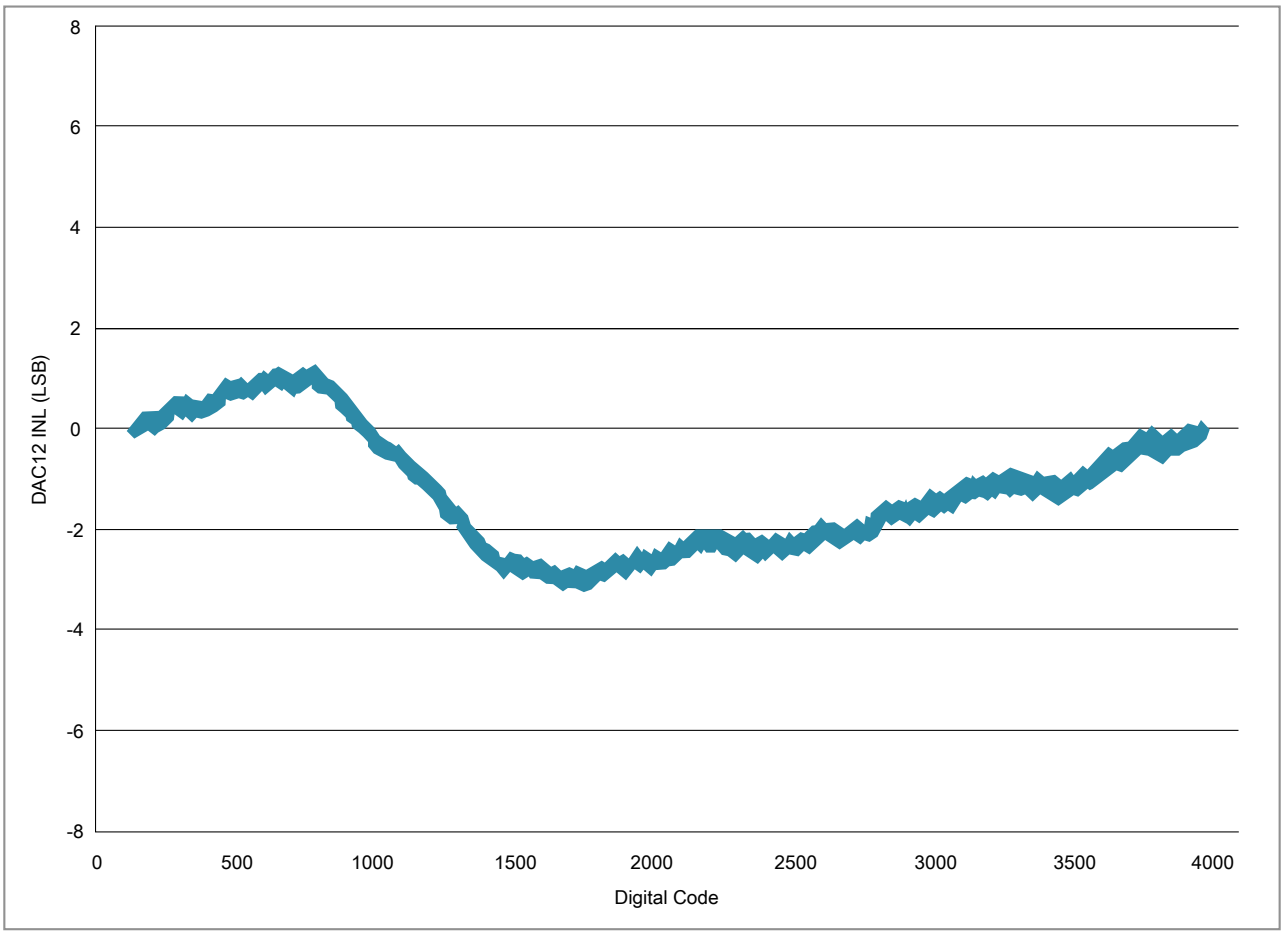


Figure 28. Typical INL error vs. digital code

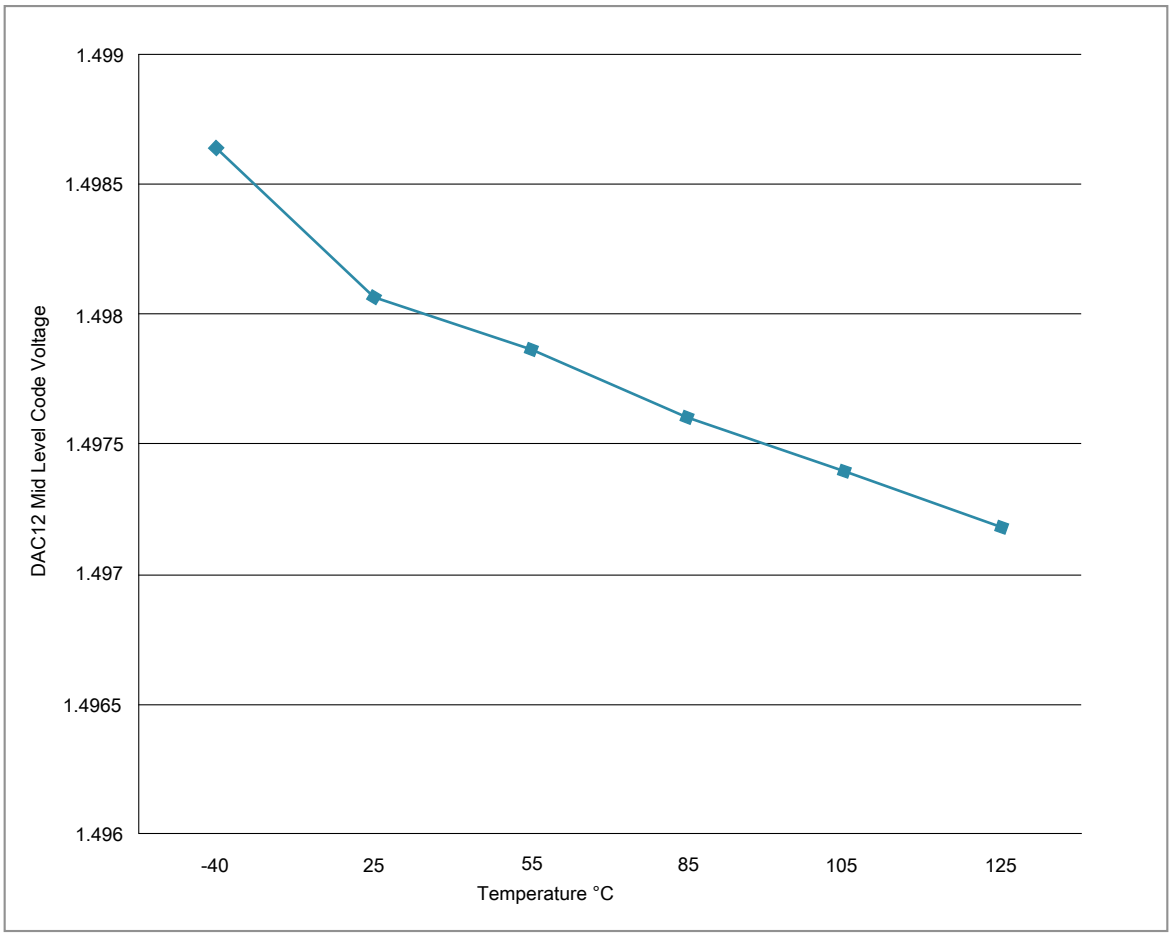


Figure 29. Offset at half scale vs. temperature

3.5.4 Voltage reference electrical specifications

Table 42. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 43. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 44. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 45. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

3.6 Timers

See General switching specifications.

3.7 Communication interfaces

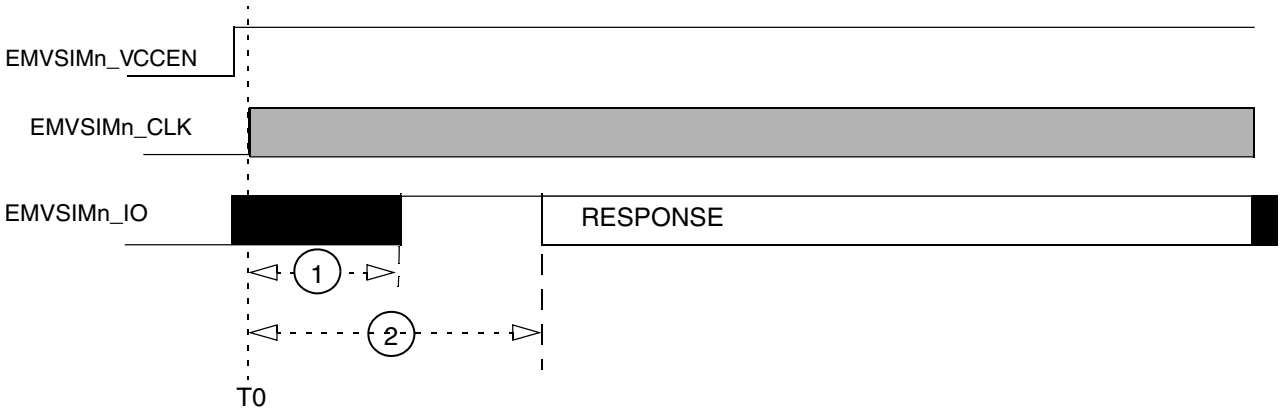


Figure 31. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 47. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

3.7.1.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps::

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

Table 53. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15 [1]	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.0	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13	ns

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

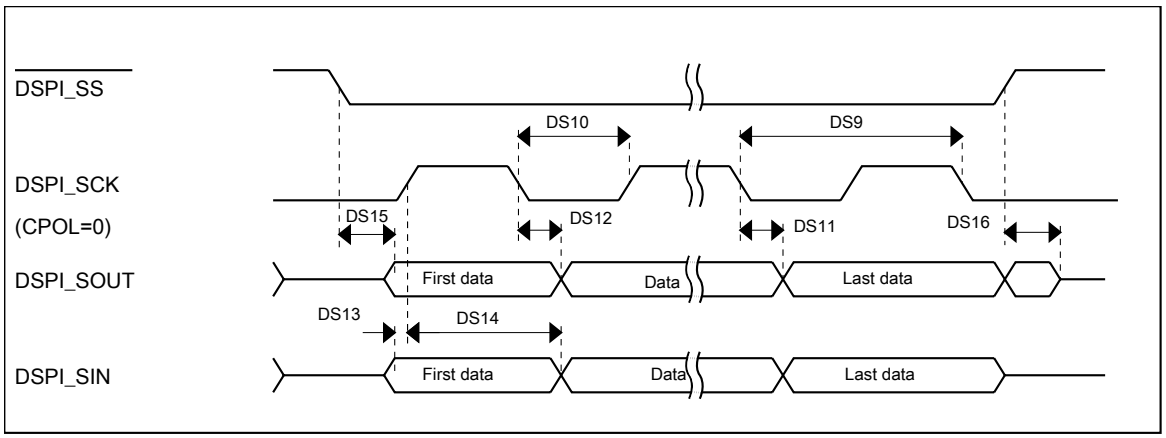


Figure 35. DSPI classic SPI timing — slave mode

Table 55. Slave mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13.0	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13.0	ns

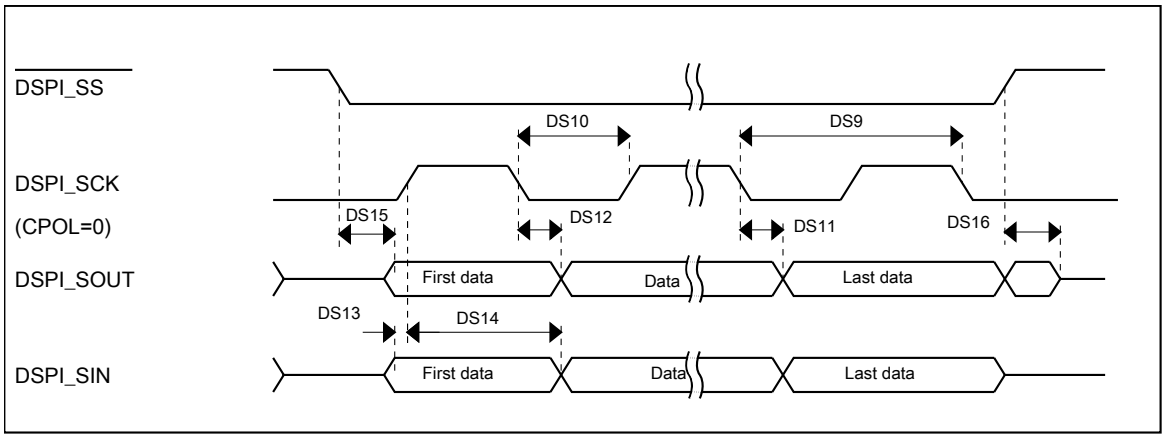


Figure 37. DSPI classic SPI timing — slave mode

3.7.6 I²C switching specifications

See General switching specifications.

3.7.7 UART switching specifications

See General switching specifications.

3.7.8 LPUART switching specifications

See General switching specifications.

3.7.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 56. SDHC full voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25/45	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	25/45	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	8.1	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

Table 57. SDHC limited voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	7	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				

Table continues on the next page...

Table 58. I2S master mode timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

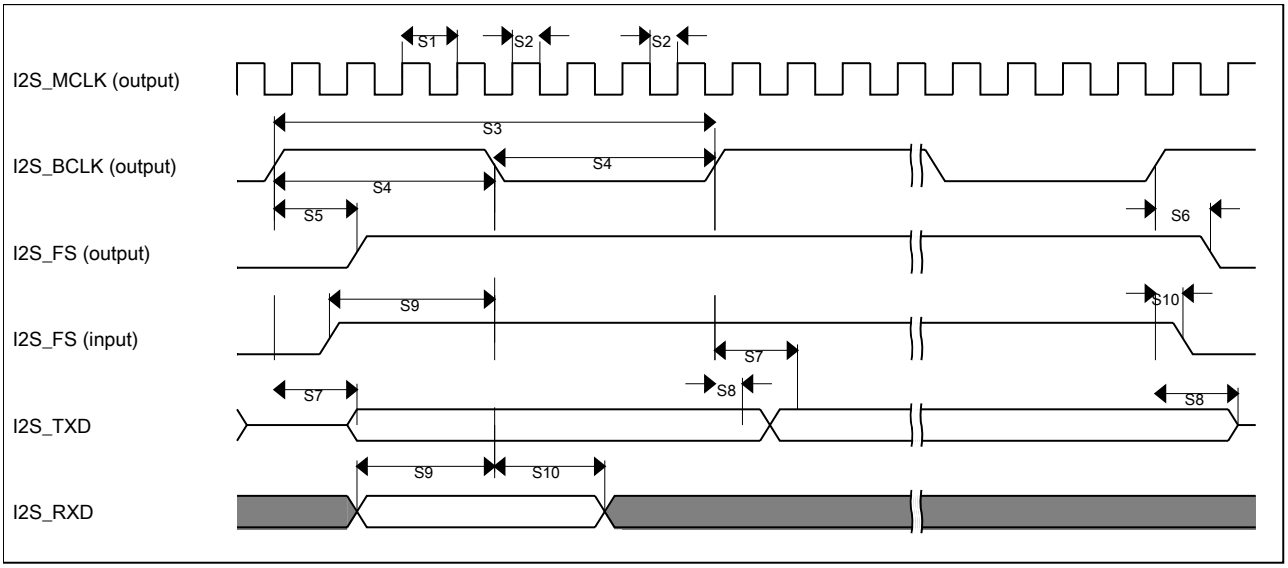


Figure 39. I²S timing — master mode

Table 59. I2S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	4.5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]		25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

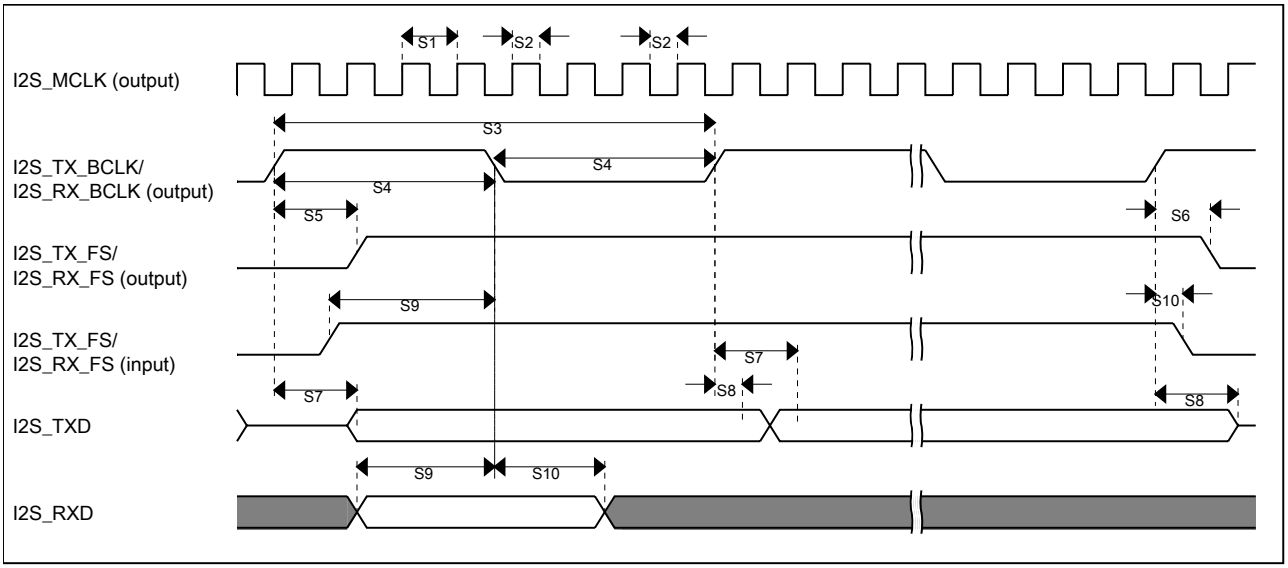


Figure 43. I2S/SAI timing — master modes

Table 63. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	5	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	56.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
32	—	K3	K11	ADC0_DM3	ADC0_DM3	ADC0_DM3								
33	22	F5	H8	VDDA	VDDA	VDDA								
34	23	G5	H9	VREFH	VREFH	VREFH								
35	24	G6	J9	VREFL	VREFL	VREFL								
36	25	F6	J8	VSSA	VSSA	VSSA								
37	26	L2	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
38	27	L1	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
39	28	L3	L11	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC0_SE22								
40	29	K4	L10	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
42	30	K5	H7	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
43	31	L4	L9	XTAL32	XTAL32	XTAL32								
44	32	L5	L8	EXTAL32	EXTAL32	EXTAL32								
45	33	K6	K8	VBAT	VBAT	VBAT								
46	34	—	G7	VDD	VDD	VDD								
47	35	—	F6	VSS	VSS	VSS								
48	—	H5	L7	PTA20	DISABLED		PTA20	I2C0_SCL	LPUART4_TX	FTM_CLKIN1	FXIO0_D8	EWM_OUT_b	TPM_CLKIN1	
49	—	J5	K7	PTA21/ LLWU_P21	DISABLED		PTA21/ LLWU_P21	I2C0_SDA	LPUART4_RX		FXIO0_D9	EWM_IN		
50	36	L7	J7	PTA0	JTAG_TCLK/ SWD_CLK	TSI0_CH1	PTA0	LPUART0_CTS_b	FTM0_CH5		FXIO0_D10	EMVSIM0_CLK	JTAG_TCLK/ SWD_CLK	
51	37	H8	J6	PTA1	JTAG_TDI	TSI0_CH2	PTA1	LPUART0_RX	FTM0_CH6	I2C3_SDA	FXIO0_D11	EMVSIM0_IO	JTAG_TDI	
52	38	J7	K6	PTA2	JTAG_TDO/ TRACE_SWO	TSI0_CH3	PTA2	LPUART0_TX	FTM0_CH7	I2C3_SCL	FXIO0_D12	EMVSIM0_PD	JTAG_TDO/ TRACE_SWO	
53	39	H9	L6	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	LPUART0_RTS_b	FTM0_CH0		FXIO0_D13	EMVSIM0_RST	JTAG_TMS/ SWD_DIO	
54	40	J8	H6	PTA4/ LLWU_P3	NMI_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1		FXIO0_D14	EMVSIM0_VCCEN	NMI_b	

144 LQFP	100 LQFP	121 XFBGA	121 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	QSPI_SIP_MODE
76	—	—	—	PTA25	DISABLED		PTA25	EMVSIM0_IO				FB_A28		
77	—	—	—	PTA26	DISABLED		PTA26	EMVSIM0_PD				FB_A27		
78	—	—	—	PTA27	DISABLED		PTA27	EMVSIM0_RST				FB_A26		
79	—	—	—	PTA28	DISABLED		PTA28	EMVSIM0_VCCEN				FB_A25		
80	—	H11	J2	PTA29	DISABLED		PTA29					FB_A24		
81	53	G11	J3	PTB0/LLWU_P5	ADC0_SE8/TSI0_CH0	ADC0_SE8/TSI0_CH0	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0		SDRAM_CAS_b	FTM1_QD_PHA/TPM1_CH0	FXIO0_D0	
82	54	G10	H2	PTB1	ADC0_SE9/TSI0_CH6	ADC0_SE9/TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1		SDRAM_RAS_b	FTM1_QD_PHB/TPM1_CH1	FXIO0_D1	
83	55	G9	H1	PTB2	ADC0_SE12/TSI0_CH7	ADC0_SE12/TSI0_CH7	PTB2	I2C0_SCL	LPUART0_RTS_b		SDRAM_WE	FTM0_FLT3	FXIO0_D2	
84	56	G8	H3	PTB3	ADC0_SE13/TSI0_CH8	ADC0_SE13/TSI0_CH8	PTB3	I2C0_SDA	LPUART0_CTS_b		SDRAM_CS0_b	FTM0_FLT0	FXIO0_D3	
85	—	B11	H4	PTB4	DISABLED		PTB4	EMVSIM1_IO			SDRAM_CS1_b	FTM1_FLT0		
86	—	C11	G1	PTB5	DISABLED		PTB5	EMVSIM1_CLK				FTM2_FLT0		
87	—	F11	G2	PTB6	DISABLED		PTB6	EMVSIM1_VCCEN			FB_AD23/SDRAM_D23			
88	—	E11	G3	PTB7	DISABLED		PTB7	EMVSIM1_PD			FB_AD22/SDRAM_D22			
89	—	D11	G4	PTB8	DISABLED		PTB8	EMVSIM1_RST	LPUART3_RTS_b		FB_AD21/SDRAM_D21			
90	57	E10	G5	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART3_CTS_b		FB_AD20/SDRAM_D20			
91	58	D10	F1	PTB10	DISABLED		PTB10	SPI1_PCS0	LPUART3_RX	I2C2_SCL	FB_AD19/SDRAM_D19	FTM0_FLT1	FXIO0_D4	
92	59	C10	F2	PTB11	DISABLED		PTB11	SPI1_SCK	LPUART3_TX	I2C2_SDA	FB_AD18/SDRAM_D18	FTM0_FLT2	FXIO0_D5	
93	60	L6	F5	VSS	VSS	VSS								
94	61	E7	G6	VDD	VDD	VDD								

5.2 Recommended connection for unused analog and digital pins

Table 65 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 65. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DAC0_OUT, DAC1_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Analog	PTx/TSIOx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOUT33	Tie to input and ground through 10kΩ	Tie to input and ground through 10kΩ
USB	VREGIN	Tie to output and ground through 10kΩ	Tie to output and ground through 10kΩ
USB	USB0_VSS	Always connect to VSS	Always connect to VSS
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential

Table continues on the next page...

Table 65. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K82 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

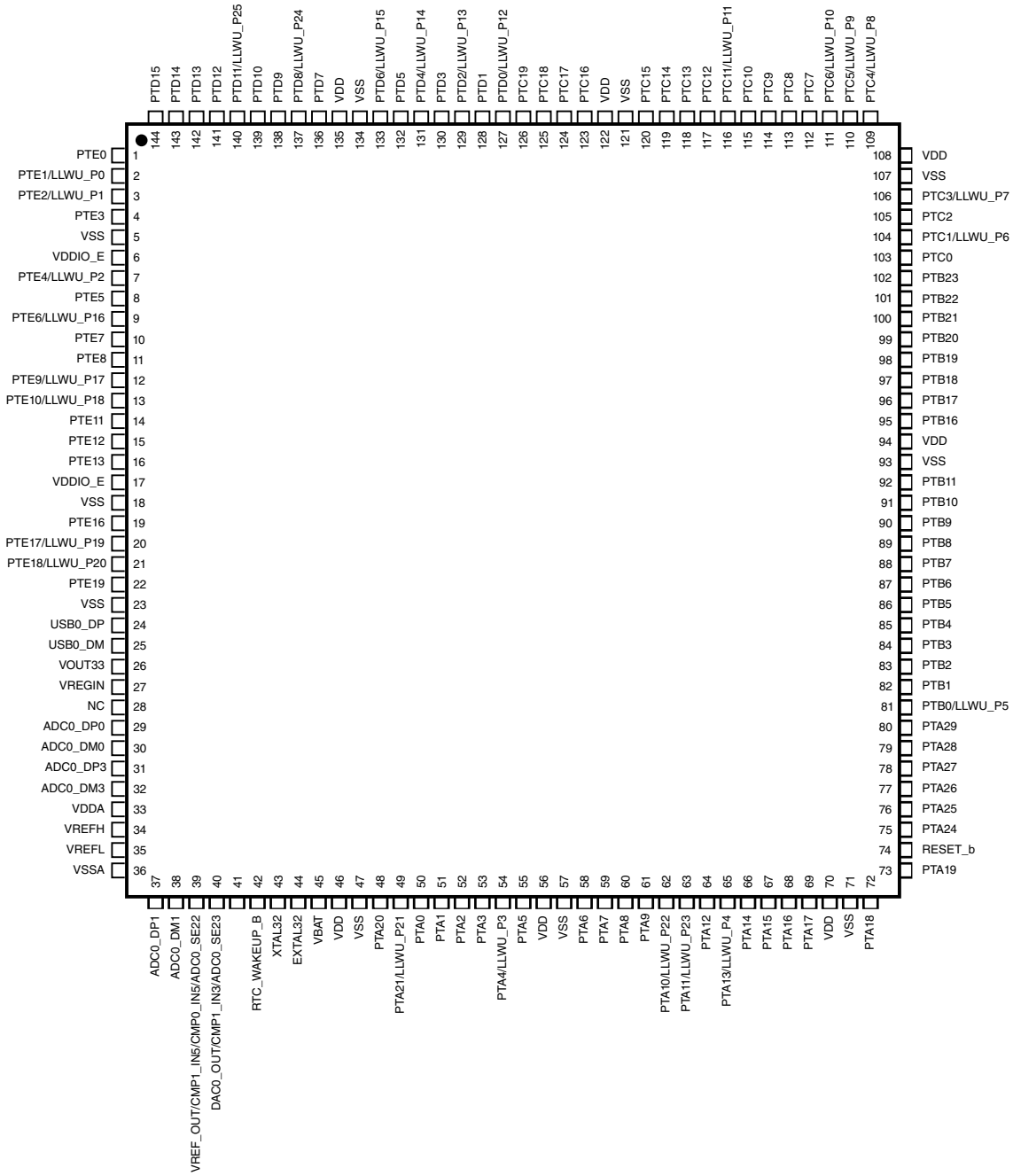


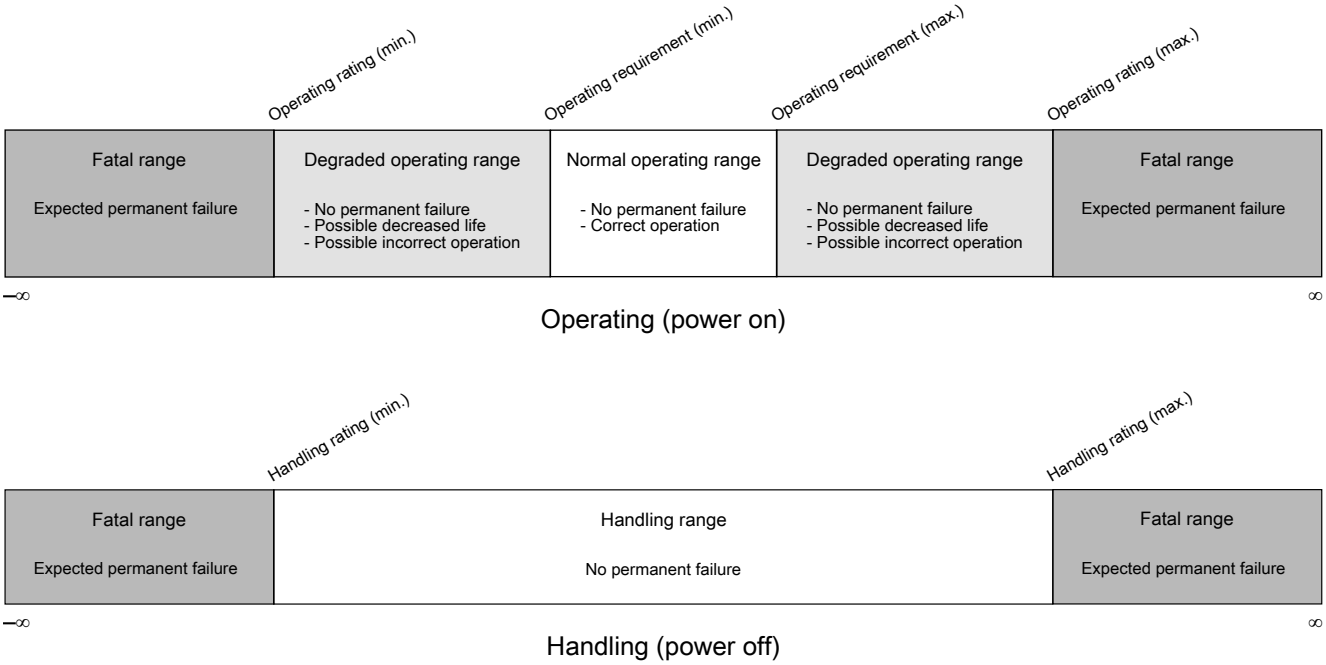
Figure 47. K82 144 LQFP Pinout Diagram

NOTE

The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.