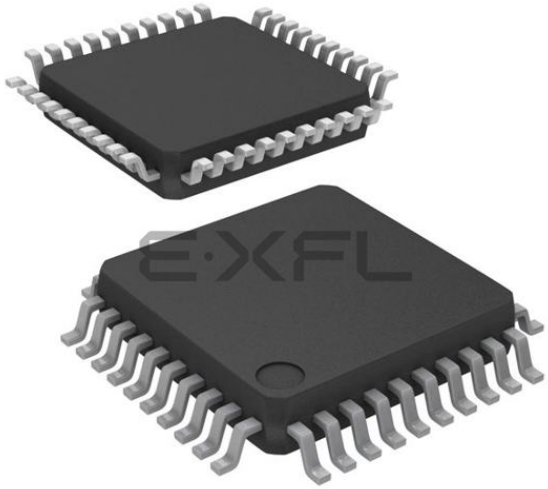
Renesas Electronics America Inc - R5F21103DFP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	SIO, UART/USART
Peripherals	LED, WDT
Number of I/O	22
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21103dfp-u0

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REJ03B0035-0160
Rev.1.60
Jan 27, 2006

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 “Product List”
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Input capture circuit)
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 8 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	Internal: 9 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator
	Oscillation stop detection function	Main clock oscillation stop detection function
Electrical characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Power consumption	Typ. 8mA (VCC = 5.0 V, (f(XIN) = 16MHz) Typ. 5mA (VCC = 3.0 V, (f(XIN) = 10MHz) Typ. 35µA (VCC = 3.0 V, Wait mode, Peripheral clock off) Typ. 0.7µA (VCC = 3.0 V, Stop mode)
Flash memory	Program/erase supply voltage	VCC = 2.7 to 5.5 V
	Program/erase endurance	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

1.4 Product Information

Table 1.2 lists the product inforamation.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21102FP	8K bytes	512 bytes	PLQP0032GB-A	Flash memory version
R5F21103FP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104FP	16K bytes	1K bytes	PLQP0032GB-A	
R5F21102DFP	8K bytes	512 bytes	PLQP0032GB-A	D version
R5F21103DFP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104DFP	16K bytes	1K bytes	PLQP0032GB-A	

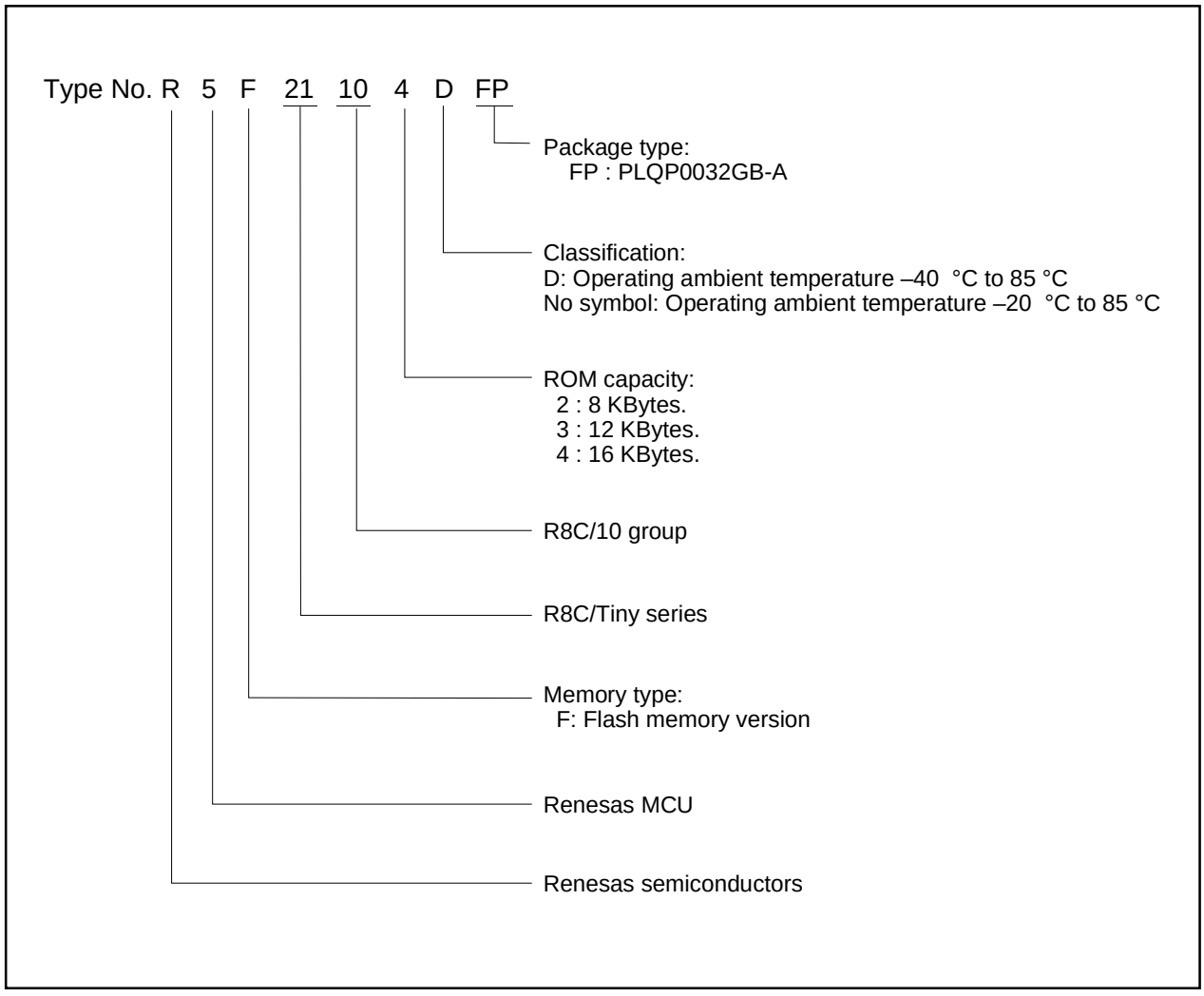
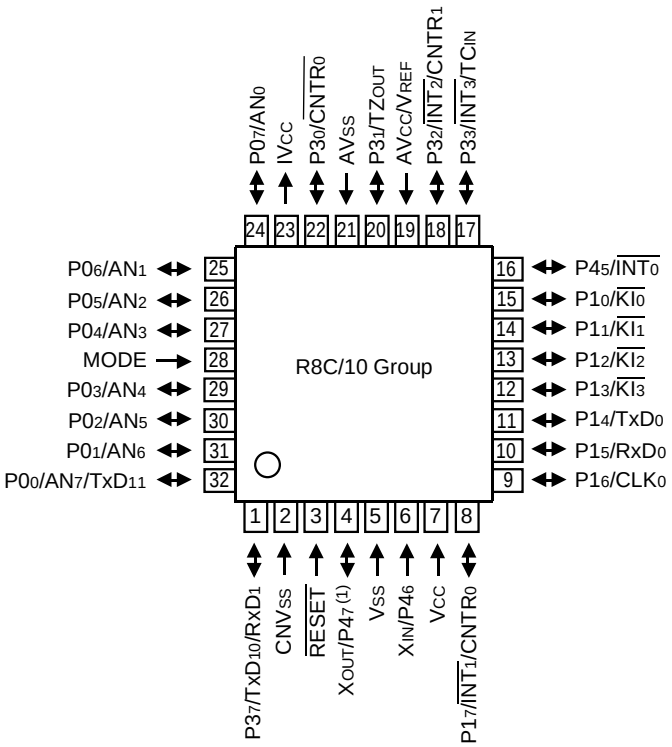


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignment

Figure 1.3 shows the pin Assignments (top view).

PIN CONFIGURATION (top view)



NOTES:
1. P4₇ functions only as an input port.
2. When using On-chip debugger, do not use pins P0₀/AN₇/TxD₁₁ and P3₇/TxD₁₀/RxD₁.
3. Do not connect IVcc to Vcc.

Package: PLQP0032GB-A (32P6U-A)

Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μF). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN7	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only.

3. Memory

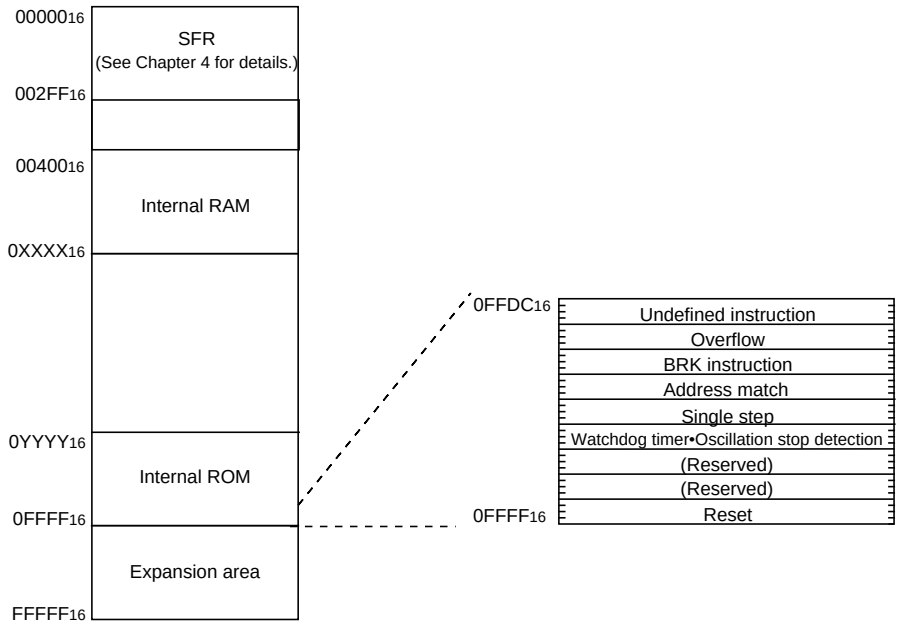
Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated lower addresses beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated addresses $0FFDC_{16}$ to $0FFFF_{16}$. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated addresses 00400_{16} to $007FF_{16}$. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000_{16} to $002FF_{16}$. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES :

1. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY₁₆	Size	Address 0XXXX₁₆
R5F21104FP, R5F21104DFP	16K bytes	0C000₁₆	1K bytes	007FF₁₆
R5F21103FP, R5F21103DFP	12K bytes	0D000₁₆	768 bytes	006FF₁₆
R5F21102FP, R5F21102DFP	8K bytes	0E000₁₆	512 bytes	005FF₁₆

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[(1)]

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	XXXX0X00₂
0005₁₆	Processor mode register 1	PM1	00XXX0X0₂
0006₁₆	System clock control register 0	CM0	01101000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	00XXX000₂
000B₁₆			
000C₁₆	Oscillation stop detection register	OCD	00000100₂
000D₁₆	Watchdog timer reset register	WDTR	XX₁₆
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00011111₂
0010₁₆ 0011₁₆ 0012₁₆	Address match interrupt register 0	RMAD0	00₁₆ 00₁₆ X0₁₆
0013₁₆			
0014₁₆ 0015₁₆ 0016₁₆	Address match interrupt register 1	RMAD1	00₁₆ 00₁₆ X0₁₆
0017₁₆			
0018₁₆			
0019₁₆			
001A₁₆			
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	$\overline{\text{INT0}}$ input filter select register	INT0F	XXXXX000₂
001F₁₆			
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

NOTES:
1. Blank spaces are reserved. No access is allowed.
X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y register	PREY	FF₁₆
0082₁₆	Timer Y secondary register	TYSC	FF₁₆
0083₁₆	Timer Y primary register	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z register	PREZ	FF₁₆
0086₁₆	Timer Z secondary register	TZSC	FF₁₆
0087₁₆	Timer Z primary register	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X register	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆ 0091₁₆	Timer C register	TC	00₁₆ 00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆ 009D₁₆	Capture register	TM0	00₁₆ 00₁₆
009E₁₆			
009F₁₆			
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate generator	U0BRG	XX₁₆
00A2₁₆ 00A3₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6₁₆ 00A7₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate generator	U1BRG	XX₁₆
00AA₁₆ 00AB₁₆	UART1 transmit buffer register	U1TB	XX₁₆ XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE₁₆ 00AF₁₆	UART1 receive buffer register	U1RB	XX₁₆ XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

NOTES:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0₁₆	AD register	AD	XXXXXXXX₂
00C1₁₆			XXXXXXXX₂
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆	AD control register 2	ADCON2	00₁₆
00D5₁₆			
00D6₁₆	AD control register 0	ADCON0	00000XXX₂
00D7₁₆	AD control register 1	ADCON1	00₁₆
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆	Port P0 register	P0	XX₁₆
00E1₁₆	Port P1 register	P1	XX₁₆
00E2₁₆	Port P0 direction register	PD0	00₁₆
00E3₁₆	Port P1 direction register	PD1	00₁₆
00E4₁₆			
00E5₁₆	Port P3 register	P3	XX₁₆
00E6₁₆			
00E7₁₆	Port P3 direction register	PD3	00₁₆
00E8₁₆	Port P4 register	P4	XX₁₆
00E9₁₆			
00EA₁₆	Port P4 direction register	PD4	00₁₆
00EB₁₆			
00EC₁₆			
00ED₁₆			
00EE₁₆			
00EF₁₆			
00F0₁₆			
00F1₁₆			
00F2₁₆			
00F3₁₆			
00F4₁₆			
00F5₁₆			
00F6₁₆			
00F7₁₆			
00F8₁₆			
00F9₁₆			
03FA₁₆			
00FB₁₆			
00FC₁₆	Pull-up control register 0	PUR0	00XX0000₂
00FD₁₆	Pull-up control register 1	PUR1	XXXXXX0X₂
00FE₁₆	Port P1 drive capacity control register	DRR	00₁₆
00FF₁₆			
≈			≈
01B3₁₆	Flash memory control register 4	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1	FMR1	0100XX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0	FMR0	00000001₂

NOTES:
1. Blank columns, 0100₁₆ to 01B2₁₆ and 01B8₁₆ to 02FF₁₆ are all reserved. No access is allowed.

X : Undefined

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} =V_{CC}	—	—	10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)		—	±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=V_{CC}	10	—	40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	—	—	µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8	—	—	µs
V_{REF}	Reference voltage			—	V_{CC}(4)	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
–	A/D operating clock frequency(2)	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:
1. V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f_{AD} exceeds 10 MHz, divide the f_{AD} and hold A/D operating clock frequency (Ø$_{AD}$) 10 MHz or below.
3. If the AVcc is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency (Ø$_{AD}$) f_{AD}/2 or below.
4. Hold Vcc=Vref.

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/erase endurance		100	—	—	times
–	Byte program time		—	50	400	µs
–	Block erase time		—	0.4	9	s
$t_{d(SR-ES)}$	Time delay from suspend request until erase suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase voltage		2.7	—	5.5	V
–	Read voltage		2.7	—	5.5	V
–	Program, Erase temperature		0	—	60	°C
–	Data hold time(2)	Ambient temperature=55 °C	20	—	—	year

NOTES:
1. V_{CC1}=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C, unless otherwise specified.
2. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on(2)		1	—	2000	µs
td(R-S)	STOP release time(3)		—	—	150	µs

NOTES:
1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

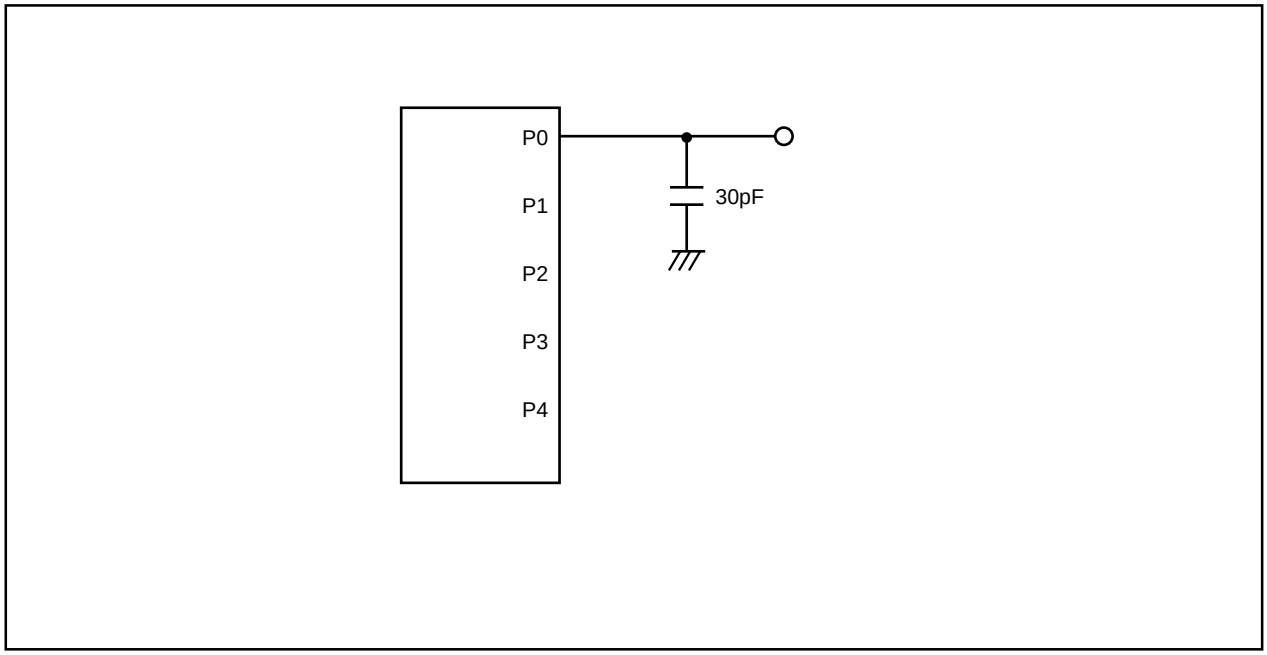


Figure 5.1 Port P0 to P4 measurement circuit

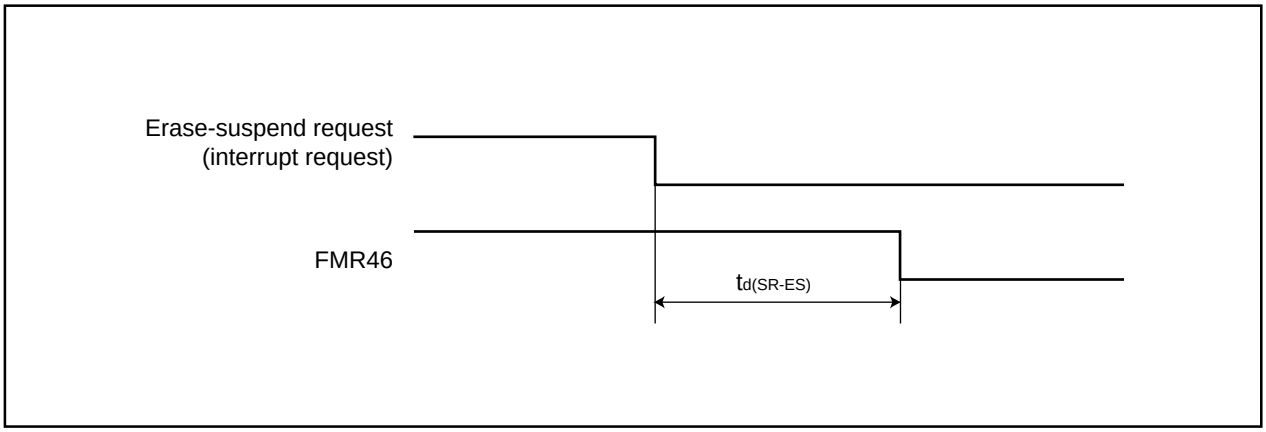


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA	V_{CC}-2.0		V_{CC}	V
			I_{OH}=-200µA	V_{CC}-0.3		V_{CC}	V
		X_{OUT}	Drive capacity HIGH I_{OH}=-1 mA	V_{CC}-2.0		V_{CC}	V
			Drive capacity LOW I_{OH}=-500µA	V_{CC}-2.0		V_{CC}	V
V_{OL}	"L" output voltage	Except P10 to P17, X_{OUT}	I_{OL}= 5 mA			2.0	V
			I_{OL}= 200 µA			0.45	V
		P10 to P17	Drive capacity HIGH I_{OL}= 15 mA			2.0	V
			Drive capacity LOW I_{OL}= 5 mA			2.0	V
			Drive capacity LOW I_{OL}= 200 µA			0.45	V
		X_{OUT}	Drive capacity HIGH I_{OL}= 1 mA			2.0	V
			Drive capacity LOW I_{OL}=500µA			2.0	V
V_{T+}-V_{T-}	Hysteresis	INT_0, INT_1, INT_2, INT_3, KI_0, KI_1, KI_2, KI_3, $CNTR_0$, $CNTR_1$, TC_{IN}, RxD_0, RxD_1, P45		0.2		1.0	V
		RESET		0.2		2.2	V
I_{IH}	"H" input current		V_I=5V			5.0	µA
I_{IL}	"L" input current		V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V	30	50	167	kΩ
R_{IXIN}	Feedback resistance	X_{IN}			1.0		MΩ
f_{RING}	On-chip oscillator frequency			40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC}=AV_{CC}=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.7 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}		High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
				X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
			On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	µA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation	—	40	80	µA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off	—	38	76	µA
			Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at Topr = 25 °C) [V_{CC}=5V]

Table 5.8 X_{IN} input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XIN)}$	X_{IN} input cycle time	62.5	–	ns
$t_{WH(XIN)}$	X_{IN} input HIGH pulse width	30	–	ns
$t_{WL(XIN)}$	X_{IN} input LOW pulse width	30	–	ns

Table 5.9 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input HIGH pulse width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input LOW pulse width	40	–	ns

Table 5.10 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TCIN)}$	TCIN input cycle time	400(1)	–	ns
$t_{WH(TCIN)}$	TCIN input HIGH pulse width	200(2)	–	ns
$t_{WL(TCIN)}$	TCIN input LOW pulse width	200(2)	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.11 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input HIGH pulse width	100	–	ns
$t_{W(CKL)}$	CLKi input LOW pulse width	100	–	ns
$t_{d(C-Q)}$	TxDi output delay time	–	80	ns
$t_{h(C-Q)}$	TxDi hold time	0	–	ns
$t_{su(D-C)}$	RxDi input setup time	35	–	ns
$t_{h(C-D)}$	RxDi input hold time	90	–	ns

Table 5.12 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input HIGH pulse width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input LOW pulse width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

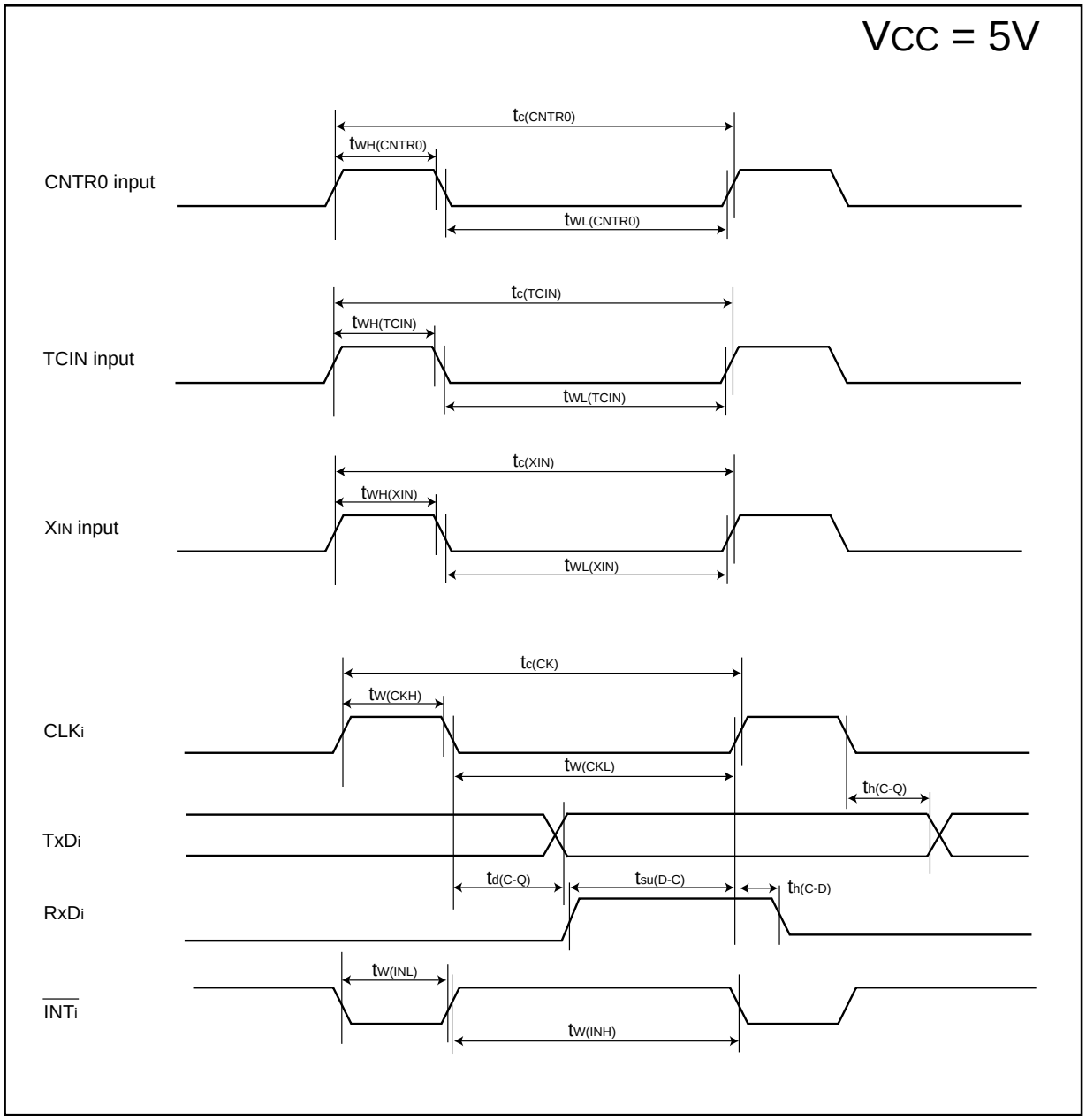


Figure 5.3 Vcc=5V timing diagram

Table 5.14 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	7	12	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	420	800	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation	—	37	74	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off	—	35	70	µA
		Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.7	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc=3V]

Table 5.15 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	100	–	ns
twH(XIN)	XIN input HIGH pulse width	40	–	ns
twL(XIN)	XIN input LOW pulse width	40	–	ns

Table 5.16 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	300	–	ns
twH(CNTR0)	CNTR0 input HIGH pulse width	120	–	ns
twL(CNTR0)	CNTR0 input LOW pulse width	120	–	ns

Table 5.17 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	1200(1)	–	ns
twH(TCIN)	TCIN input HIGH pulse width	600(2)	–	ns
twL(TCIN)	TCIN input LOW pulse width	600(2)	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	300	–	ns
tw(CKH)	CLKi input HIGH pulse width	150	–	ns
tw(CKL)	CLKi input LOW pulse width	150	–	ns
td(C-Q)	TxDi output delay time	–	160	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	55	–	ns
th(C-D)	RxDi input hold time	90	–	ns

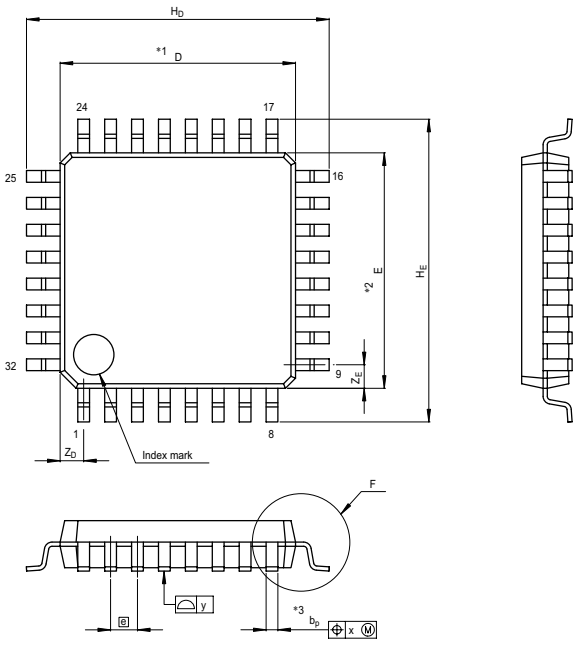
Table 5.19 External interrupt $\overline{INT0}$ input

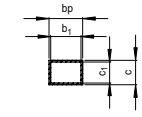
Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	380(1)	–	ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

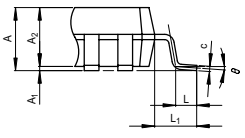
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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