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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	SIO, UART/USART
Peripherals	LED, WDT
Number of I/O	22
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21103fp-u0

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1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

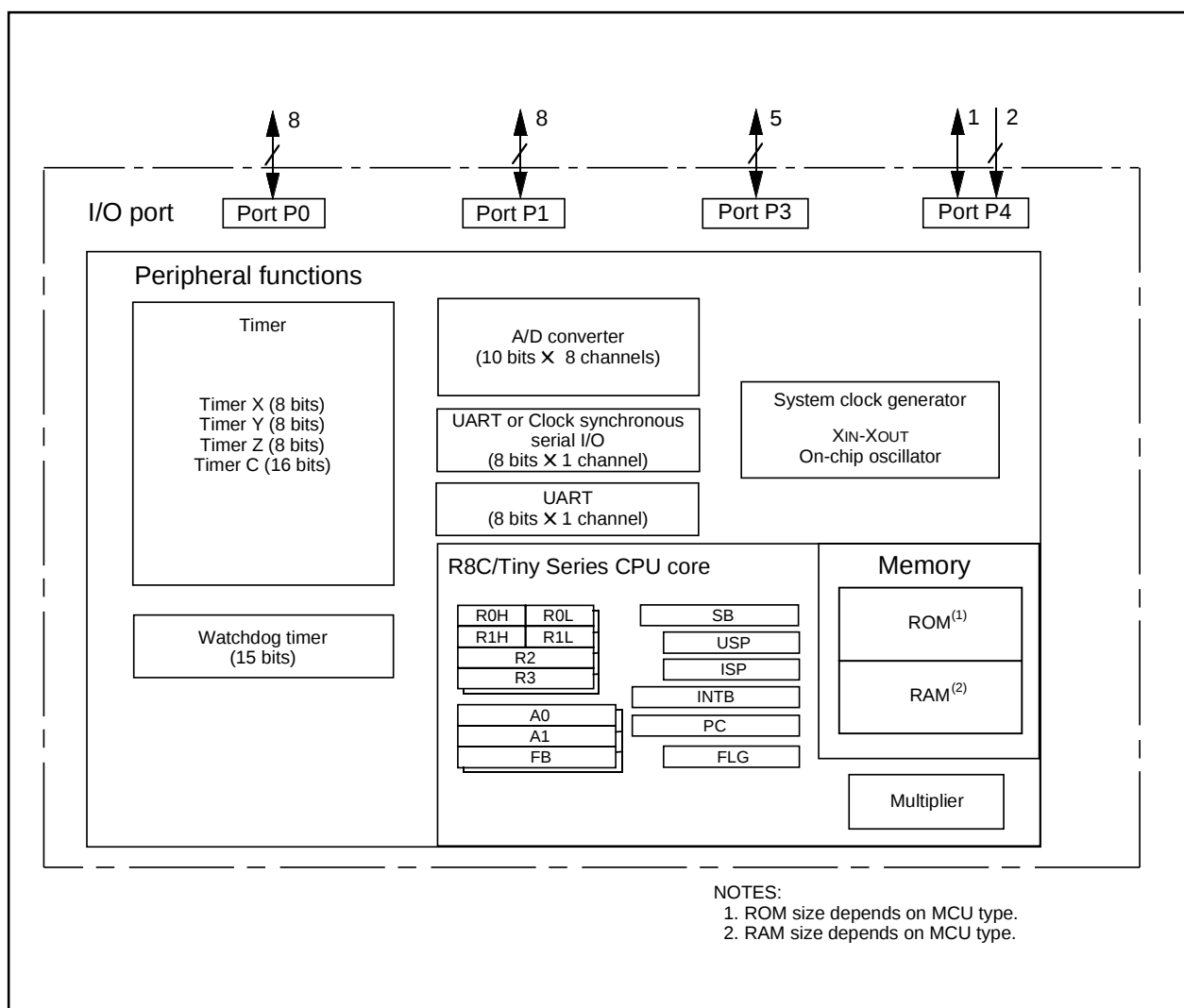


Figure 1.1 Block Diagram

1.5 Pin Assignment

Figure 1.3 shows the pin Assignments (top view).

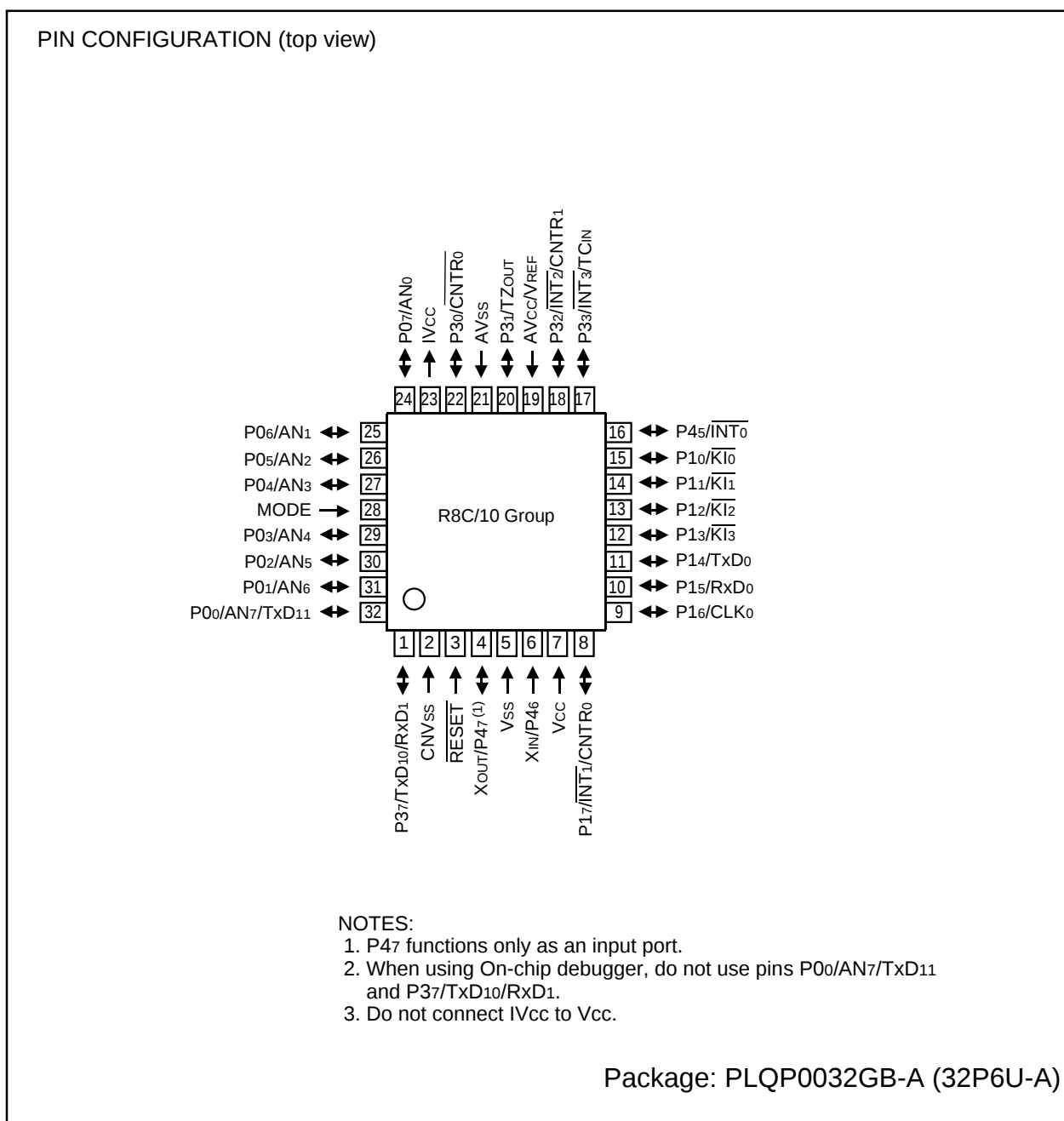


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN7	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

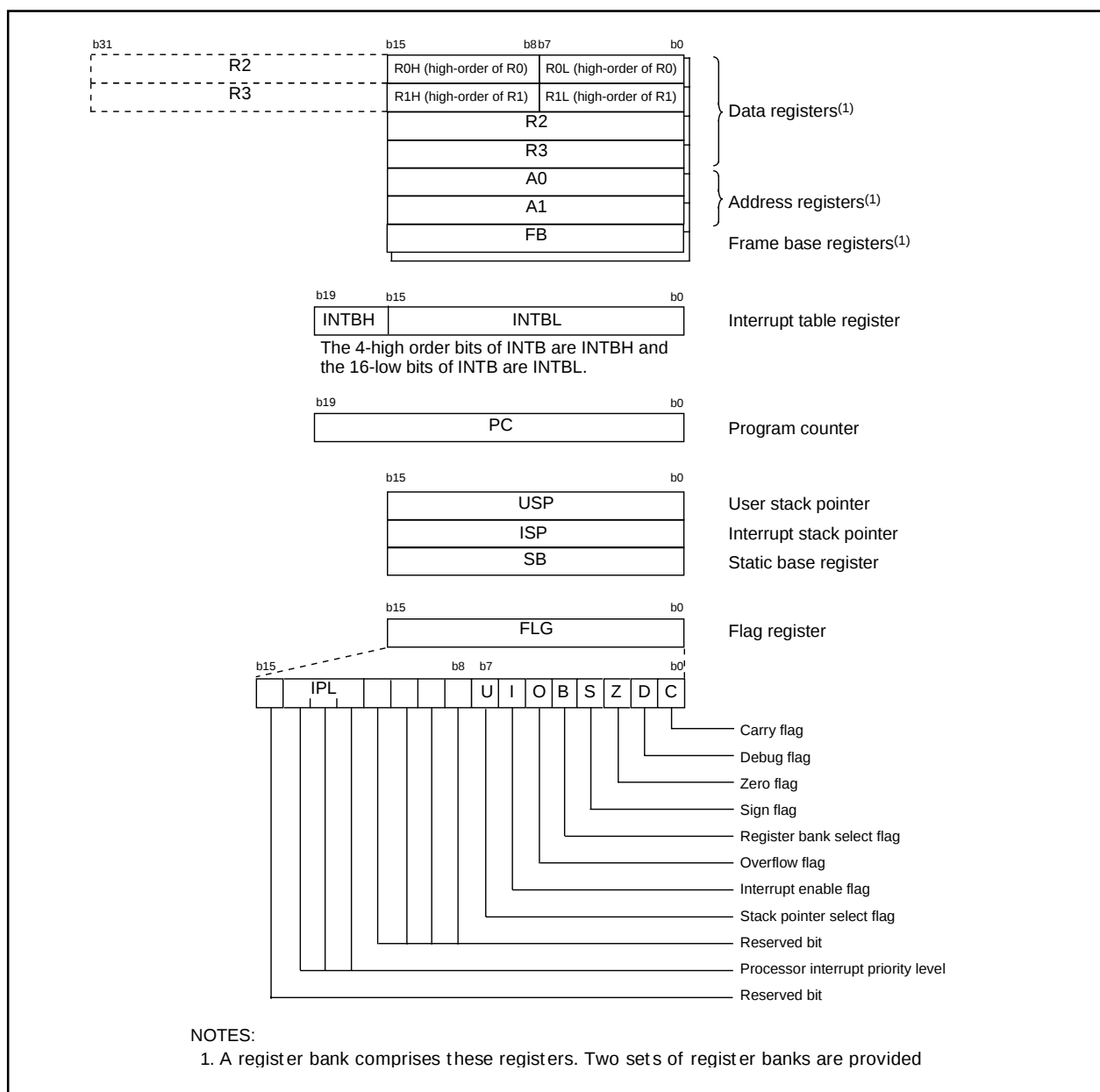


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated lower addresses beginning with address 0C000₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

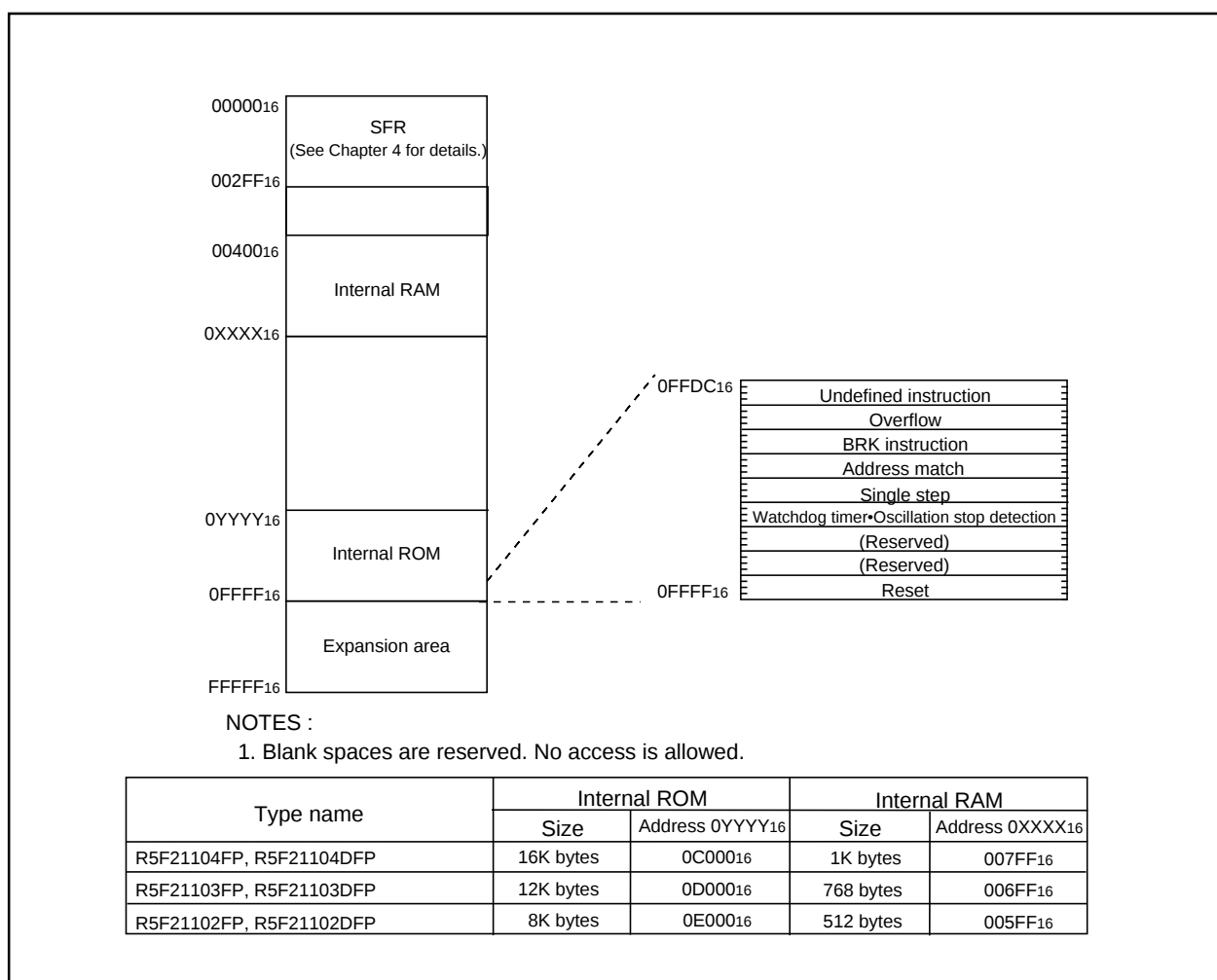


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	XXXX0X002
0005 ₁₆	Processor mode register 1	PM1	00XXX0X02
0006 ₁₆	System clock control register 0	CM0	011010002
0007 ₁₆	System clock control register 1	CM1	001000002
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A ₁₆	Protect register	PRCR	00XXX0002
000B ₁₆			
000C ₁₆	Oscillation stop detection register	OCD	000001002
000D ₁₆	Watchdog timer reset register	WDTR	XX16
000E ₁₆	Watchdog timer start register	WDTS	XX16
000F ₁₆	Watchdog timer control register	WDC	000111112
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

NOTES:

- Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)⁽¹⁾

Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	00 ₁₆
0081 ₁₆	Prescaler Y register	PREY	FF ₁₆
0082 ₁₆	Timer Y secondary register	TYSC	FF ₁₆
0083 ₁₆	Timer Y primary register	TYPR	FF ₁₆
0084 ₁₆	Timer Y, Z waveform output control register	PUM	00 ₁₆
0085 ₁₆	Prescaler Z register	PREZ	FF ₁₆
0086 ₁₆	Timer Z secondary register	TZSC	FF ₁₆
0087 ₁₆	Timer Z primary register	TZPR	FF ₁₆
0088 ₁₆			
0089 ₁₆			
008A ₁₆	Timer Y, Z output control register	TYZOC	00 ₁₆
008B ₁₆	Timer X mode register	TXMR	00 ₁₆
008C ₁₆	Prescaler X register	PREX	FF ₁₆
008D ₁₆	Timer X register	TX	FF ₁₆
008E ₁₆	Count source set register	TCSS	00 ₁₆
008F ₁₆			
0090 ₁₆	Timer C register	TC	00 ₁₆
0091 ₁₆			00 ₁₆
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	00 ₁₆
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	00 ₁₆
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	00 ₁₆
009B ₁₆	Timer C control register 1	TCC1	00 ₁₆
009C ₁₆	Capture register	TM0	00 ₁₆
009D ₁₆			00 ₁₆
009E ₁₆			
009F ₁₆			
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
00A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆
00A3 ₁₆			XX ₁₆
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
00A6 ₁₆	UART0 receive buffer register	U0RB	XX ₁₆
00A7 ₁₆			XX ₁₆
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
00A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
00AA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
00AB ₁₆			XX ₁₆
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
00AE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
00AF ₁₆			XX ₁₆
00B0 ₁₆	UART transmit/receive control register 2	UCON	00 ₁₆
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

NOTES:

1. Blank spaces are reserved. No access is allowed.

X : Undefined

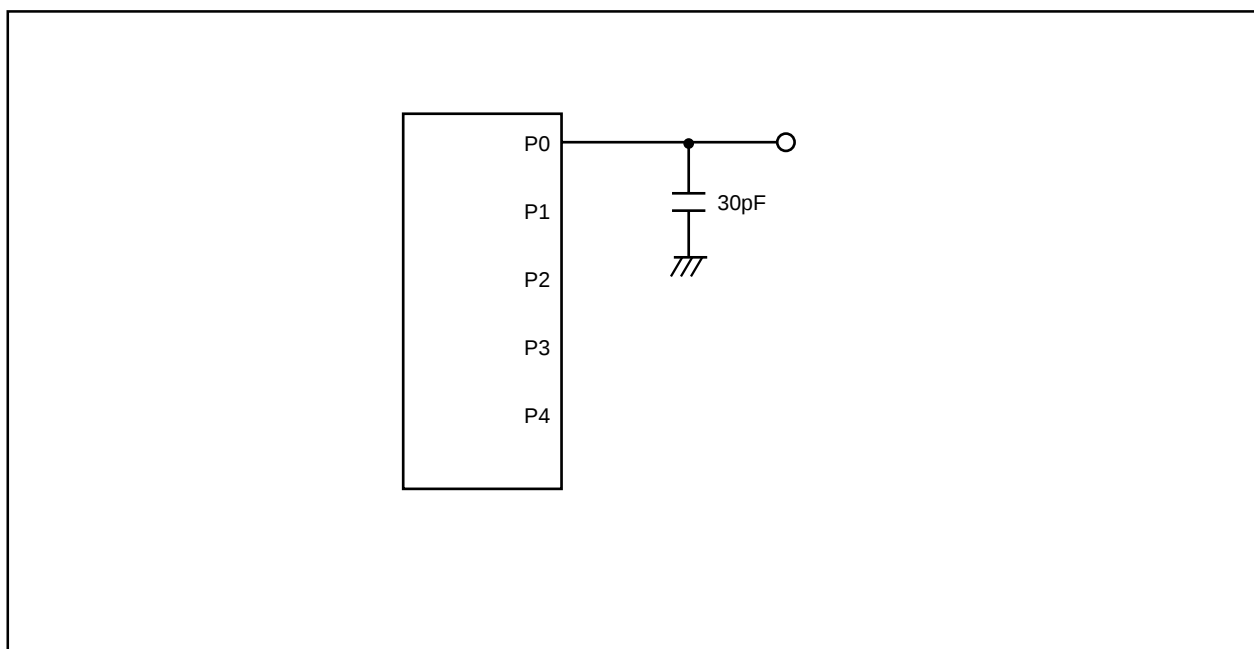
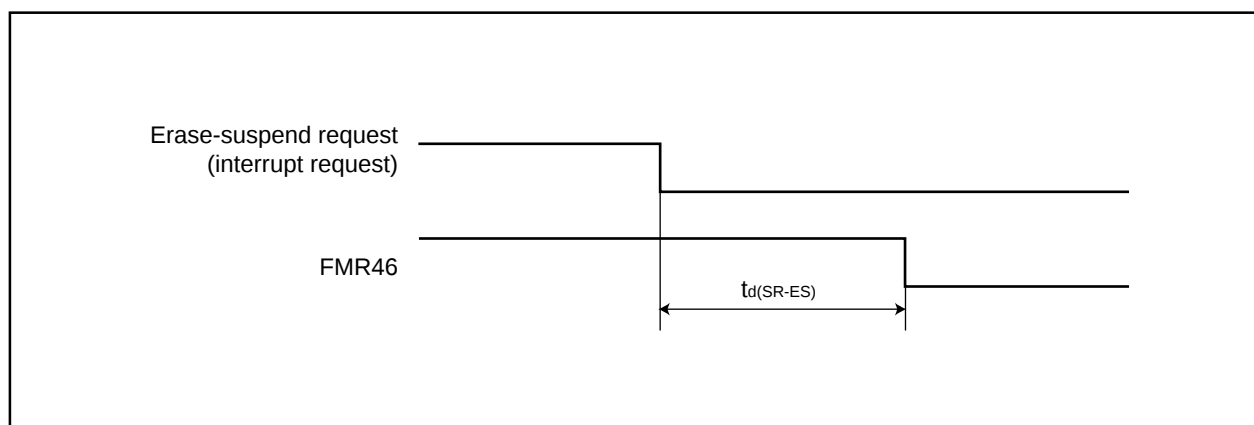
Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0 ₁₆	AD register	AD	XXXXXXXX ₂
00C1 ₁₆			XXXXXXXX ₂
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆	AD control register 2	ADCON2	0016
00D5 ₁₆			
00D6 ₁₆	AD control register 0	ADCON0	00000XXX ₂
00D7 ₁₆	AD control register 1	ADCON1	0016
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆	Port P0 register	P0	XX ₁₆
00E1 ₁₆	Port P1 register	P1	XX ₁₆
00E2 ₁₆	Port P0 direction register	PD0	0016
00E3 ₁₆	Port P1 direction register	PD1	0016
00E4 ₁₆			
00E5 ₁₆	Port P3 register	P3	XX ₁₆
00E6 ₁₆			
00E7 ₁₆	Port P3 direction register	PD3	0016
00E8 ₁₆	Port P4 register	P4	XX ₁₆
00E9 ₁₆			
00EA ₁₆	Port P4 direction register	PD4	0016
00EB ₁₆			
00EC ₁₆			
00ED ₁₆			
00EE ₁₆			
00EF ₁₆			
00F0 ₁₆			
00F1 ₁₆			
00F2 ₁₆			
00F3 ₁₆			
00F4 ₁₆			
00F5 ₁₆			
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆			
00F9 ₁₆			
03FA ₁₆			
00FB ₁₆			
00FC ₁₆	Pull-up control register 0	PUR0	00XX0000 ₂
00FD ₁₆	Pull-up control register 1	PUR1	XXXXXXXX ₂
00FE ₁₆	Port P1 drive capacity control register	DRR	0016
00FF ₁₆			
~~~~~			
01B3 ₁₆	Flash memory control register 4	FMR4	01000000 ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1	FMR1	0100XX0X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0	FMR0	00000001 ₂

NOTES:

1. Blank columns, 0100₁₆ to 01B2₁₆ and 01B8₁₆ to 02FF₁₆ are all reserved. No access is allowed.

X : Undefined

**Figure 5.1 Port P0 to P4 measurement circuit****Figure 5.2 Time delay from Suspend Request until Erase Suspend**

**Table 5.6 Electrical Characteristics (1) [Vcc=5V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-5mA	Vcc-2.0		Vcc	V
			IOH=-200μA	Vcc-0.3		Vcc	V
	XOUT		Drive capacity HIGH IOH=-1 mA	Vcc-2.0		Vcc	V
			Drive capacity LOW IOH=-500μA	Vcc-2.0		Vcc	V
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 5 mA			2.0	V
			IOL= 200 μA			0.45	V
	P10 to P17		Drive capacity HIGH IOL= 15 mA			2.0	V
			Drive capacity LOW IOL= 5 mA			2.0	V
			Drive capacity LOW IOL= 200 μA			0.45	V
	XOUT		Drive capacity HIGH IOL= 1 mA			2.0	V
			Drive capacity LOW IOL=500μA			2.0	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45		0.2		1.0	V
		RESET		0.2		2.2	V
IiH	"H" input current		Vi=5V			5.0	μA
IiL	"L" input current		Vi=0V			-5.0	μA
RPULLUP	Pull-up resistance		Vi=0V	30	50	167	kΩ
RtXIN	Feedback resistance	XIN			1.0		MΩ
fRING	On-chip oscillator frequency			40	125	250	kHz
VRAM	RAM retention voltage		At stop mode	2.0			V

## NOTES:

1. Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz unless otherwise specified.

**Timing requirements (Unless otherwise noted:  $V_{CC} = 5V$ ,  $V_{SS} = 0V$  at  $T_{opr} = 25\text{ }^{\circ}C$ ) [ $V_{CC}=5V$ ]****Table 5.8 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(XIN)$	XIN input cycle time	62.5	—	ns
$t_{WH}(XIN)$	XIN input HIGH pulse width	30	—	ns
$t_{WL}(XIN)$	XIN input LOW pulse width	30	—	ns

**Table 5.9 CNTR0 input, CNTR1 input,  $\overline{INT2}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(CNTR0)$	CNTR0 input cycle time	100	—	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	40	—	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	40	—	ns

**Table 5.10 TCIN input,  $\overline{INT3}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TCIN)$	TCIN input cycle time	400 ⁽¹⁾	—	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	200 ⁽²⁾	—	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	200 ⁽²⁾	—	ns

**NOTES:**

1. When using the Timer C capture function, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.11 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(CLK)$	CLKi input cycle time	200	—	ns
$t_{W}(CLKH)$	CLKi input HIGH pulse width	100	—	ns
$t_{W}(CLKL)$	CLKi input LOW pulse width	100	—	ns
$t_d(C-Q)$	TxDi output delay time	—	80	ns
$t_h(C-Q)$	TxDi hold time	0	—	ns
$t_{su}(D-C)$	RxDi input setup time	35	—	ns
$t_h(C-D)$	RxDi input hold time	90	—	ns

**Table 5.12 External interrupt  $\overline{INT0}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W}(\overline{INH})$	$\overline{INT0}$ input HIGH pulse width	250 ⁽¹⁾	—	ns
$t_{W}(\overline{INL})$	$\overline{INT0}$ input LOW pulse width	250 ⁽²⁾	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.

**Table 5.13 Electrical Characteristics (3) [Vcc=3V]**

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA		Vcc-0.5	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH=-0.1 mA	Vcc-0.5	—	Vcc	V
			Drive capacity LOW	IOH=-50 μA	Vcc-0.5	—	Vcc	V
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	IOL= 2 mA	—	—	0.5	V
			Drive capacity LOW	IOL= 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	IOL= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	IOL=50 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
IiH	"H" input current		Vi=3V		—	—	4.0	μA
IiL	"L" input current		Vi=0V		—	—	-4.0	μA
RPULLUP	Pull-up resistance		Vi=0V		66	160	500	kΩ
RXIN	Feedback resistance	XIN			—	3.0	—	MΩ
fRING	On-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

## NOTES:

1. Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

**Table 5.14 Electrical Characteristics (4) [Vcc=3V]**

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I _{cc}	Power supply current (V _{CC1} =2.7 to 3.3V)  In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	7	12	mA
			X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
			X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	420	800	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation	—	37	74	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off	—	35	70	μA
		Stop mode	Main clock off, T _{opr} = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.7	3.0	μA

## NOTES:

1. Timer Y is operated with timer mode.

2. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

**Timing requirements (Unless otherwise noted:  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_{opr} = 25\text{ }^{\circ}C$ ) [ $V_{CC}=3V$ ]****Table 5.15  $X_{IN}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(X_{IN})$	$X_{IN}$ input cycle time	100	—	ns
$t_{WH}(X_{IN})$	$X_{IN}$ input HIGH pulse width	40	—	ns
$t_{WL}(X_{IN})$	$X_{IN}$ input LOW pulse width	40	—	ns

**Table 5.16 CNTR0 input, CNTR1 input,  $\overline{INT2}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	CNTR0 input cycle time	300	—	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	120	—	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	120	—	ns

**Table 5.17 TCIN input,  $\overline{INT3}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	TCIN input cycle time	1200 ⁽¹⁾	—	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	600 ⁽²⁾	—	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	600 ⁽²⁾	—	ns

**NOTES:**

1. When using the Timer C capture function, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.18 Serial Interface**

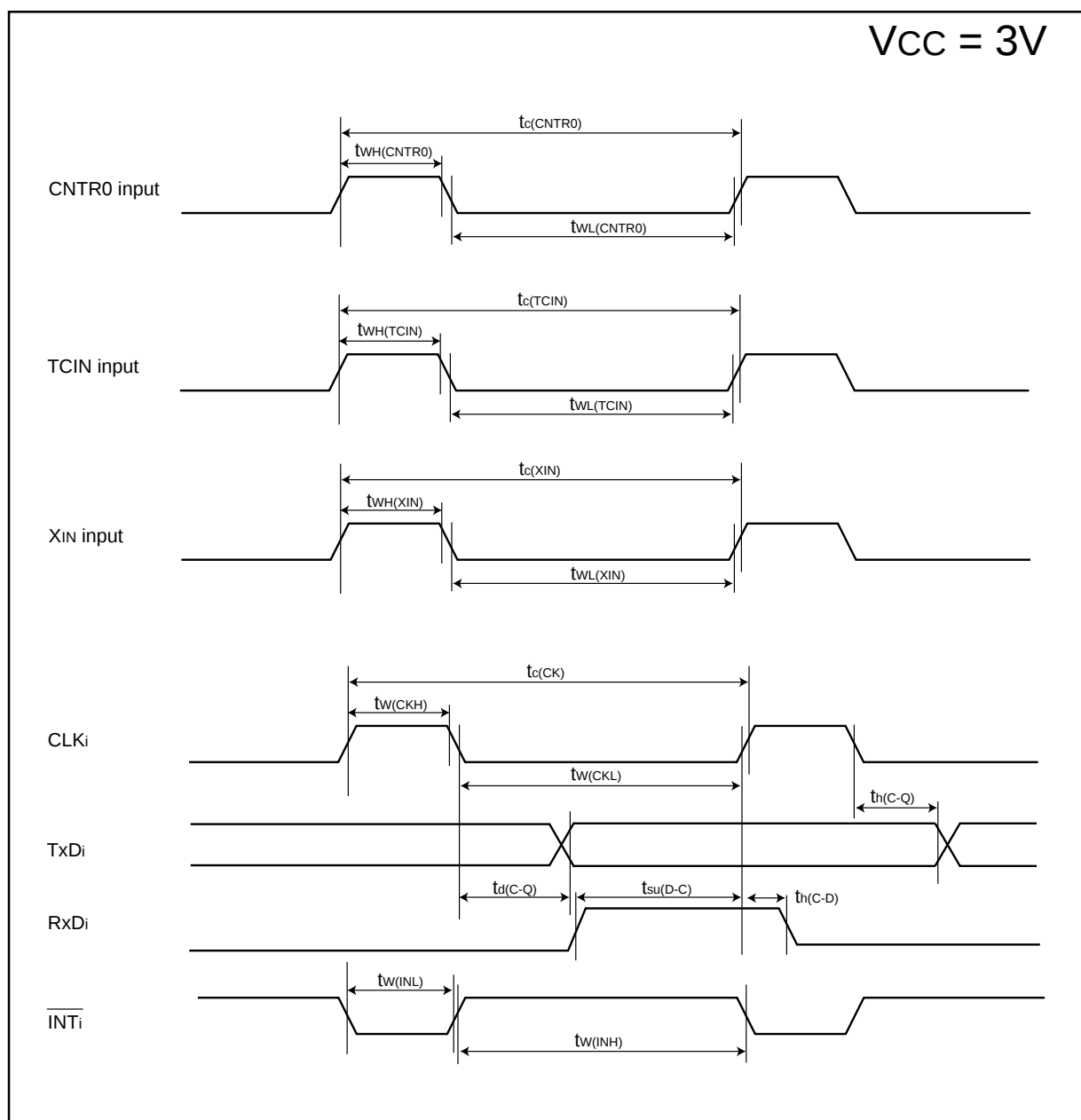
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CK)$	CLKi input cycle time	300	—	ns
$t_W(CKH)$	CLKi input HIGH pulse width	150	—	ns
$t_W(CKL)$	CLKi input LOW pulse width	150	—	ns
$t_d(C-Q)$	TxDi output delay time	—	160	ns
$t_h(C-Q)$	TxDi hold time	0	—	ns
$t_{su}(D-C)$	RxDi input setup time	55	—	ns
$t_h(C-D)$	RxDi input hold time	90	—	ns

**Table 5.19 External interrupt  $\overline{INT0}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_W(INH)$	$\overline{INT0}$ input HIGH pulse width	380 ⁽¹⁾	—	ns
$t_W(INL)$	$\overline{INT0}$ input LOW pulse width	380 ⁽²⁾	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.

Figure 5.4  $V_{CC}=3V$  timing diagram

REVISION HISTORY	R8C/10 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 12 14	Table 1.1: Shortest instruction execution time and $f(X_{IN})$ changed Figure 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ Table 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ The value of Time C register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 14 15 16 18  19 20 21 22  23 24	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Table 5.2: Note 3 and Note 4 deleted tsamp in Table 5.3 deleted Figure 5.1 added Table 5.7: Vcc changed from "4.2 to 5.5V" to "3.3V to 5.5V", on-chip oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, data added and modified Table 5.8 to Table 5.12 added Figure 5.2 added Table 5.13: Note 1, $f(BCLK)=5\text{ MHz}$ changed to 10 MHz Table 5.14: on-chip oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, data added and modified Table 5.15 to Table 5.19 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.40	Sep 30, 2004	All pages 2 5 6 10-13 12 14 15 17 18 19 21 22 23	Words standardized (on-chip oscillator, serial interface, A/D) Table 1.1 revised Figure 1.3, NOTES 3 added Table 1.3 revised One body sentence in chapter 4 added ; Titles 4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised Table 5.2 revised Table 5.3 revised ; Table 5.4 revised Table 5.6 revised Table 5.7 revised Table 5.8 revised ; Table 5.12 revised Table 5.13 revised Table 5.14 revised Table 5.15 revised ; Table 5.17 revised ; Table 5.19 revised
1.50	Apr.27.2005	4 5 10	Table 1.2, Figure 1.2 package name revised Figure 1.3 package name revised Table 4.1 revised

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