Infineon Technologies - CY9AF315NAPMC-G-MNE2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy9af315napmc-g-mne2

Multi-function Timer (Max 2units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activation compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D converter activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 2units)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32/16bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters.
Operation mode is selectable from the followings for each timer channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from Low-Power Consumption mode.

Interval timer: up to 64s (Max) @ Sub Clock: 32.768kHz

Watch dog Timer (2channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a, "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in low speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except STOP mode.

External Interrupt Controller Unit

- Up to 16 external interrupt input pins.
- Include one non-maskable interrupt (NMI) input pin.

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 fast General Purpose I/O Ports @ 100pin Package
- Some ports are 5V tolerant I/O (MB9AF315MA/NA, MB9AF316MA/NA only)
  Please see "Pin Description" to confirm the corresponding pins.

CRC (Cyclic Redundancy Check) Accelerator

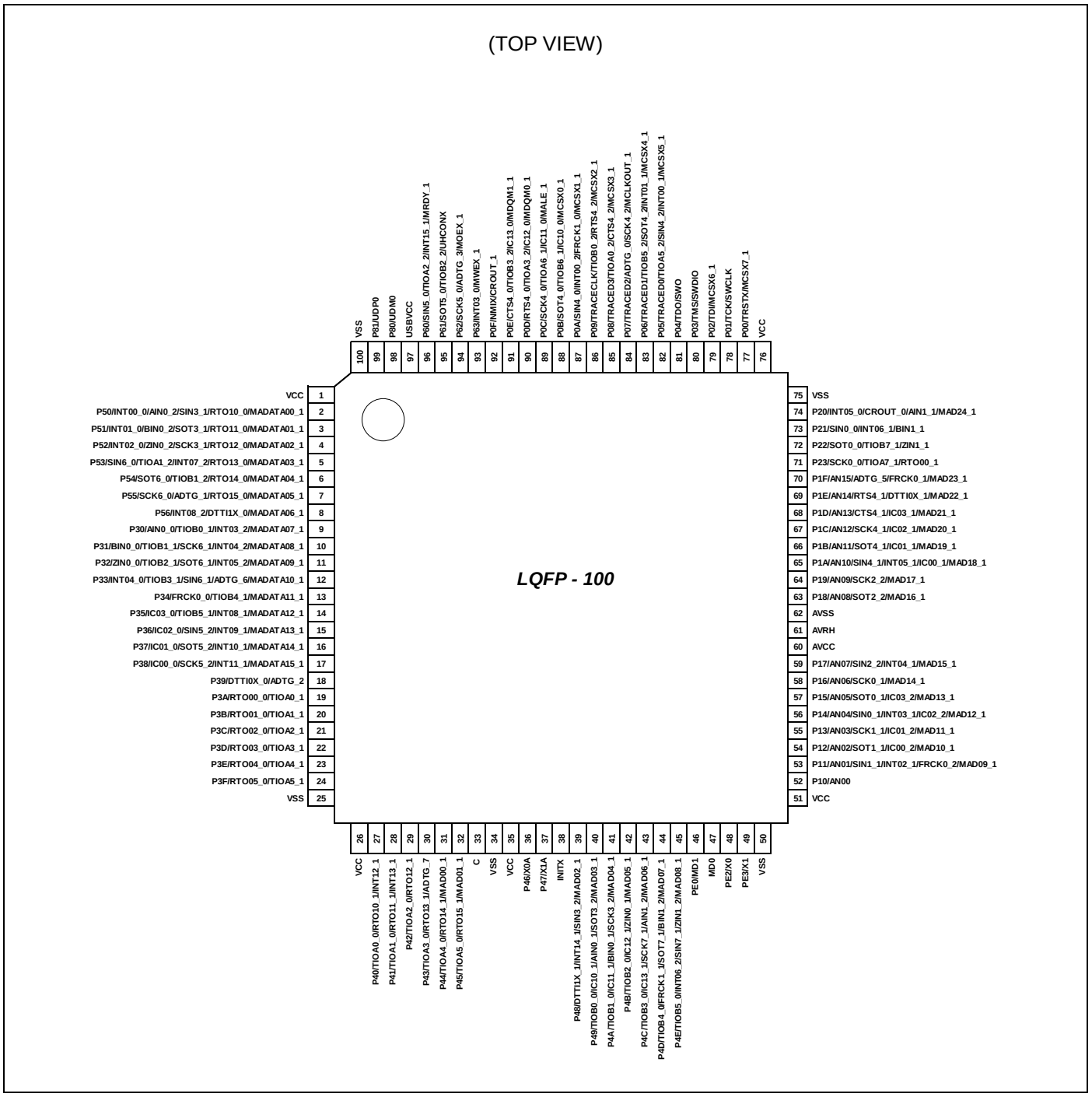
The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

3. Pin Assignment

FPT-100P-M23



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
44	22	J7	34	26	P4D	E / I*	I
					TIOB4_0		
					SOT7_1 (SDA7_1)		
					BIN1_2		
				-	FRCK1_1		
					MAD07_1		
45	23	K8	35	27	P4E	E / I*	I
					TIOB5_0		
					INT06_2		
					SIN7_1		
					ZIN1_2		
				-	MAD08_1		
46	24	K9	36	28	MD1	C	P
					PE0		
47	25	L8	37	29	MD0	J	D
48	26	L9	38	30	X0	A	A
					PE2		
49	27	L10	39	31	X1	A	B
					PE3		
50	28	L11	40	32	VSS	-	
51	29	K11	41	33	VCC	-	
52	30	J11	42	34	P10	F	K
					AN00		
53	31	J10	43	35	P11	F	L
					AN01		
					SIN1_1		
					INT02_1		
					FRCK0_2		
				-	MAD09_1		
54	32	J8	44	36	P12	F	K
					AN02		
					SOT1_1 (SDA1_1)		
					IC00_2		
				-	MAD10_1		
-	-	K10	-	-	VSS	-	
-	-	J9	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
83	61	D9	-	-	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 MCSX4_1	E	F
84	62	A7	66 -	-	P07 ADTG_0 MCLKOUT_1 TRACED2 SCK4_2 (SCL4_2)	E	G
85	63	B7	-	-	P08 TRACED3 TIOA0_2 CTS4_2 MCSX3_1	E	G
86	64	C7	-	-	P09 TRACECLK TIOB0_2 RTS4_2 MCSX2_1	E	G
87	65	D7	67	54 -	P0A SIN4_0 INT00_2 FRCK1_0 MCSX1_1	E / I*	H
88	66	A6	68	55 -	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MCSX0_1	E / I*	I
89	67	B6	69	56 -	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 MALE_1	E / I*	I
-	-	D4	-	-	VSS	-	
-	-	C3	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
90	68	C6	70	-	P0D RTS4_0 TIOA3_2 IC12_0 MDQM0_1	E	I
91	69	A5	71	-	P0E CTS4_0 TIOB3_2 IC13_0 MDQM1_1	E	I
92	70	B5	72	57	P0F NMIX CROUT_1	E	J
93	71	D6	73	-	P63 INT03_0 MWEX_1	E	H
94	72	C5	74	58	P62 SCK5_0 (SCL5_0) ADTG_3	E	I
				-	MOEX_1		
95	73	B4	75	59	P61 SOT5_0 (SDA5_0) TIOB2_2	E	I
96	74	C4	76	60	P60 SIN5_0 TIOA2_2 INT15_1	E / I*	H
				-	MRDY_1		
97	75	A4	77	61	USBVCC	-	
98	76	A3	78	62	P80 UDM0	H	O
99	77	A2	79	63	P81 UDP0	H	O
100	78	A1	80	64	VSS	-	

*: 5V tolerant I/O on MB9AF315MA/NA and MB9AF316MA/NA

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
External Interrupt	INT00_0	External interrupt request 00 input pin	2	80	C1	2	2
	INT00_1		82	60	C8	-	-
	INT00_2		87	65	D7	67	54
	INT01_0	External interrupt request 01 input pin	3	81	C2	3	3
	INT01_1		83	61	D9	-	-
	INT02_0	External interrupt request 02 input pin	4	82	B3	4	4
	INT02_1		53	31	J10	43	35
	INT03_0	External interrupt request 03 input pin	93	71	D6	73	-
	INT03_1		56	34	H9	46	38
	INT03_2		9	87	E1	9	5
	INT04_0	External interrupt request 04 input pin	12	90	E4	12	8
	INT04_1		59	37	G9	49	40
	INT04_2		10	88	E2	10	6
	INT05_0	External interrupt request 05 input pin	74	52	C10	60	-
	INT05_1		65	43	F9	55	-
	INT05_2		11	89	E3	11	7
	INT06_1	External interrupt request 06 input pin	73	51	C11	59	48
	INT06_2		45	23	K8	35	27
	INT07_2	External interrupt request 07 input pin	5	83	D1	5	-
	INT08_1	External interrupt request 08 input pin	14	92	F2	-	-
	INT08_2		8	86	D5	8	-
	INT09_1	External interrupt request 09 input pin	15	93	F3	-	-
	INT10_1	External interrupt request 10 input pin	16	94	G1	-	-
	INT11_1	External interrupt request 11 input pin	17	95	G2	-	-
	INT12_1	External interrupt request 12 input pin	27	5	J4	-	-
	INT13_1	External interrupt request 13 input pin	28	6	L5	-	-
	INT14_1	External interrupt request 14 input pin	39	17	K6	29	-
	INT15_1	External interrupt request 15 input pin	96	74	C4	76	60
	NMIX	Non-Maskable Interrupt input	92	70	B5	72	57

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
GPIO	P00	General-purpose I/O port 0	77	55	A9	61	49
	P01		78	56	B9	62	50
	P02		79	57	B11	63	51
	P03		80	58	A8	64	52
	P04		81	59	B8	65	53
	P05		82	60	C8	-	-
	P06		83	61	D9	-	-
	P07		84	62	A7	66	-
	P08		85	63	B7	-	-
	P09		86	64	C7	-	-
	P0A		87	65	D7	67	54
	P0B		88	66	A6	68	55
	P0C		89	67	B6	69	56
	P0D		90	68	C6	70	-
	P0E		91	69	A5	71	-
	P0F		92	70	B5	72	57
	P10	General-purpose I/O port 1	52	30	J11	42	34
	P11		53	31	J10	43	35
	P12		54	32	J8	44	36
	P13		55	33	H10	45	37
	P14		56	34	H9	46	38
	P15		57	35	H7	47	39
	P16		58	36	G10	48	-
	P17		59	37	G9	49	40
	P18		63	41	G8	53	44
	P19		64	42	F10	54	45
	P1A		65	43	F9	55	-
	P1B		66	44	E11	56	-
	P1C		67	45	E10	-	-
	P1D		68	46	F8	-	-
	P1E		69	47	E9	-	-
	P1F		70	48	D11	-	-
	P20	General-purpose I/O port 2	74	52	C10	60	-
	P21		73	51	C11	59	48
	P22		72	50	E8	58	47
	P23		71	49	D10	57	46

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin	73	51	C11	59	48
	SIN0_1		56	34	H9	46	-
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	72	50	E8	58	47
	SOT0_1 (SDA0_1)		57	35	H7	47	-
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin This pin operates as SCK0 when it is used in a CSIO (operation modes 2) and as SCL0 when it is used in an I^2C (operation mode 4).	71	49	D10	57	46
	SCK0_1 (SCL0_1)		58	36	G10	48	-
Multi Function Serial 1	SIN1_1	Multifunction serial interface ch.1 input pin	53	31	J10	43	35
	SOT1_1 (SDA1_1)	Multifunction serial interface ch.1 output pin This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	54	32	J8	44	36
	SCK1_1 (SCL1_1)	Multifunction serial interface ch.1 clock I/O pin This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I^2C (operation mode 4).	55	33	H10	45	37
Multi Function Serial 2	SIN2_2	Multifunction serial interface ch.2 input pin	59	37	G9	49	40
	SOT2_2 (SDA2_2)	Multifunction serial interface ch.2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	63	41	G8	53	44
	SCK2_2 (SCL2_2)	Multifunction serial interface ch.2 clock I/O pin This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	64	42	F10	54	45
Multi Function Serial 3	SIN3_1	Multifunction serial interface ch.3 input pin	2	80	C1	2	2
	SIN3_2		39	17	K6	29	-
	SOT3_1 (SDA3_1)	Multifunction serial interface ch.3 output pin This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	3	81	C2	3	3
	SOT3_2 (SDA3_2)		40	18	J6	30	-
	SCK3_1 (SCL3_1)	Multifunction serial interface ch.3 clock I/O pin This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	82	B3	4	4
	SCK3_2 (SCL3_2)		41	19	L7	31	-

List of Pin Status

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enabled	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*[1]/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*[1]/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	Vcc	Vss - 0.5	Vss + 6.5	V	
Power supply voltage (for USB) *1, *3	USBVcc	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage*1, *4	AVcc	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage*1, *4	AVRH	Vss - 0.5	Vss + 6.5	V	
Input voltage*1	V_I	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	Except for USB pin
		Vss - 0.5	USBVcc + 0.5 (≤ 6.5V)	V	USB pin
		Vss - 0.5	Vss + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	Vss - 0.5	AVcc + 0.5 (≤ 6.5V)	V	
Output voltage*1	V_O	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
"L" level maximum output current*5	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80, P81
"L" level average output current*6	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			18.5	mA	P80, P81
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*5	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80, P81
"H" level average output current*6	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 20.5	mA	P80, P81
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that Vss = AVss = 0.0V.

*2: Vcc must not drop below Vss - 0.5V.

*3: USBVcc must not drop below Vss - 0.5V.

*4: Be careful not to exceed Vcc + 0.5 V, for example, when the power is turned on.

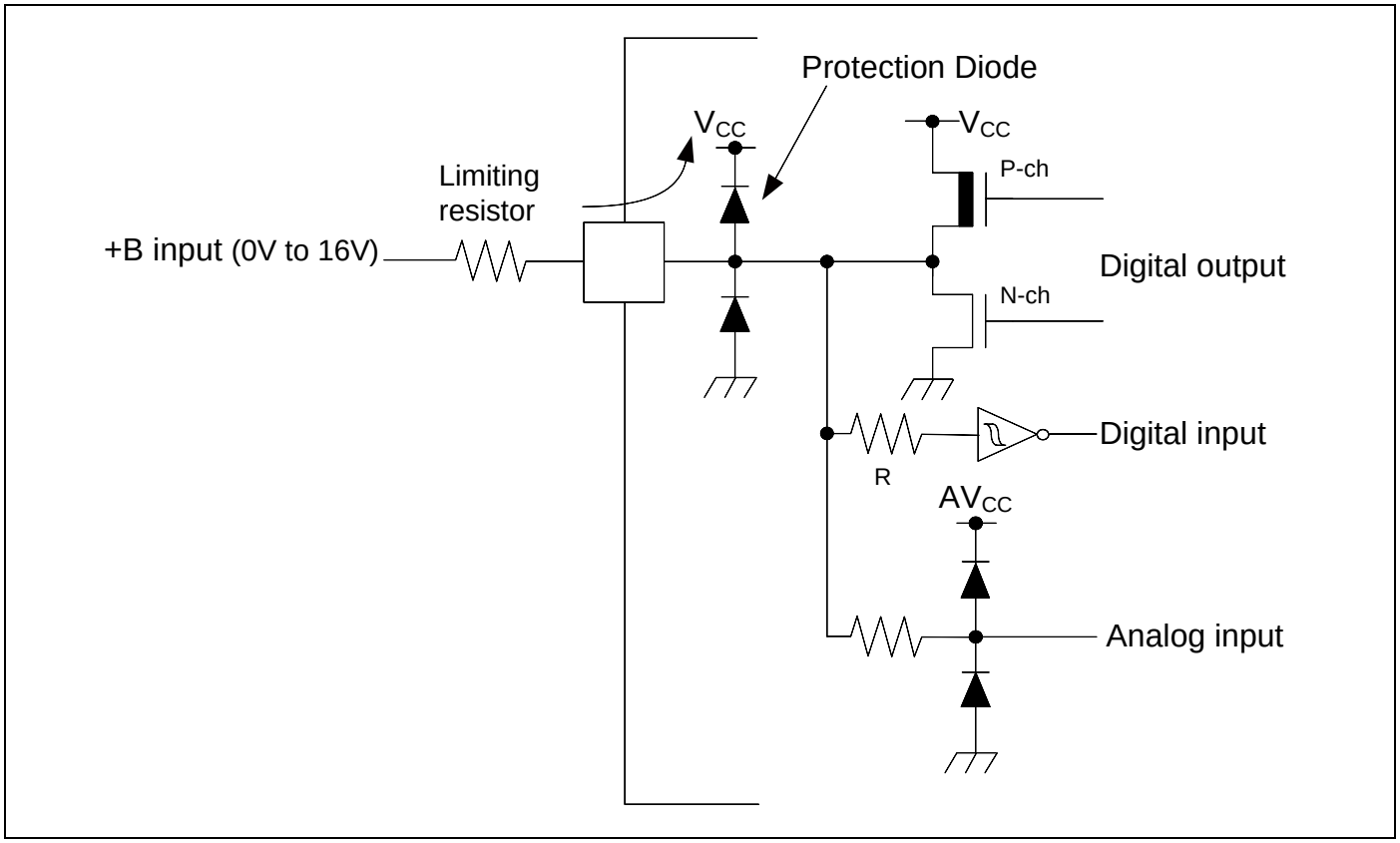
*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

*8:

- See “4. List of Pin Functions” and “5. I/O Circuit Type” about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Vcc = AVcc = 2.7V to 5.5V, USBVcc = 3.0V to 3.6V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	Ta = + 25°C, When LVD is off *3	2.5	3	mA	*1
				Ta = + 105°C, When LVD is off *3	-	6	mA	*1
			Sub TIMER mode	Ta = + 25°C, When LVD is off *4	60	230	µA	*1
				Ta = + 105°C, When LVD is off *4	-	3.1	mA	*1
STOP mode current	I_{CCH}		STOP mode	Ta = + 25°C, When LVD is off	35	200	µA	*1
				Ta = + 105°C, When LVD is off	-	3	mA	*1

*1: When all ports are fixed.

*2: V_{CC}=5.5V

*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt Vcc = 5.5V	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	11.4	13.1	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, Ta = - 40°C to + 105°C)

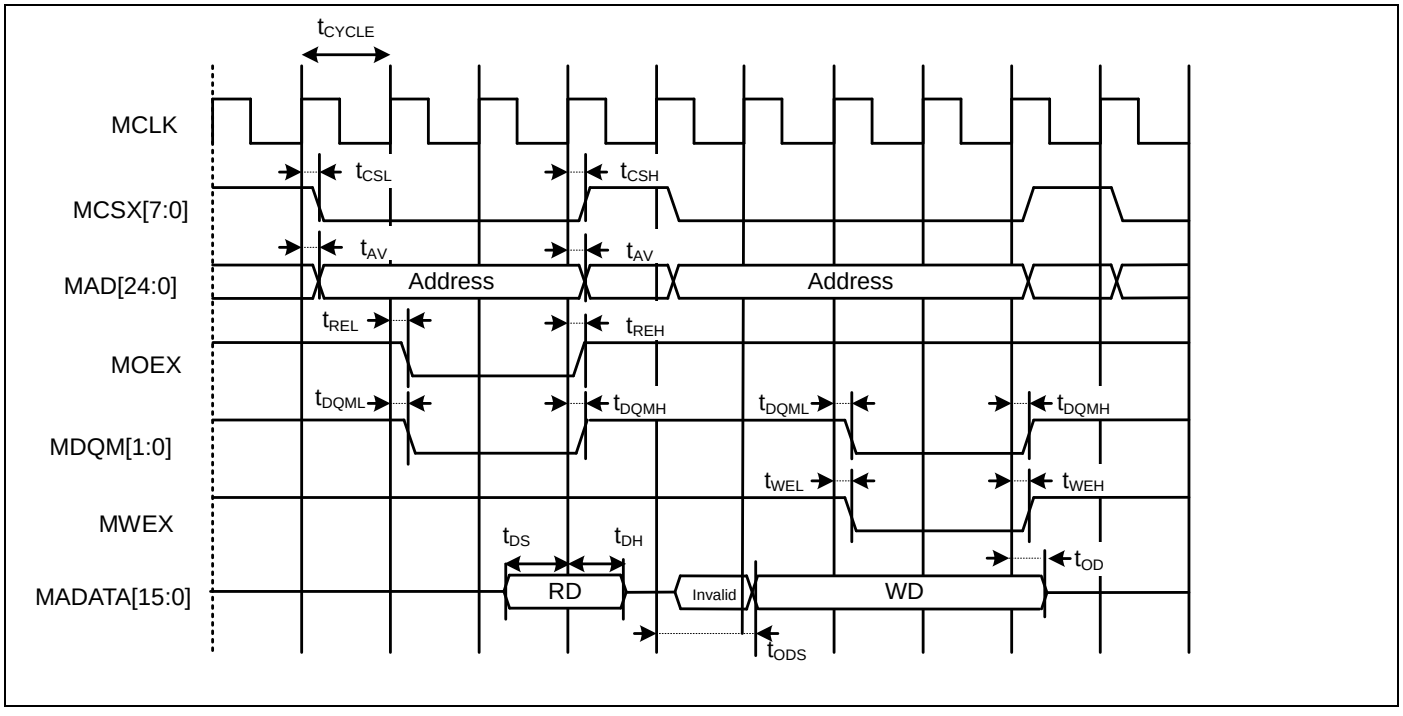
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.57	0.72	mA	
			At stop	0.06	20	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5V	1.1	1.96	mA	
			At stop	0.06	4	µA	

Separate Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK MAD[24:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MCSX delay time	t_{CSL}	MCLK MCSX[7:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{CSH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MOEX delay time	t_{REL}	MCLK MOEX	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{REH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	19	-	ns
			Vcc < 4.5V	37		
MCLK ↑→ Data hold time	t_{DH}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	0	-	ns
			Vcc < 4.5V			
MWEX delay time	t_{WEL}	MCLK MWEX	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{WEH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK MDQM[1:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{DQMH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	V_{CC} ≥ 4.5V	MCLK+1	MCLK+18	ns
			V_{CC} < 4.5V		MCLK+24	
MCLK ↑ → Data output time	t_{OD}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	1	18	ns
			Vcc < 4.5V	1	24	

Note: When the external load capacitance C_L = 30pF.

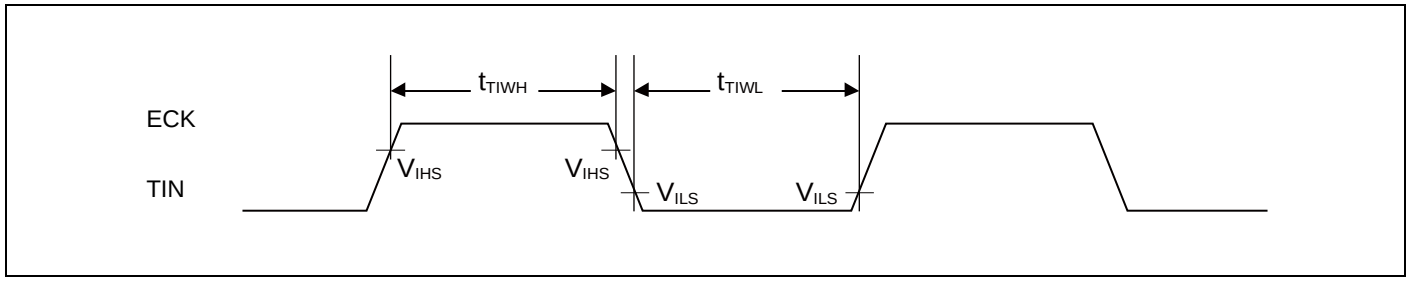


12.4.9 Base Timer Input Timing

Timer input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

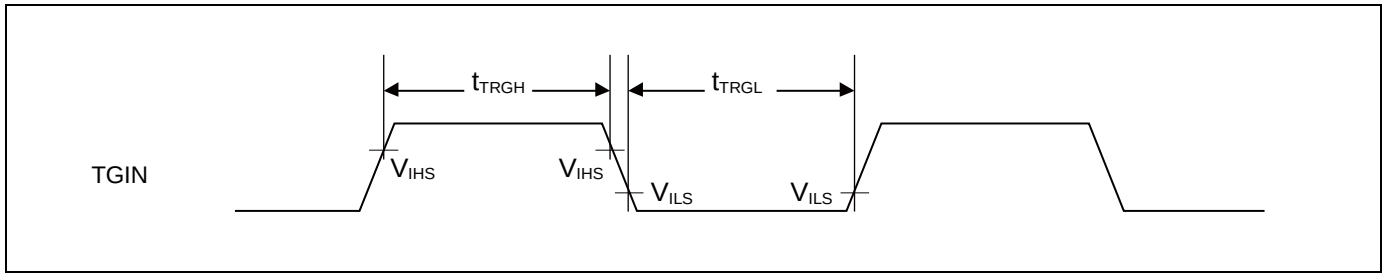
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK,TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the Base Timer is connected to, see “8. Block Diagram” in this datasheet.

CSIO (SPI = 0, SCINV = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see “Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.

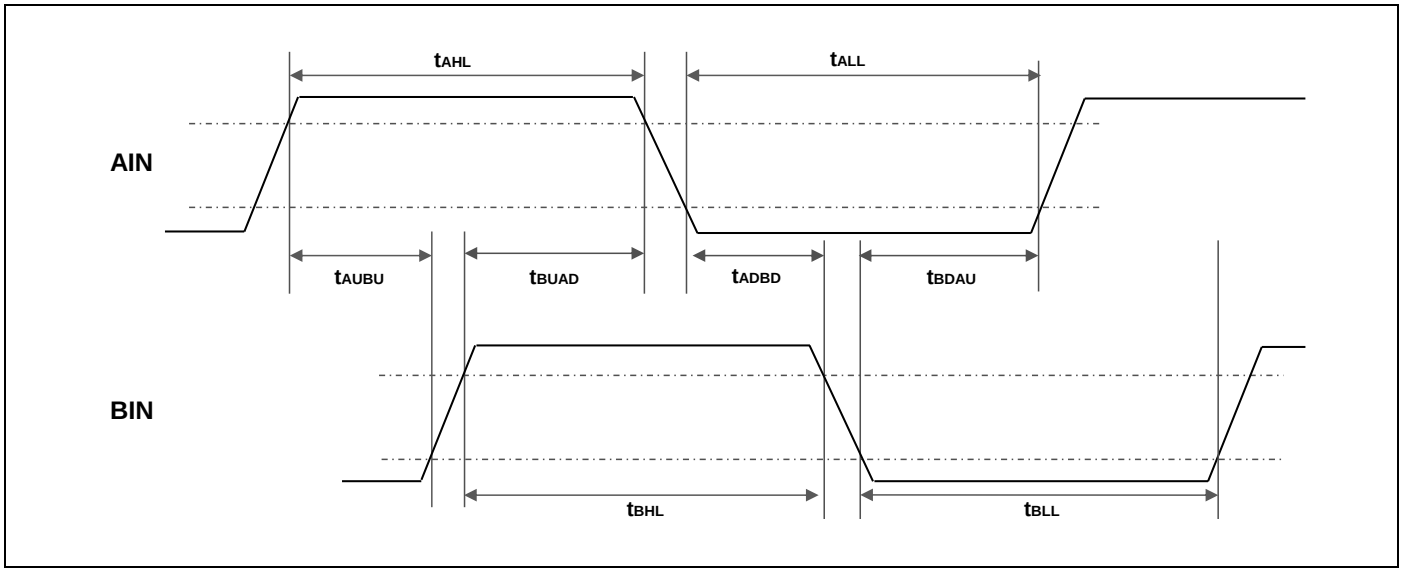
12.4.12 Quadrature Position/Revolution Counter timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$ *	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rise time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR:CGSC = "1"			

* : t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.



12.4.13 I^2C Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

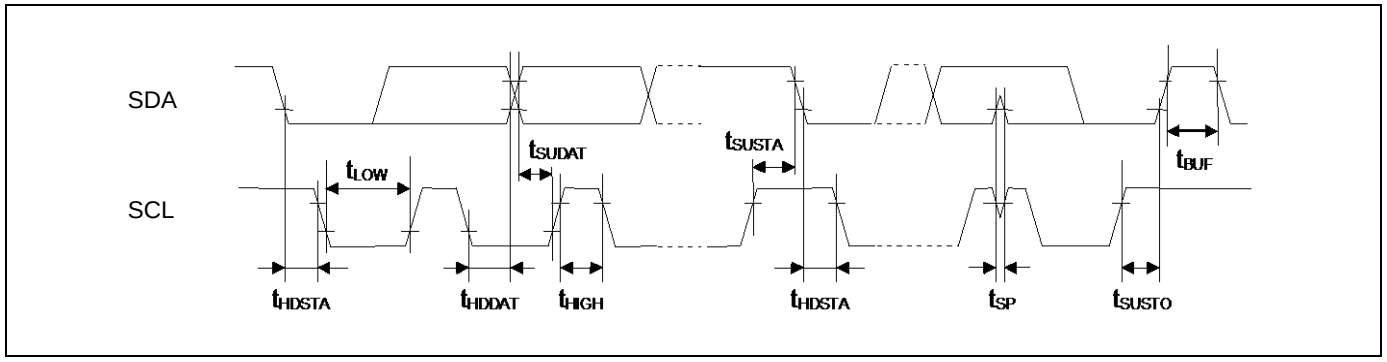
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓→ SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

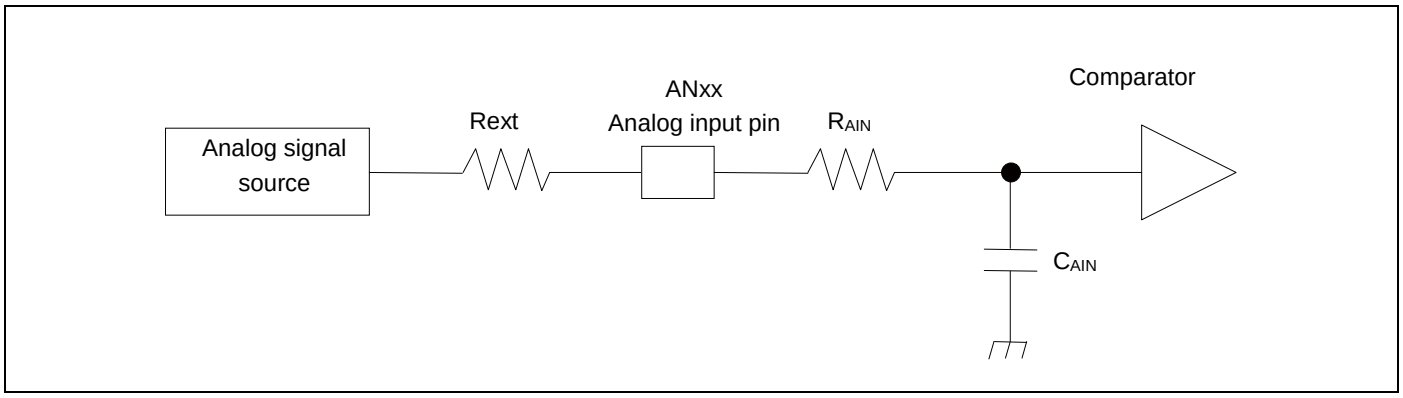
*1; R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: Fast-mode I^2C bus device can be used on Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I2C is connected to, see "8. Block Diagram" in this datasheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts : Sampling time

R_{AIN} : input resistor of A/D = 2kΩ $4.5 \leq AV_{CC} \leq 5.5$

input resistor of A/D = 3.8kΩ $2.7 \leq AV_{CC} < 4.5$

C_{AIN} : input capacity of A/D = 12.9pF $2.7 \leq AV_{CC} \leq 5.5$

Rext : Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time

Tcck : Compare clock cycle

12.7 Low-voltage Detection Characteristics

Low-voltage detection reset

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

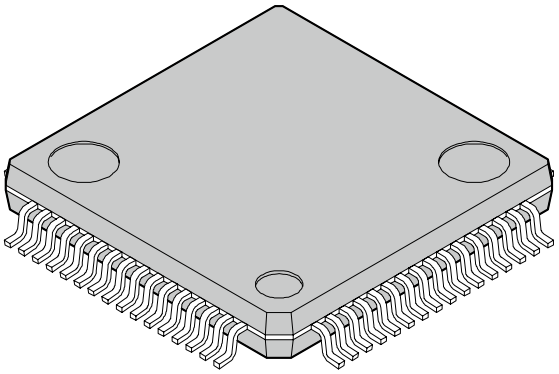
Interrupt of low-voltage detection

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	2240 × tcycp *	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

64-pin plastic LQFP

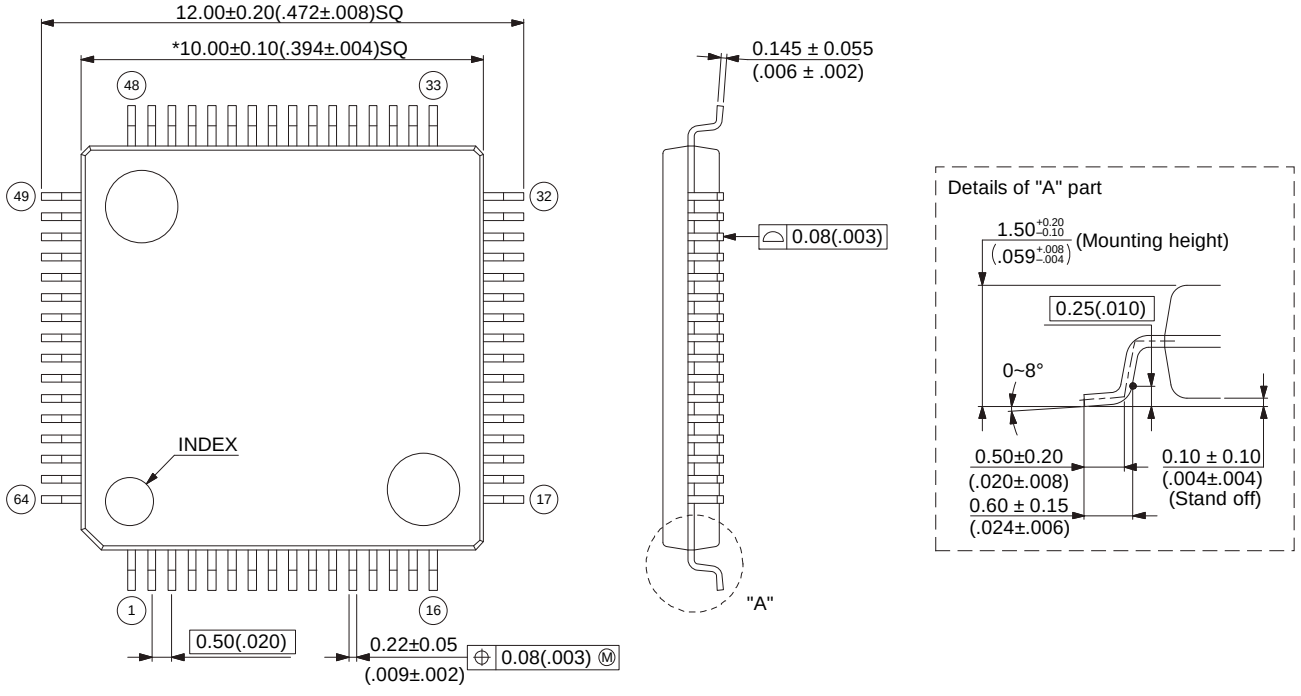


(FPT-64P-M38)

Lead pitch	0.50 mm
Package width × package length	10.00 mm × 10.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.