Infineon Technologies - MB9AF311LAPMC-G-JNE2 Datasheet

Welcome to E-XFL.COM

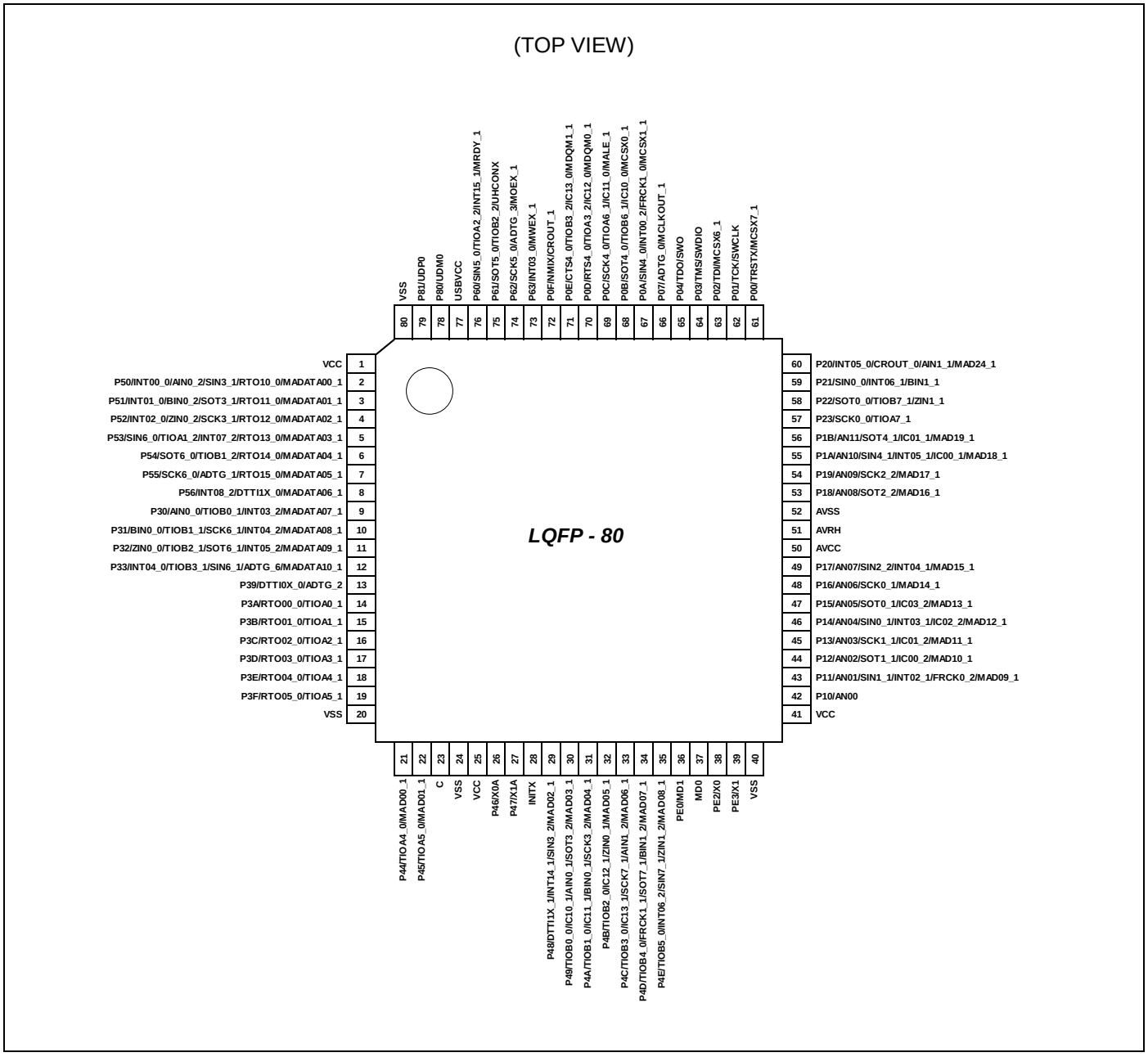
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af311lapmc-g-jne2

LCC-80P-M37



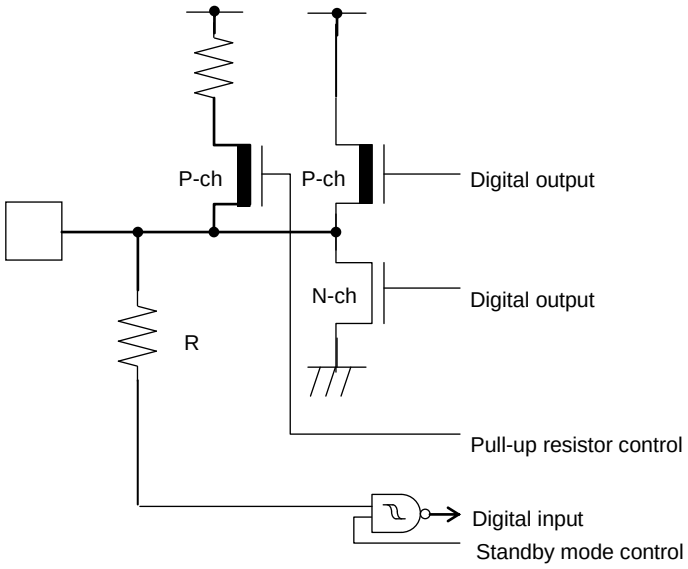
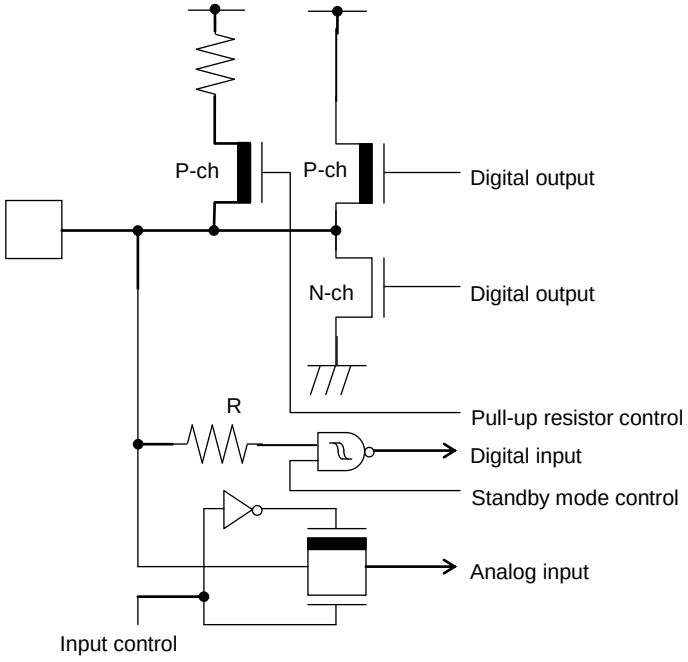
Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

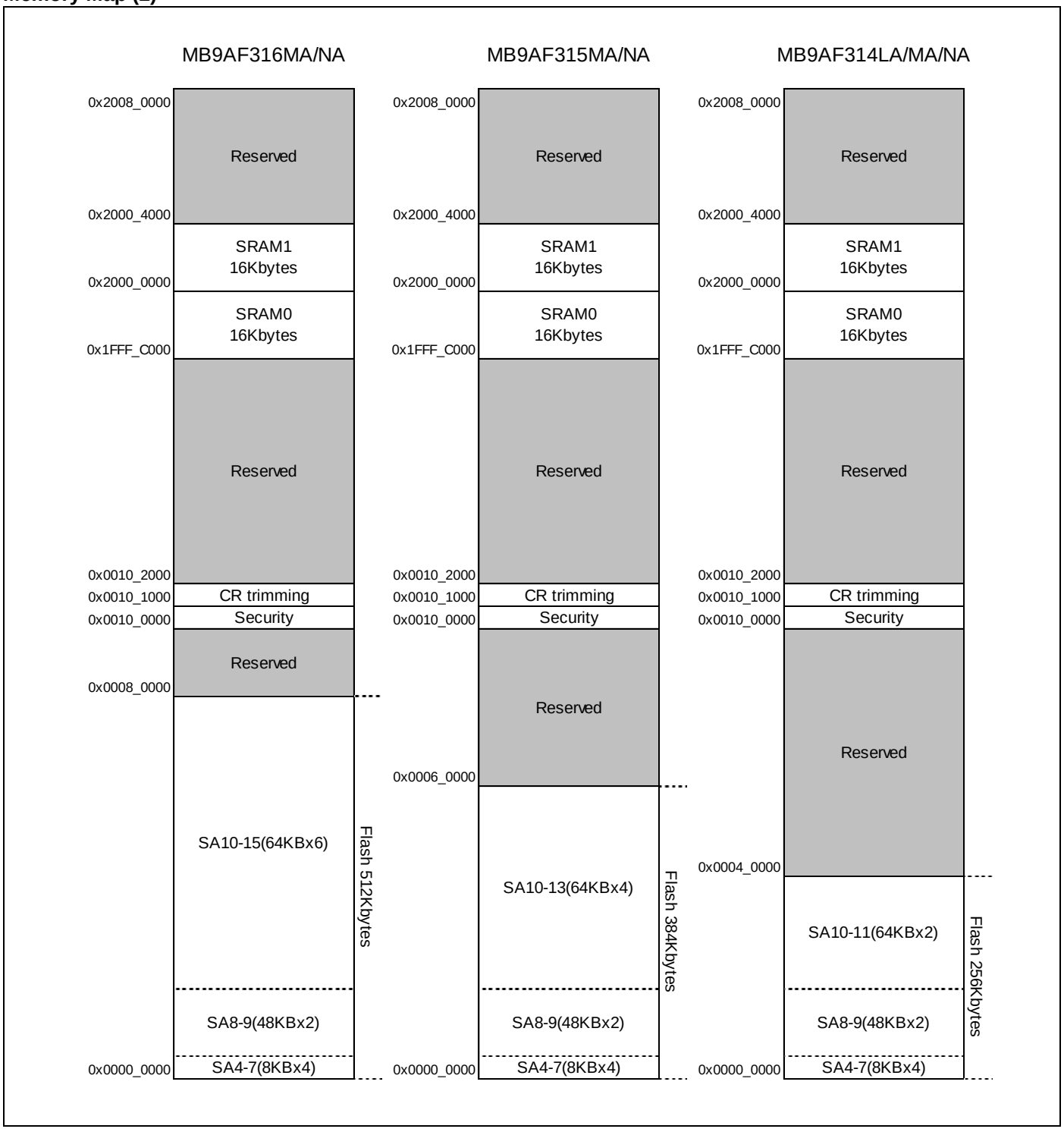
Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
83	61	D9	-	-	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 MCSX4_1	E	F
84	62	A7	66 -	-	P07 ADTG_0 MCLKOUT_1 TRACED2 SCK4_2 (SCL4_2)	E	G
85	63	B7	-	-	P08 TRACED3 TIOA0_2 CTS4_2 MCSX3_1	E	G
86	64	C7	-	-	P09 TRACECLK TIOB0_2 RTS4_2 MCSX2_1	E	G
87	65	D7	67	54 -	P0A SIN4_0 INT00_2 FRCK1_0 MCSX1_1	E / I*	H
88	66	A6	68	55 -	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MCSX0_1	E / I*	I
89	67	B6	69	56 -	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 MALE_1	E / I*	I
-	-	D4	-	-	VSS	-	
-	-	C3	-	-	VSS	-	

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	9	87	E1	9	5
	AIN0_1		40	18	J6	30	22
	AIN0_2		2	80	C1	2	2
	BIN0_0	QPRC ch.0 BIN input pin	10	88	E2	10	6
	BIN0_1		41	19	L7	31	23
	BIN0_2		3	81	C2	3	3
	ZIN0_0	QPRC ch.0 ZIN input pin	11	89	E3	11	7
	ZIN0_1		42	20	K7	32	24
	ZIN0_2		4	82	B3	4	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	74	52	C10	60	-
	AIN1_2		43	21	H6	33	25
	BIN1_1	QPRC ch.1 BIN input pin	73	51	C11	59	-
	BIN1_2		44	22	J7	34	26
	ZIN1_1	QPRC ch.1 ZIN input pin	72	50	E8	58	-
	ZIN1_2		45	23	K8	35	27
USB	UDM0	USB Function / HOST D – pin	98	76	A3	78	62
	UDP0	USB Function / HOST D + pin	99	77	A2	79	63
	UHCONX	USB external pull-up control pin	95	73	B4	75	59

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Memory Map (2)



*: See "MB9A310/110 Series Flash programming Manual" for sector structure of Flash.

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

(Vcc = AVcc = 2.7V to 5.5V, USBVcc = 3.0V to 3.6V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	Ta = + 25°C, When LVD is off *3	2.5	3	mA	*1
				Ta = + 105°C, When LVD is off *3	-	6	mA	*1
			Sub TIMER mode	Ta = + 25°C, When LVD is off *4	60	230	µA	*1
				Ta = + 105°C, When LVD is off *4	-	3.1	mA	*1
STOP mode current	I_{CCH}		STOP mode	Ta = + 25°C, When LVD is off	35	200	µA	*1
				Ta = + 105°C, When LVD is off	-	3	mA	*1

*1: When all ports are fixed.

*2: V_{CC}=5.5V

*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt Vcc = 5.5V	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	11.4	13.1	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.57	0.72	mA	
			At stop	0.06	20	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5V	1.1	1.96	mA	
			At stop	0.06	4	µA	

12.3.2 Pin Characteristics

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

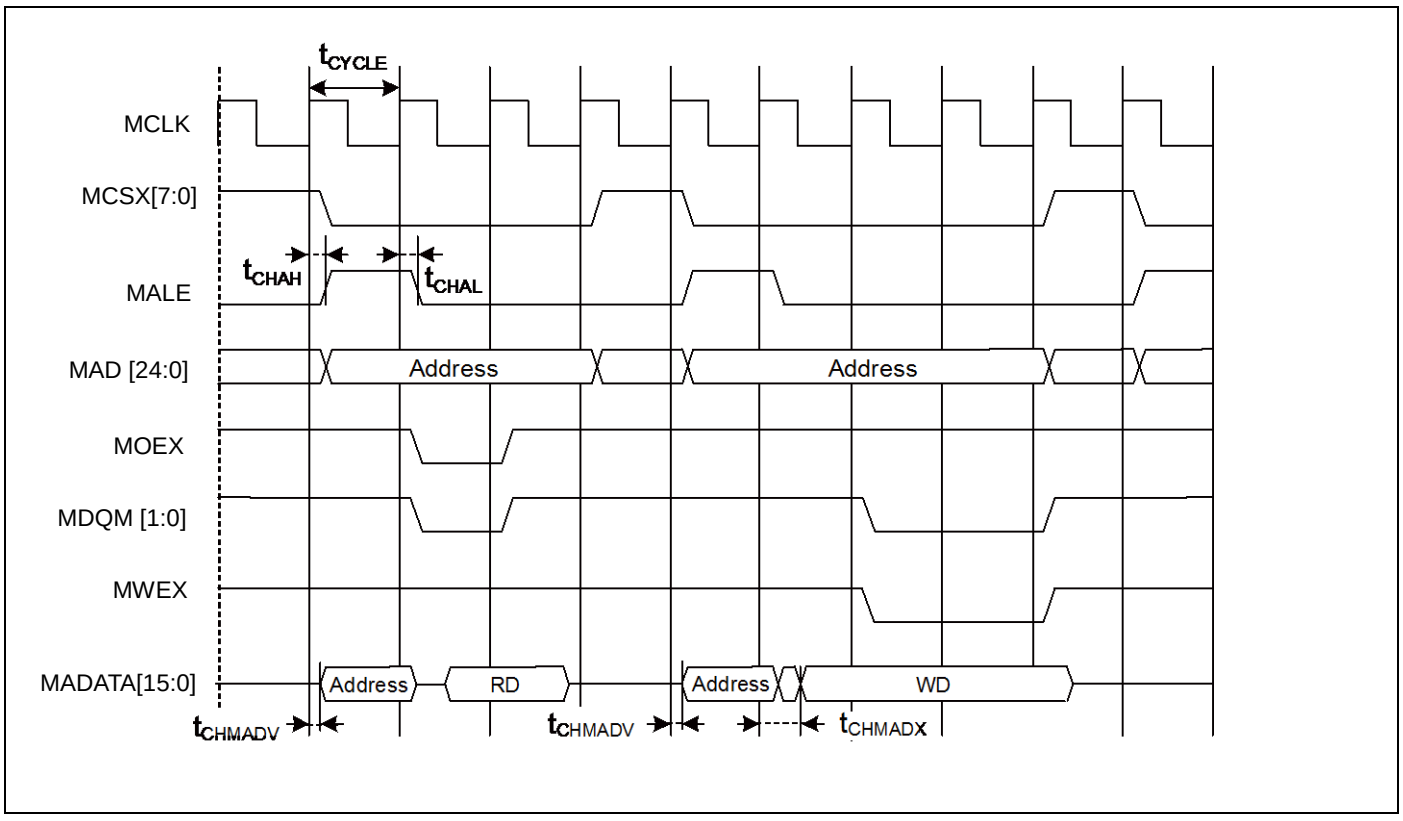
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	Vcc × 0.8	-	Vcc + 0.3	V	
		5V tolerant I/O pin	-	Vcc × 0.8	-	Vss + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	Vss - 0.3	-	Vcc × 0.2	V	
"H" level output voltage	V_{OH}	4mA type	Vcc ≥ 4.5 V I_{OH} = - 4mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 2mA					
		12mA type	Vcc ≥ 4.5 V I_{OH} = - 12mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 8mA					
		P80, P81	Vcc ≥ 4.5 V I_{OH} = - 20.5mA	Vcc - 0.4	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 13.0mA					
"L" level output voltage	V_{OL}	4mA type	Vcc ≥ 4.5 V I_{OL} = 4mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 2mA					
		12mA type	Vcc ≥ 4.5 V I_{OL} = 12mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 8mA					
		P80, P81	Vcc ≥ 4.5 V I_{OL} = 18.5mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 10.5mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	Vcc ≥ 4.5 V	25	50	100	kΩ	
			Vcc < 4.5 V	30	80	200		
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

Multiplexed Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK ALE	Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
	t_{CHAH}		Vcc ≥ 4.5V	1	9	ns	
			Vcc < 4.5V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		Vcc ≥ 4.5V	1	t_{OD}	ns	
			Vcc < 4.5V				

Note: When the external load capacitance C_L = 30pF.

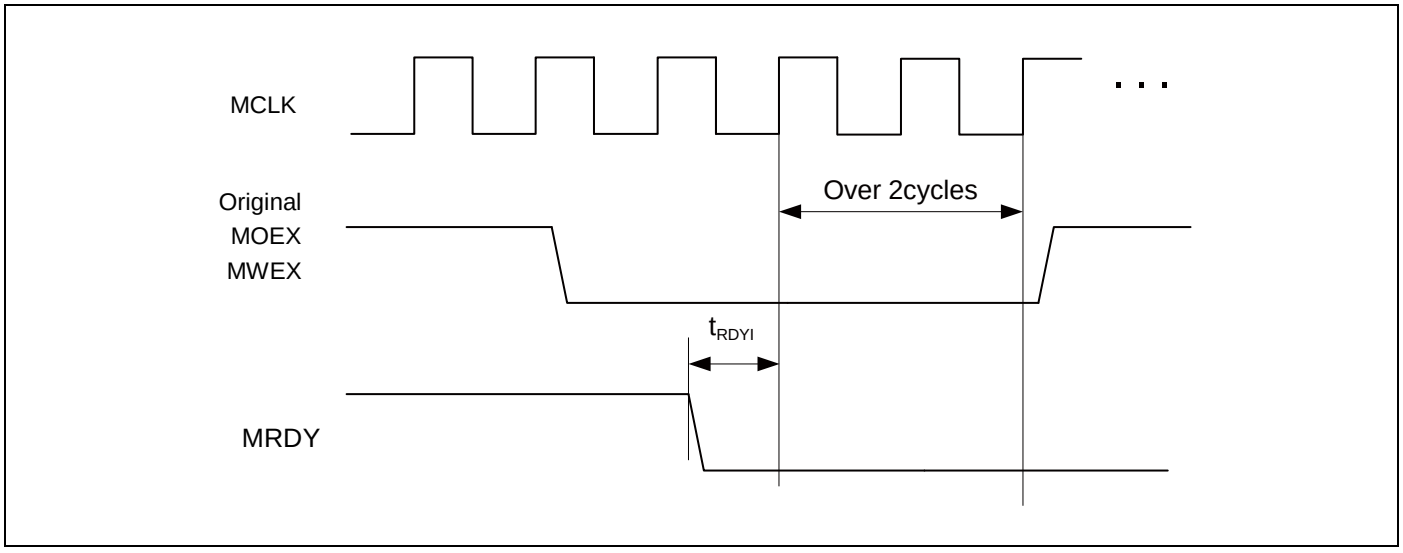


External Ready Input Timing

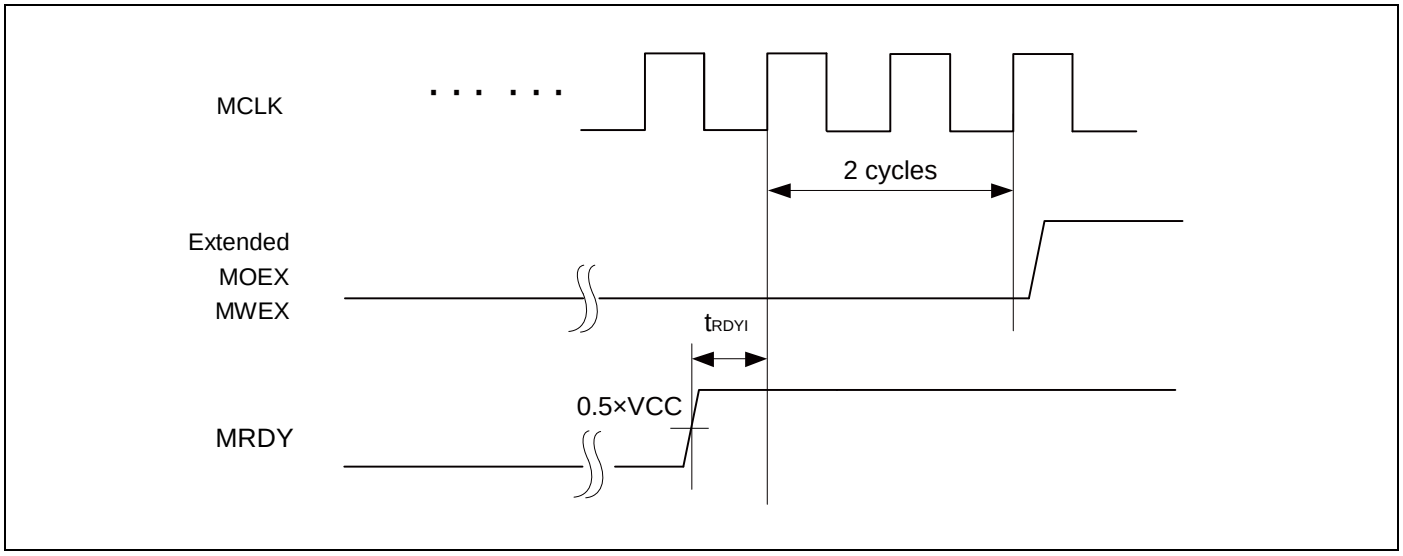
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK MRDY	Vcc ≥ 4.5V	19	-	ns	
			Vcc < 4.5V	37			

When RDY is input



When RDY is released



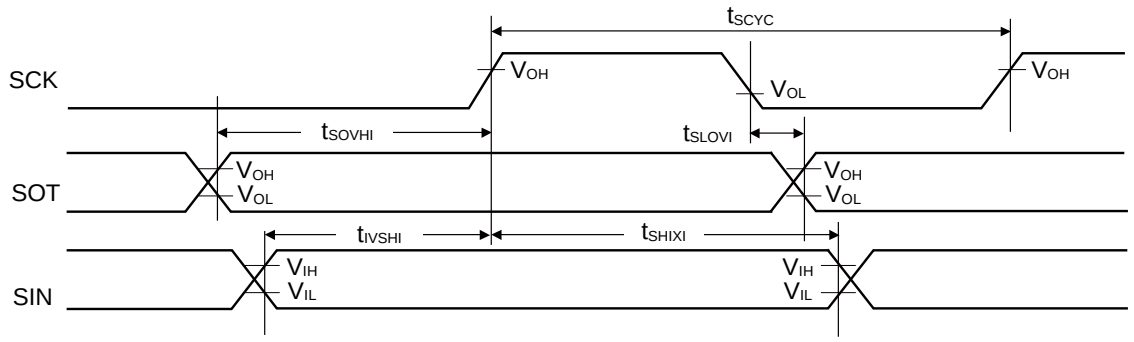
CSIO (SPI = 0, SCINV = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

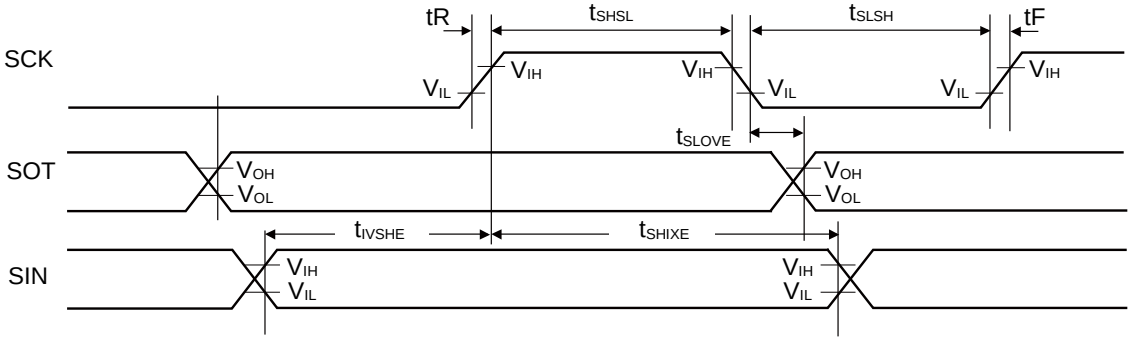
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see “Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



Master mode

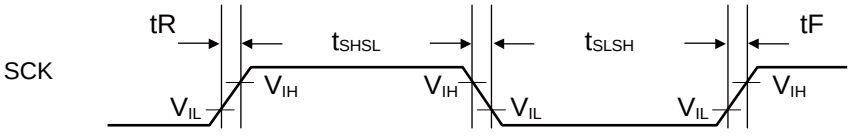


Slave mode

UART external clock input (EXT = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t_{SLSH}	C_L = 30pF	tcycp + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		tcycp + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



12.8 Flash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(Vcc = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	0.3	1.1		
Half word (16-bit) write time		12	384	µs	Not including system-level overhead time
Chip erase time	64K/128K/256KByte	5.2	23.6	s	Includes write time prior to internal erase
	384K/512KByte	8	38.4	s	

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.8.2 Erase/Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: At average + 85°C

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

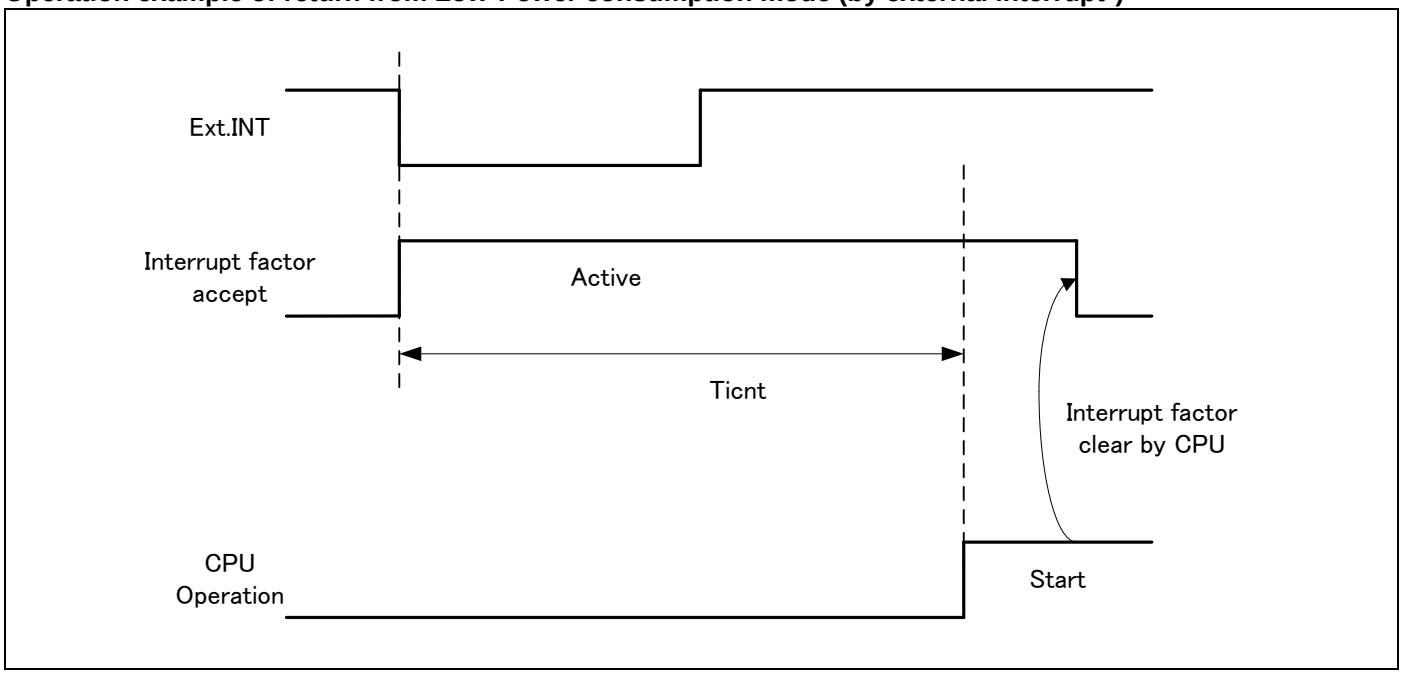
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		40	80	µs	
Low-speed CR TIMER mode		453	737	µs	
Sub TIMER mode		453	737	µs	
STOP mode		453	737	µs	

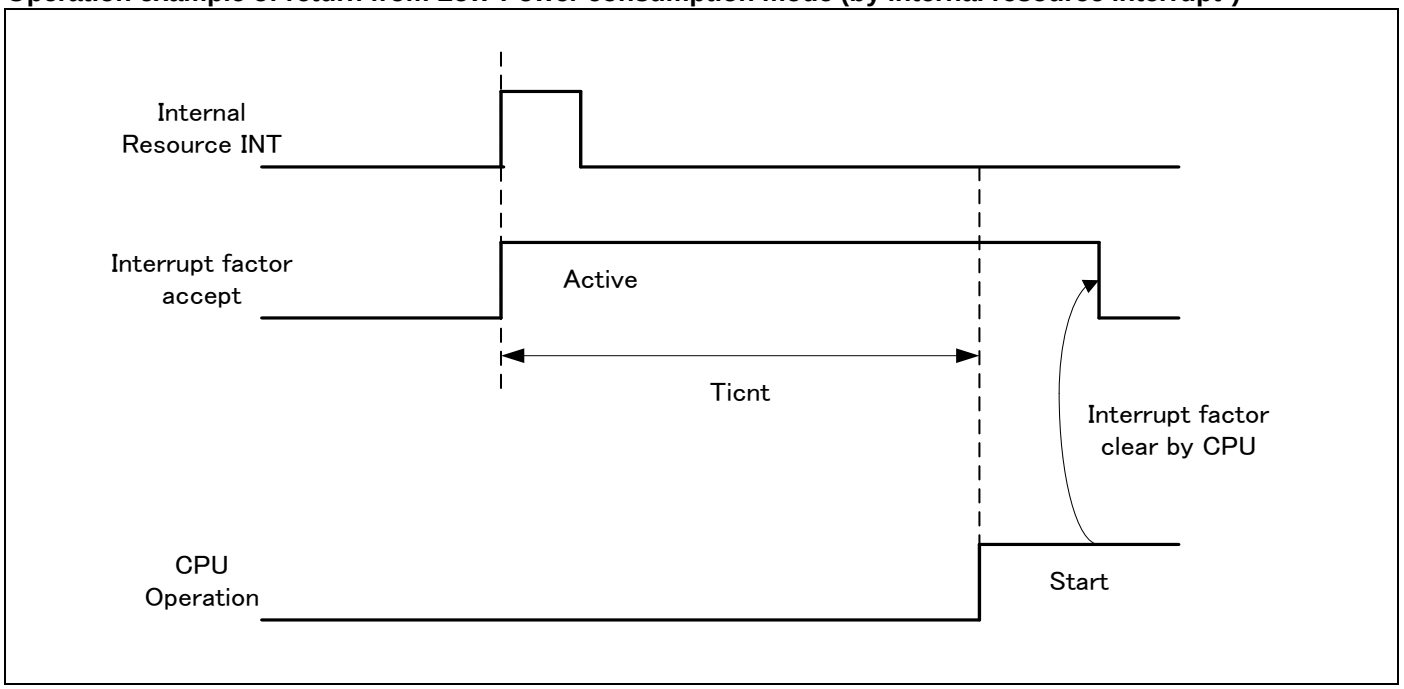
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual about the return factor from Low-Power consumption mode.
- When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF311LAPMC1-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),64-pin (FPT-64P-M38)	Tray
MB9AF312LAPMC1-G-JNE2	128Kbyte	16Kbyte		
MB9AF314LAPMC1-G-JNE2	256Kbyte	32Kbyte		
MB9AF311LAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.65mm pitch),64-pin (FPT-64P-M39)	
MB9AF312LAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314LAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF311LAQN-G-AVE2	64Kbyte	16Kbyte	Plastic □ QFN (0.5mm pitch),64-pin (LCC-64P-M24)	
MB9AF312LAQN-G-AVE2	128Kbyte	16Kbyte		
MB9AF314LAQN-G-AVE2	256Kbyte	32Kbyte		
MB9AF311MAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),80-pin (FPT-80P-M37)	
MB9AF312MAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314MAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF315MAPMC-G-JNE2	384Kbyte	32Kbyte		
MB9AF316MAPMC-G-JNE2	512Kbyte	32Kbyte		
MB9AF311NAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),100-pin (FPT-100P-M23)	
MB9AF312NAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314NAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF315NAPMC-G-JNE2	384Kbyte	32Kbyte		
MB9AF316NAPMC-G-JNE2	512Kbyte	32Kbyte		
MB9AF311NAPF-G-JNE1	64Kbyte	16Kbyte	Plastic □ QFP (0.65mm pitch), 100-pin (FPT-100P-M06)	
MB9AF312NAPF-G-JNE1	128Kbyte	16Kbyte		
MB9AF314NAPF-G-JNE1	256Kbyte	32Kbyte		
MB9AF315NAPF-G-JNE1	384Kbyte	32Kbyte		
MB9AF316NAPF-G-JNE1	512Kbyte	32Kbyte		
MB9AF311NABGL-GE1	64Kbyte	16Kbyte	Plastic □ PFBGA (0.8mm pitch),112-pin (BGA-112P-M04)	
MB9AF312NABGL-GE1	128Kbyte	16Kbyte		
MB9AF314NABGL-GE1	256Kbyte	32Kbyte		

15. Major Changes

Spansion Publication Number: MB9A310A-DS706-00012

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
-	-	Revised series name and part number: MB9A310 Series → MB9A310A Series MB9AF311L → MB9AF311LA MB9AF312L → MB9AF312LA MB9AF314L → MB9AF314LA MB9AF311M → MB9AF311MA MB9AF312M → MB9AF312MA MB9AF314M → MB9AF314MA MB9AF315M → MB9AF315MA MB9AF316M → MB9AF316MA MB9AF311N → MB9AF311NA MB9AF312N → MB9AF312NA MB9AF314N → MB9AF314NA MB9AF315N → MB9AF315NA MB9AF316N → MB9AF316NA Added the following package. LCC-64P-M24
7	PRODUCT LINEUP Function Multi-function Serial	Added the following description. ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO
	External Interrupts	Corrected the following description. 7pins (Max) → 8pins (Max)
34 to 37	SIGNAL DESCRIPTION Multi-function Serial (ch.0 to ch.7)	Corrected the description for function. Added "LIN pin" Deleted "UART pin"
42, 43	I/O CIRCUIT TYPE	Corrected the following schematic for "TypeB". CMOS level hysteresis input → Digital input Corrected the following schematic for "TypeC". Control Pin → Digital output
51	HANDLING DEVICE Power supply pins	Corrected the description.
54	MEMORY SIZE	Added "MEMORY SIZE".
69	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1)Main Clock input Characteristics	Added the items F_{CM} to the Internal operating clock frequency.
71	(4-2) Operating Conditions of Main PLL	Added the description.
72	(7) External Bus Timing External bus clock output Characteristics	
79	(8) Base Timer Input Timing Trigger input timing	Added the Note.
88	(10) External input timing	Corrected the footnote.
94	5. 12-bit A/D Converter (1) Electrical characteristics for the A/D converter	Corrected the value of "Full-scale transition voltage". Min: -20 → AVRH-20 Max: +20 → AVRH+20 Corrected the value of "Compare clock cycle". Max: 10000 → 2000 Corrected the value of "Reference voltage". Min: AVSS → 2.7
Revision 2.1		
-	-	Company name and layout design change
Revision 3.0		
2	FEATURES USB Interface	Added the description of PLL for USB

Document History

Document Title: MB9A310A Series 32-Bit ARM® Cortex®-M3, FM3 Microcontroller
Document Number: 002-04674

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	AKIH	12/16/2014	Migrated to Cypress and assigned document number 002-04674. No change to document contents or format.
*A	5198894	AKIH	04/06/2016	Updated to Cypress format.