Infineon Technologies - MB9AF312LAPMC-G-JNE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af312lapmc-g-jne2

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4MHz to 48MHz
- Sub Clock : 32.768kHz
- Built-in high-speed CR Clock : 4MHz
- Built-in low-speed CR Clock : 100kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pins
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three Low-Power Consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug

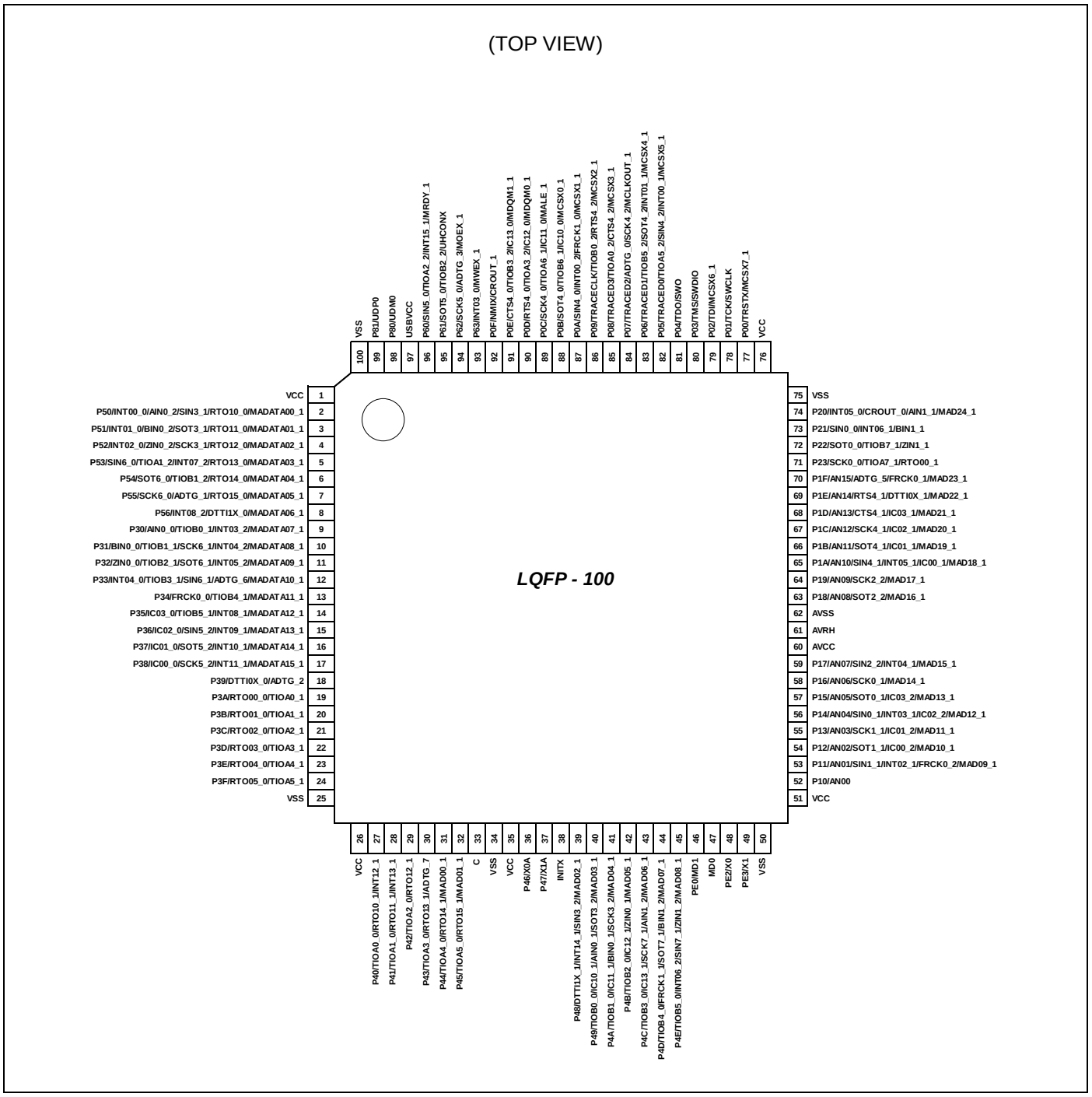
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM).*
  *: MB9AF311LA/MA, F312LA/MA, F314LA/MA, F315MA and F316MA support only SWJ-DP.

Power Supply

- Two Power Supplies
- VCC = 2.7V to 5.5V: Correspond to the wide range voltage.
- USBVCC = 3.0V to 3.6V: for USB I/O power supply, when USB is used.
  = 2.7V to 5.5V: when GPIO is used.

3. Pin Assignment

FPT-100P-M23



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
23	1	H3	18	14	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	2	J2	19	15	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	3	L1	20	16	VSS	-	
26	4	J1	-	-	VCC	-	
27	5	J4	-	-	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	H
28	6	L5	-	-	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	H
29	7	K5	-	-	P42 TIOA2_0 RTO12_1 (PPG12_1)	G	I
30	8	J5	-	-	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7	G	I
31	9	H5	21 -	-	P44 TIOA4_0 MAD00_1 RTO14_1 (PPG14_1)	G	I
32	10	L6	22 -	-	P45 TIOA5_0 MAD01_1 RTO15_1 (PPG14_1)	G	I
-	-	K2	-	-	VSS	-	
-	-	J3	-	-	VSS	-	
-	-	H4	-	-	VSS	-	

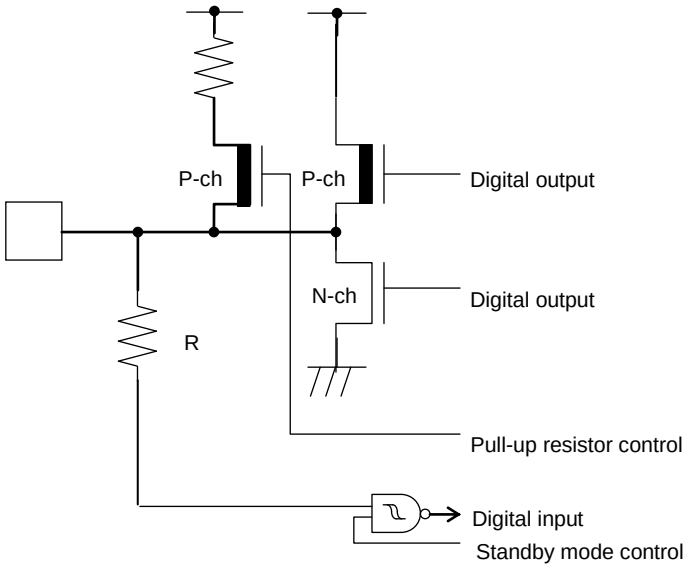
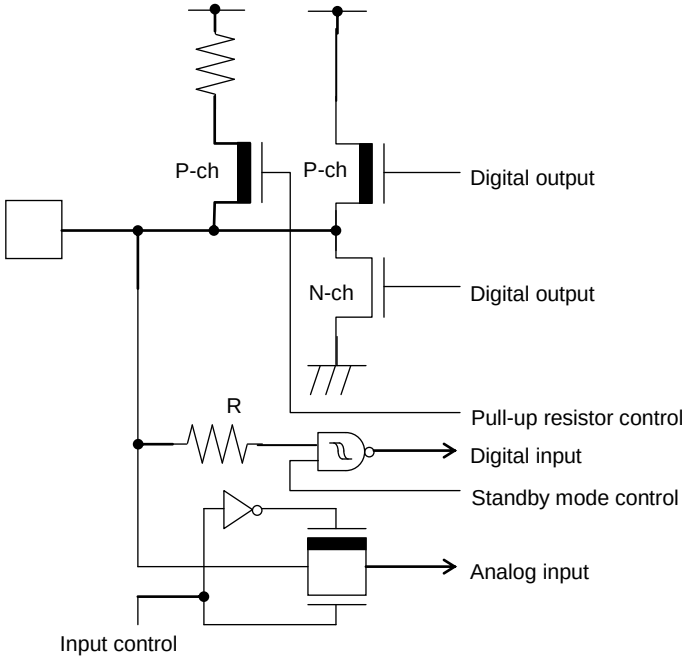
Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
65	43	F9	55	-	P1A AN10 SIN4_1 INT05_1 IC00_1 MAD18_1	F	L
66	44	E11	56	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_1	F	K
67	45	E10	-	-	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_1	F	K
68	46	F8	-	-	P1D AN13 CTS4_1 IC03_1 MAD21_1	F	K
69	47	E9	-	-	P1E AN14 RTS4_1 DTTI0X_1 MAD22_1	F	K
70	48	D11	-	-	P1F AN15 ADTG_5 FRCK0_1 MAD23_1	F	K
-	-	B10	-	-	VSS	-	
-	-	C9	-	-	VSS	-	

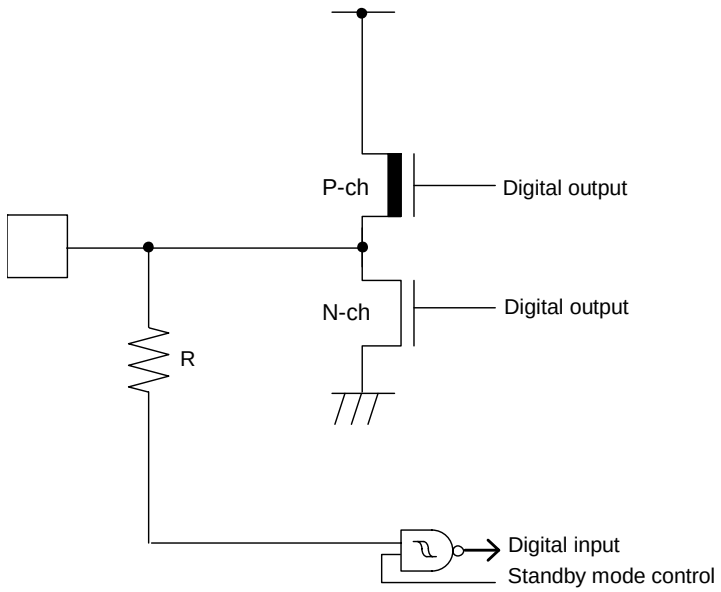
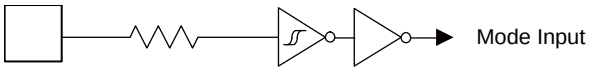
Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	87	65	D7	67	54
	SIN4_1		65	43	F9	55	-
	SIN4_2		82	60	C8	-	-
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	55
	SOT4_1 (SDA4_1)		66	44	E11	56	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	90	68	C6	70	-
	RTS4_1		69	47	E9	-	-
	RTS4_2		86	64	C7	-	-
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	91	69	A5	71	-
	CTS4_1		68	46	F8	-	-
	CTS4_2		85	63	B7	-	-
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	96	74	C4	76	60
	SIN5_2		15	93	F3	-	-
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin	5	83	D1	5	-
	SIN6_1		12	90	E4	12	8
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	84	D2	6	-
	SOT6_1 (SDA6_1)		11	89	E3	11	7
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	85	D3	7	-
	SCK6_1 (SCL6_1)		10	88	E2	10	6
Multi Function Serial 7	SIN7_1	Multifunction serial interface ch.7 input pin	45	23	K8	35	27
	SOT7_1 (SDA7_1)	Multifunction serial interface ch.7 output pin This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	44	22	J7	34	26
	SCK7_1 (SCL7_1)	Multifunction serial interface ch.7 clock I/O pin This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I^2C (operation mode 4).	43	21	H6	33	25

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Timer 1	DTTI1X_0	Input signal of wave form generator to control outputs RTO10 to RTO15 of multi-function timer 1	8	86	D5	8	-
	DTTI1X_1		39	17	K6	29	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	87	65	D7	67	-
	FRCK1_1		44	22	J7	34	-
	IC10_0	16-bit input capture input pin of multi-function timer 1 ICxx describes channel number.	88	66	A6	68	-
	IC10_1		40	18	J6	30	-
	IC11_0		89	67	B6	69	-
	IC11_1		41	19	L7	31	-
	IC12_0		90	68	C6	70	-
	IC12_1		42	20	K7	32	-
	IC13_0		91	69	A5	71	-
	IC13_1		43	21	H6	33	-
	RTO10_0 (PPG10_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG10 when it is used in PPG 1 output modes.	2	80	C1	2	-
	RTO10_1 (PPG10_1)		27	5	J4	-	-
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG10 when it is used in PPG 1 output modes.	3	81	C2	3	-
	RTO11_1 (PPG10_1)		28	6	L5	-	-
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG12 when it is used in PPG 1 output modes.	4	82	B3	4	-
	RTO12_1 (PPG12_1)		29	7	K5	-	-
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG12 when it is used in PPG 1 output modes.	5	83	D1	5	-
	RTO13_1 (PPG12_1)		30	8	J5	-	-
	RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG14 when it is used in PPG 1 output modes.	6	84	D2	6	-
	RTO14_1 (PPG14_1)		31	9	H5	21	-
	RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1 This pin operates as PPG14 when it is used in PPG 1 output modes.	7	85	D3	7	-
	RTO15_1 (PPG14_1)		32	10	L6	22	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	9	87	E1	9	5
	AIN0_1		40	18	J6	30	22
	AIN0_2		2	80	C1	2	2
	BIN0_0	QPRC ch.0 BIN input pin	10	88	E2	10	6
	BIN0_1		41	19	L7	31	23
	BIN0_2		3	81	C2	3	3
	ZIN0_0	QPRC ch.0 ZIN input pin	11	89	E3	11	7
	ZIN0_1		42	20	K7	32	24
	ZIN0_2		4	82	B3	4	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	74	52	C10	60	-
	AIN1_2		43	21	H6	33	25
	BIN1_1	QPRC ch.1 BIN input pin	73	51	C11	59	-
	BIN1_2		44	22	J7	34	26
	ZIN1_1	QPRC ch.1 ZIN input pin	72	50	E8	58	-
	ZIN1_2		45	23	K8	35	27
USB	UDM0	USB Function / HOST D – pin	98	76	A3	78	62
	UDP0	USB Function / HOST D + pin	99	77	A2	79	63
	UHCONX	USB external pull-up control pin	95	73	B4	75	59

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

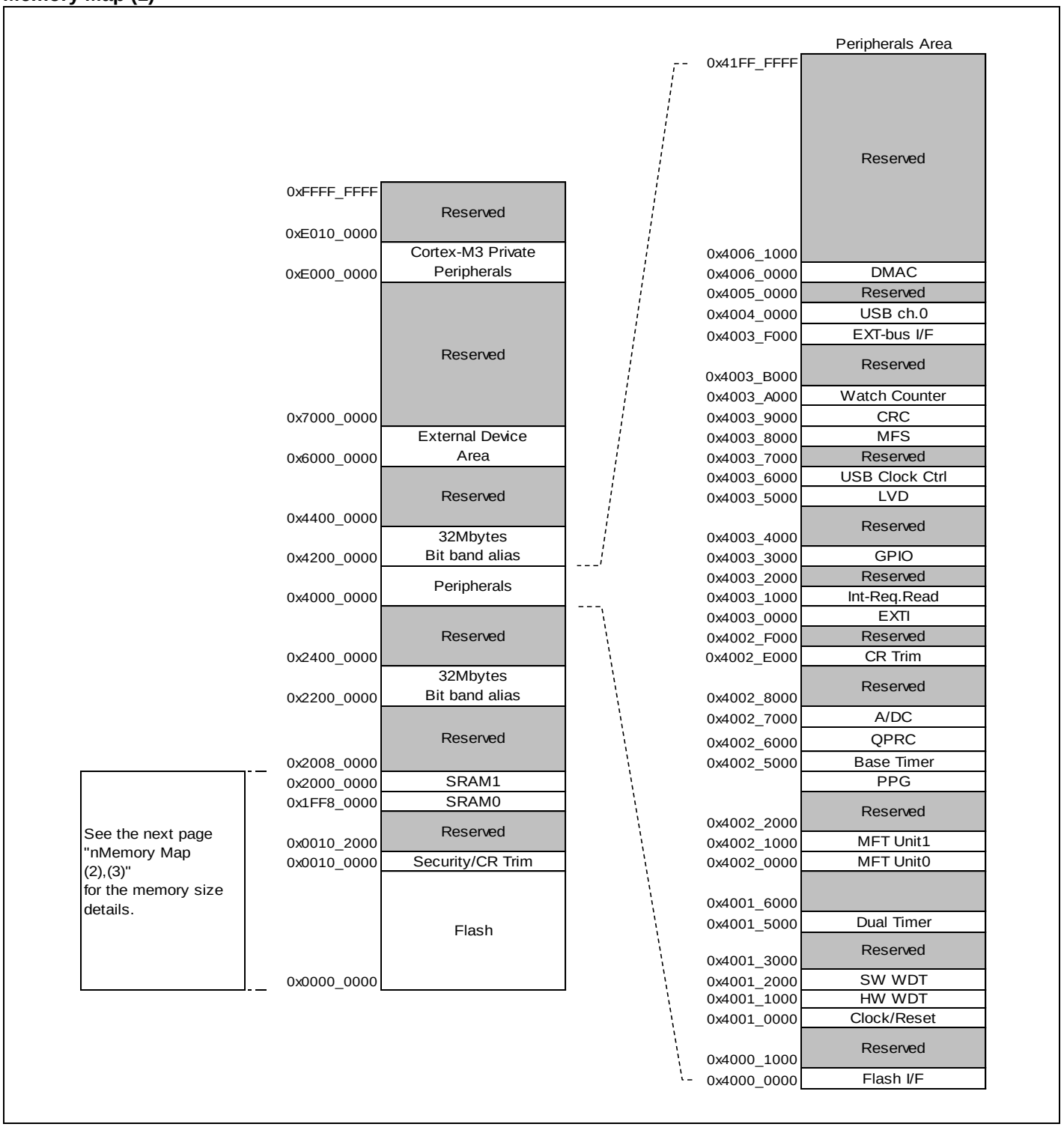
1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

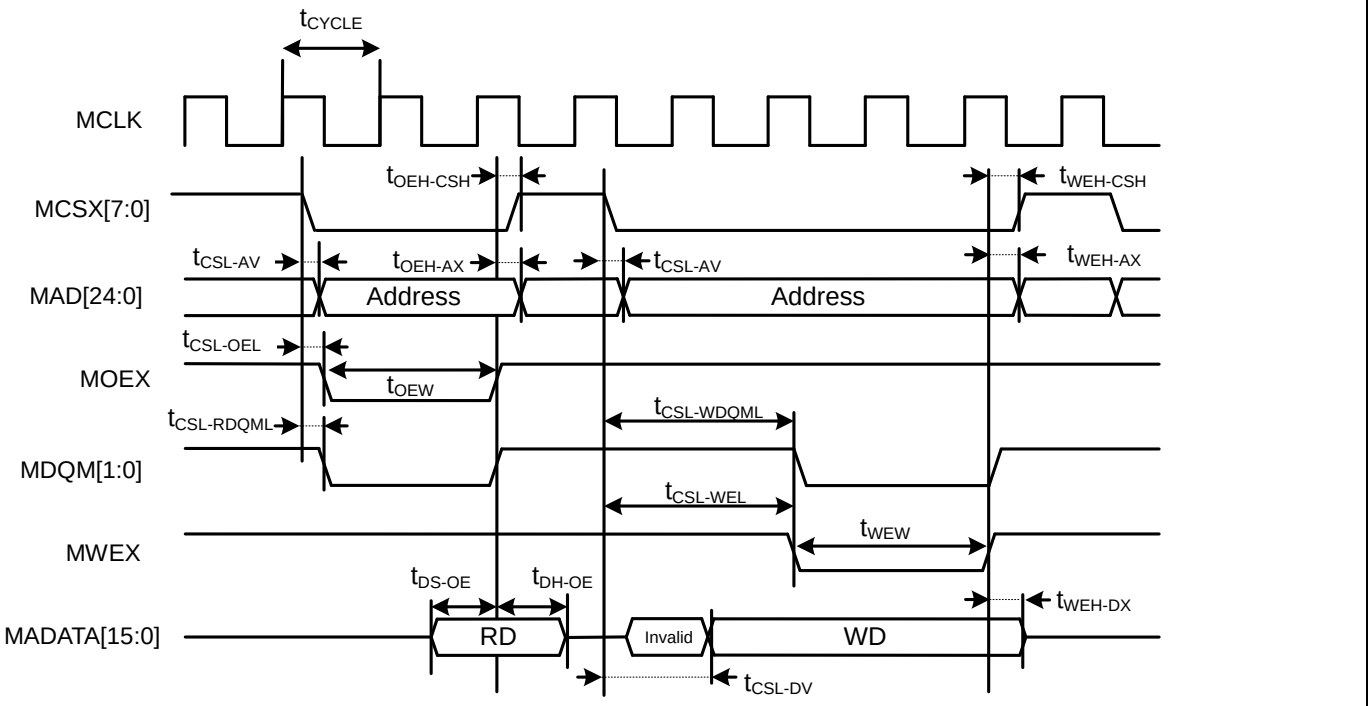
9. Memory Size

See “Memory size” in “1. Product Lineup” to confirm the memory size.

10. Memory Map

Memory Map (1)



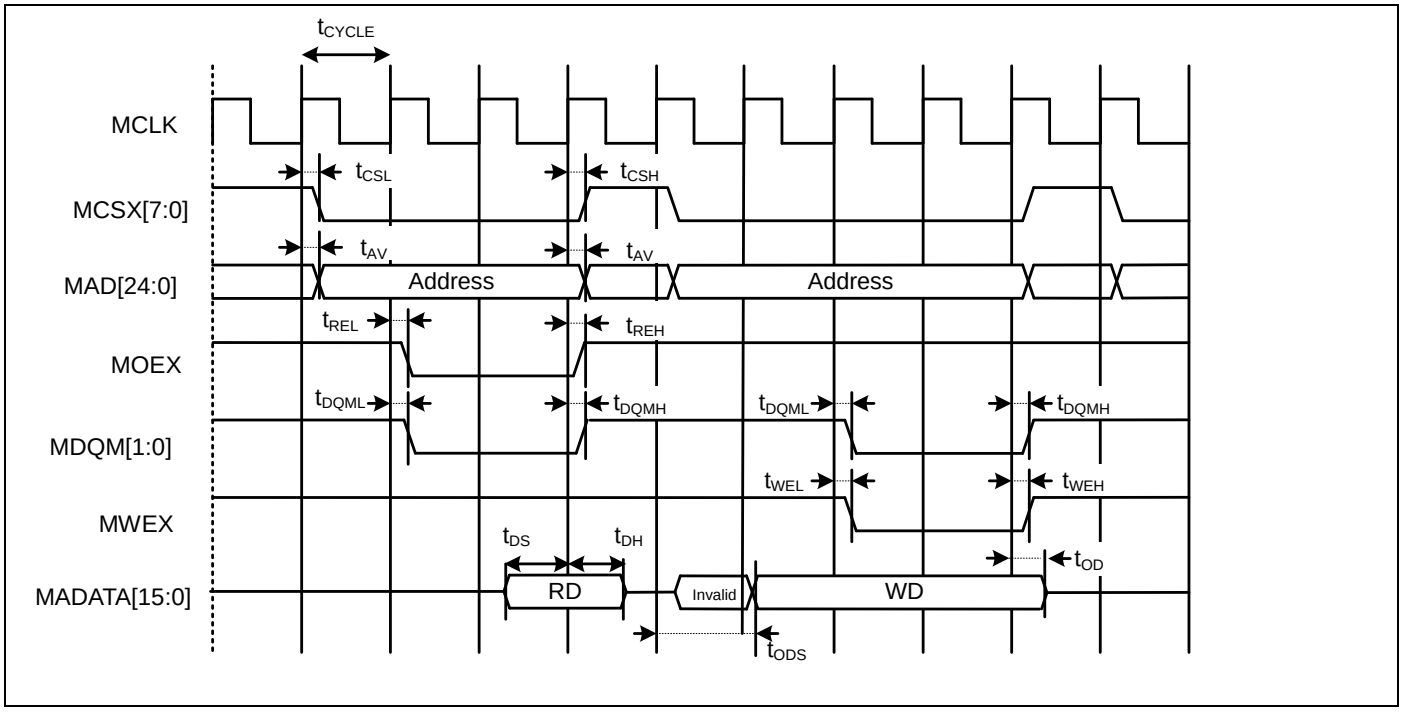

tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

Separate Bus Access Synchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK MAD[24:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MCSX delay time	t_{CSL}	MCLK MCSX[7:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{CSH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MOEX delay time	t_{REL}	MCLK MOEX	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{REH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	19	-	ns
			Vcc < 4.5V	37		
MCLK ↑→ Data hold time	t_{DH}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	0	-	ns
			Vcc < 4.5V			
MWEX delay time	t_{WEL}	MCLK MWEX	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{WEH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK MDQM[1:0]	Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
	t_{DQMH}		Vcc ≥ 4.5V	1	9	ns
			Vcc < 4.5V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	V_{CC} ≥ 4.5V	MCLK+1	MCLK+18	ns
			V_{CC} < 4.5V		MCLK+24	
MCLK ↑ → Data output time	t_{OD}	MCLK MADATA[15:0]	Vcc ≥ 4.5V	1	18	ns
			Vcc < 4.5V	1	24	

Note: When the external load capacitance C_L = 30pF.

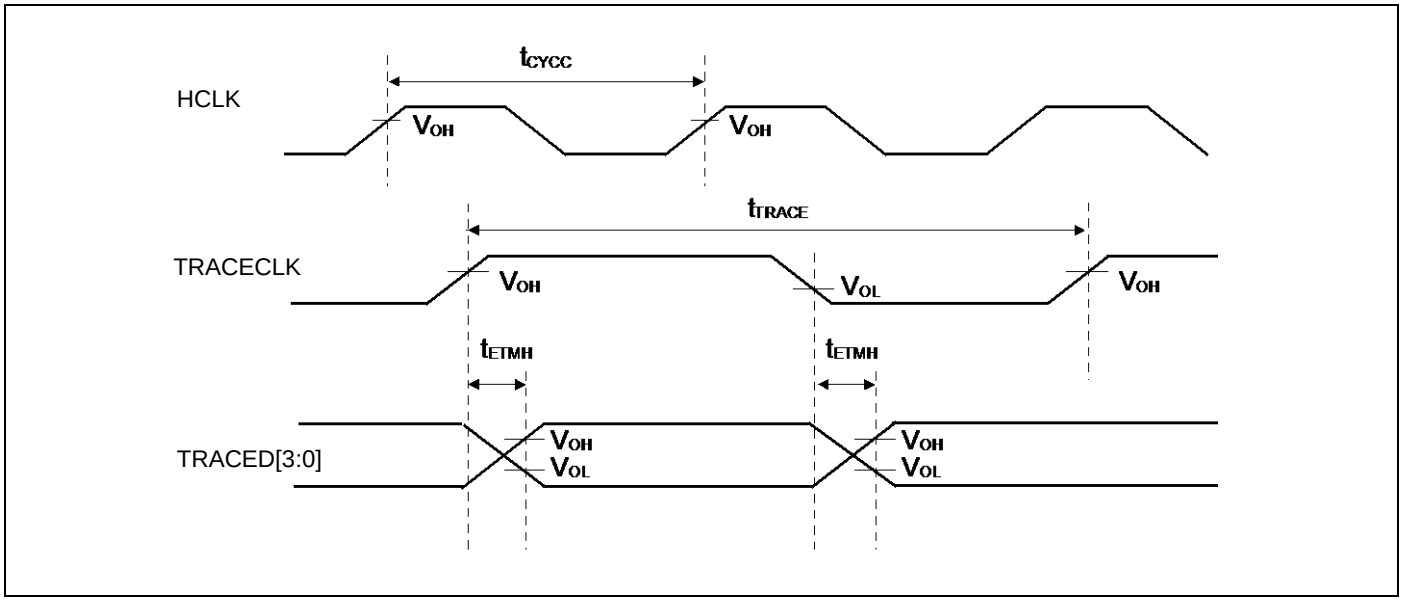


12.4.14 ETM timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED[3:0]	Vcc ≥ 4.5V	2	9	ns	
			Vcc < 4.5V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	Vcc ≥ 4.5V	-	40	MHz	
			Vcc < 4.5V	-	32	MHz	
TRACECLK Clock cycle time	t_{TRACE}		Vcc ≥ 4.5V	25	-	ns	
			Vcc < 4.5V	31.25	-	ns	

Note: When the external load capacitance C_L = 30pF.

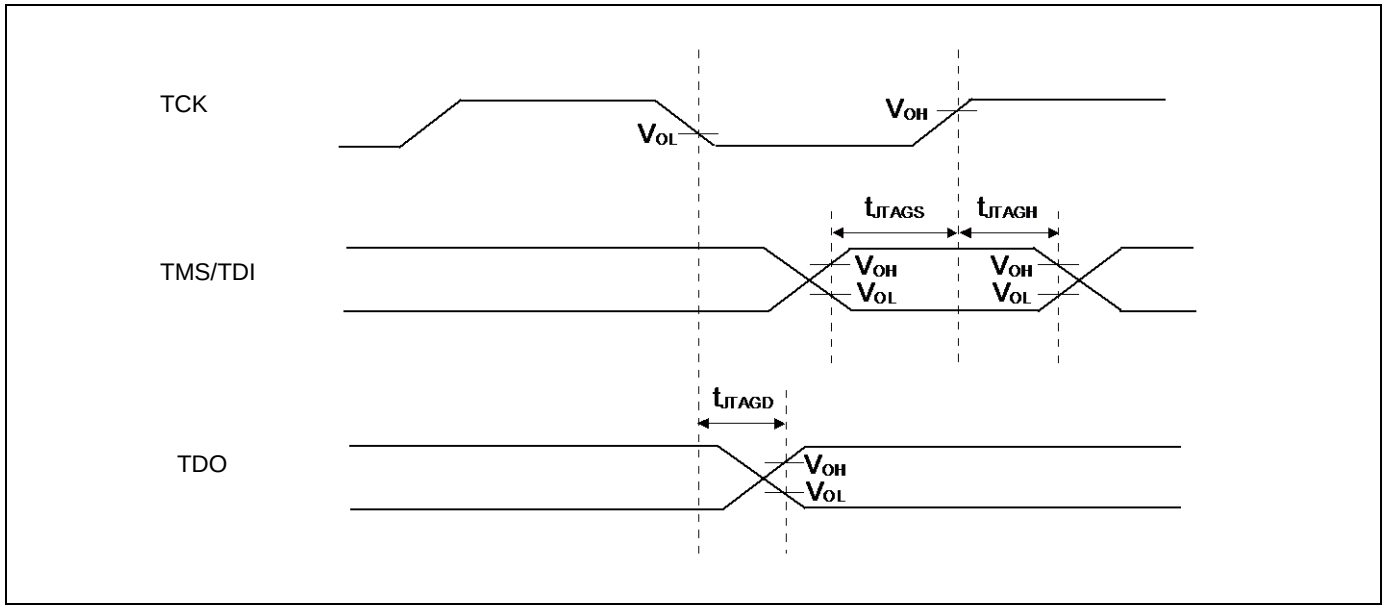


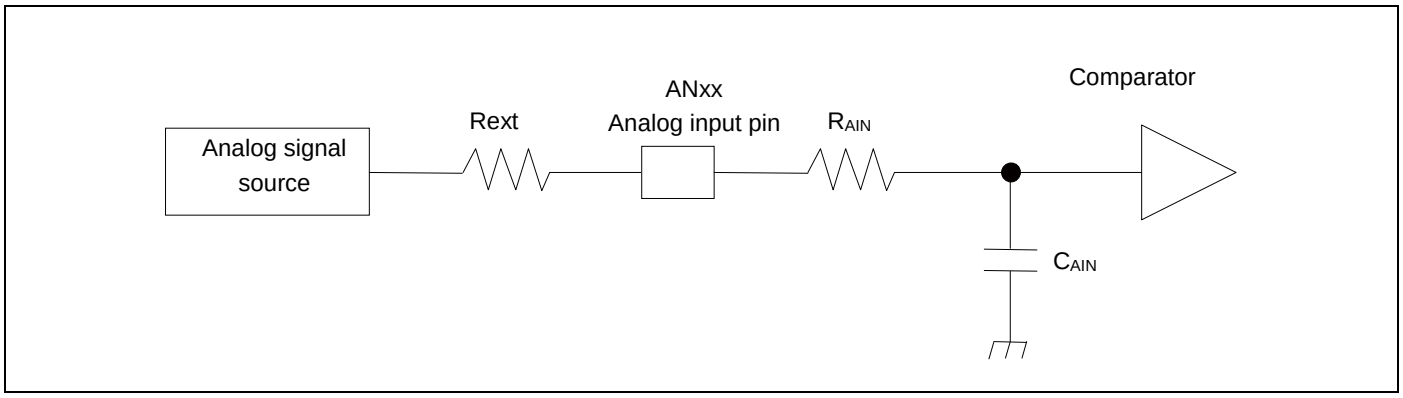
12.4.15 JTAG Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TMS, TDI hold time	t_{JTAGH}	TCK TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TDO delay time	t_{JTAGD}	TCK TDO	Vcc ≥ 4.5V	-	25	ns	
			Vcc < 4.5V	-	45		

Note: When the external load capacitance C_L = 30pF.





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts : Sampling time

R_{AIN} : input resistor of A/D = 2kΩ $4.5 \leq AV_{CC} \leq 5.5$

input resistor of A/D = 3.8kΩ $2.7 \leq AV_{CC} < 4.5$

C_{AIN} : input capacity of A/D = 12.9pF $2.7 \leq AV_{CC} \leq 5.5$

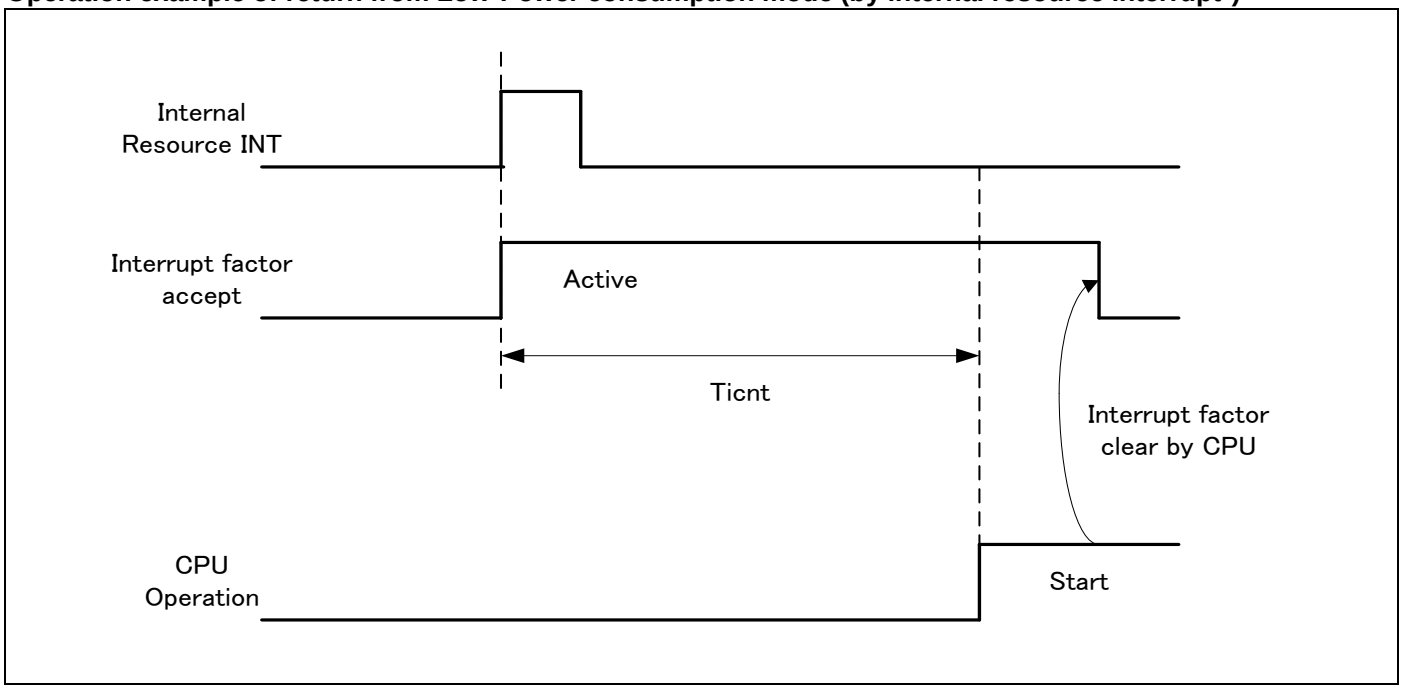
Rext : Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time

Tcck : Compare clock cycle

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)

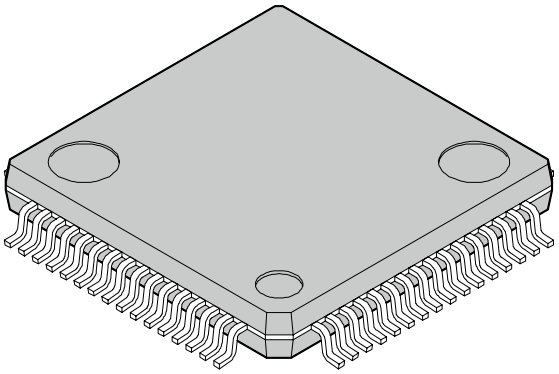


*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual about the return factor from Low-Power consumption mode.
- When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".

64-pin plastic LQFP

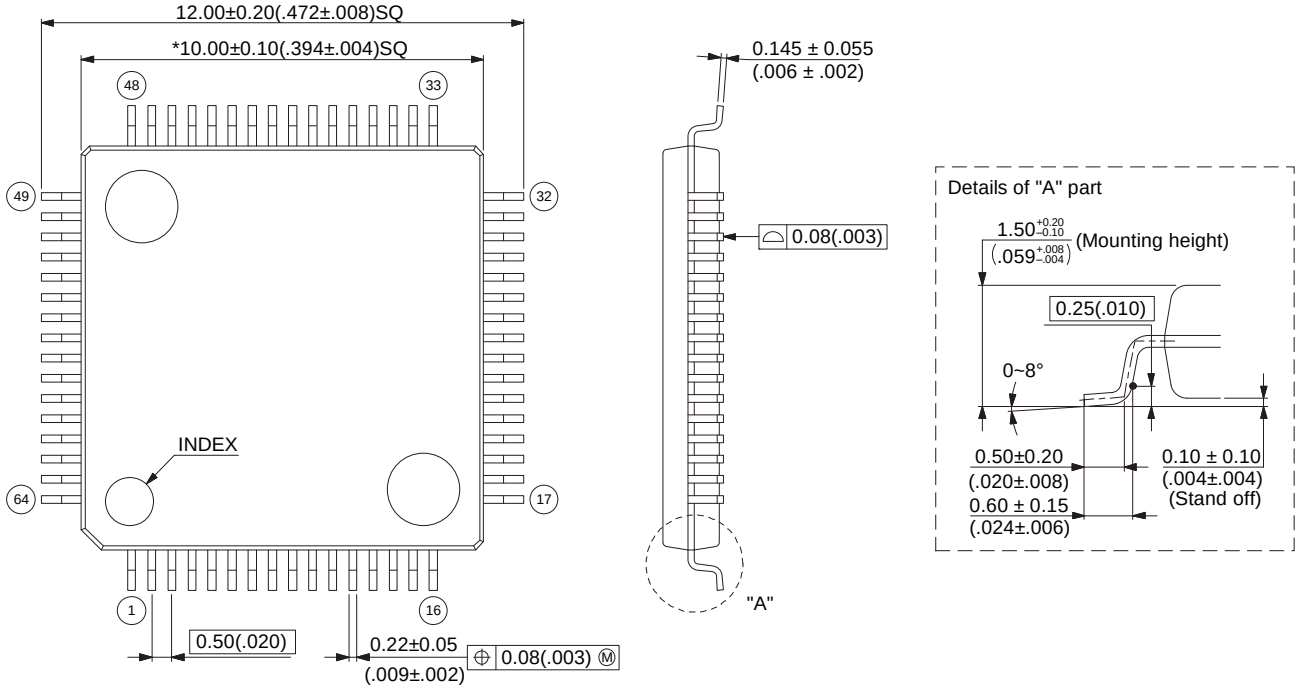


(FPT-64P-M38)

Lead pitch	0.50 mm
Package width × package length	10.00 mm × 10.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.