Infineon Technologies - MB9AF314LAPMC-G-JNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af314lapmc-g-jne2

2. Packages

Package \ Product name	MB9AF311LA MB9AF312LA MB9AF314LA	MB9AF311MA MB9AF312MA MB9AF314MA MB9AF315MA MB9AF316MA	MB9AF311NA MB9AF312NA MB9AF314NA MB9AF315NA MB9AF316NA
LQFP: FPT-64P-M38 (0.5mm pitch)	❍	-	-
LQFP: FPT-64P-M39 (0.65mm pitch)	❍	-	-
QFN : LCC-64P-M24 (0.5mm pitch)	❍	-	-
LQFP: FPT-80P-M37 (0.5mm pitch)	-	❍	-
LQFP: FPT-100P-M23 (0.5mm pitch)	-	-	❍
QFP : FPT-100P-M06 (0.65mm pitch)	-	-	❍
BGA : BGA-112P-M04 (0.8mm pitch)	-	-	❍*

❍: Supported
* : MB9AF315NA, MB9AF316NA are planning

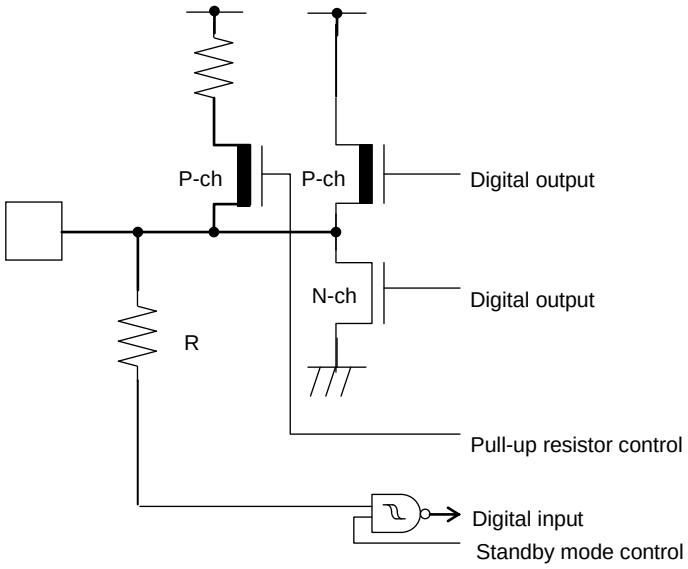
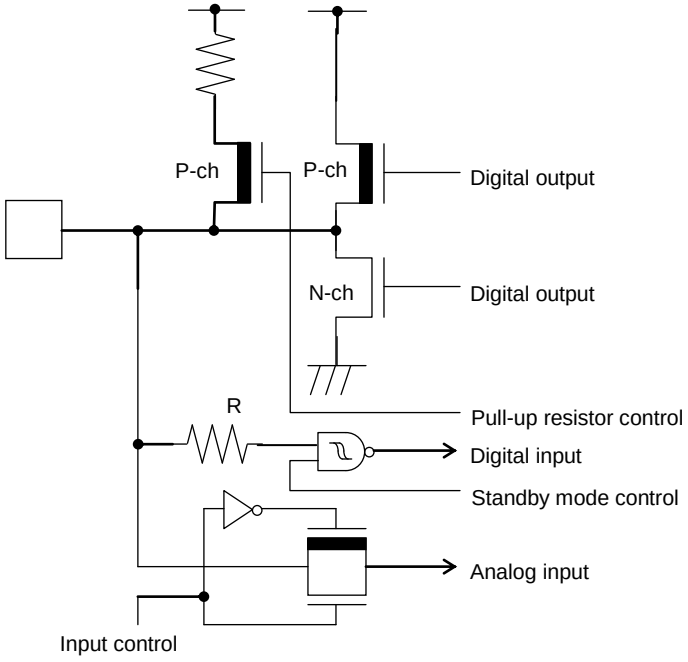
Note: Refer to “14. Package Dimensions” for detailed information on each package.

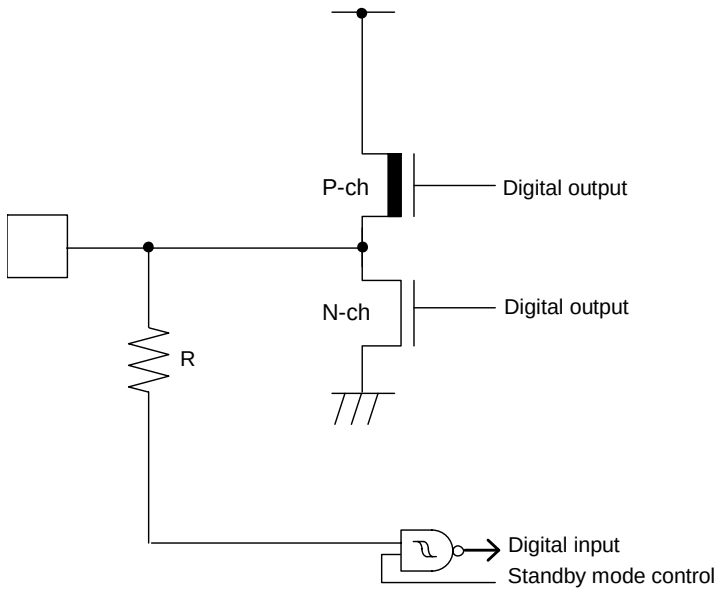
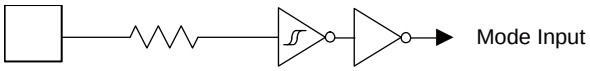
Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
7	85	D3	7	-	P55	E	I
					SCK6_0 (SCL6_0)		
					ADTG_1		
					RTO15_0 (PPG14_0)		
					MADATA05_1		
8	86	D5	8	-	P56	E	H
					INT08_2		
					DTTI1X_0		
					MADATA06_1		
9	87	E1	9	5	P30	E	H
					AIN0_0		
					TIOB0_1		
					INT03_2		
				-	MADATA07_1		
10	88	E2	10	6	P31	E	H
					BIN0_0		
					TIOB1_1		
					SCK6_1 (SCL6_1)		
					INT04_2		
				-	MADATA08_1		
11	89	E3	11	7	P32	E	H
					ZIN0_0		
					TIOB2_1		
					SOT6_1 (SDA6_1)		
					INT05_2		
				-	MADATA09_1		
12	90	E4	12	8	P33	E	H
					INT04_0		
					TIOB3_1		
					SIN6_1		
					ADTG_6		
				-	MADATA10_1		
13	91	F1	-	-	P34	E	I
					FRCK0_0		
					TIOB4_1		
					MADATA11_1		

Pin No					Pin name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64			
14	92	F2	-	-	P35 IC03_0 TIOB5_1 INT08_1 MADATA12_1	E	H
15	93	F3	-	-	P36 IC02_0 SIN5_2 INT09_1 MADATA13_1	E	H
16	94	G1	-	-	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	H
17	95	G2	-	-	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	H
18	96	F4	13	9	P39 DTTI0X_0 ADTG_2	E	I
19	97	G3	14	10	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
20	98	H1	15	11	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	99	H2	16	12	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	100	G4	17	13	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
-	-	B2	-	-	VSS	-	

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
External Bus	MCSX0_1	External bus interface chip select output pin	88	66	A6	68	-
	MCSX1_1		87	65	D7	67	-
	MCSX2_1		86	64	C7	-	-
	MCSX3_1		85	63	B7	-	-
	MCSX4_1		83	61	D9	-	-
	MCSX5_1		82	60	C8	-	-
	MCSX6_1		79	57	B11	63	-
	MCSX7_1		77	55	A9	61	-
	MDQM0_1	External bus interface byte mask signal output	90	68	C6	70	-
	MDQM1_1		91	69	A5	71	-
	MOEX_1	External bus interface read enable signal for SRAM	94	72	C5	74	-
	MWEX_1	External bus interface write enable signal for SRAM	93	71	D6	73	-
	MADATA00_1	External bus interface data bus	2	80	C1	2	-
	MADATA01_1		3	81	C2	3	-
	MADATA02_1		4	82	B3	4	-
	MADATA03_1		5	83	D1	5	-
	MADATA04_1		6	84	D2	6	-
	MADATA05_1		7	85	D3	7	-
	MADATA06_1		8	86	D5	8	-
	MADATA07_1		9	87	E1	9	-
	MADATA08_1		10	88	E2	10	-
	MADATA09_1		11	89	E3	11	-
	MADATA10_1		12	90	E4	12	-
	MADATA11_1		13	91	F1	-	-
	MADATA12_1		14	92	F2	-	-
	MADATA13_1		15	93	F3	-	-
	MADATA14_1		16	94	G1	-	-
	MADATA15_1		17	95	G2	-	-
	MALE_1	Address Latch enable signal for multiplex	89	67	B6	69	-
	MRDY_1	External RDY input signal	96	74	C4	76	-
	MCLKOUT_1	External bus clock output	84	62	A7	66	-

Module	Pin name	Function	Pin No				
			LQFP-100	QFP-100	BGA-112	LQFP-80	LQFP-64 QFN-64
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	87	65	D7	67	54
	SIN4_1		65	43	F9	55	-
	SIN4_2		82	60	C8	-	-
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	55
	SOT4_1 (SDA4_1)		66	44	E11	56	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	90	68	C6	70	-
	RTS4_1		69	47	E9	-	-
	RTS4_2		86	64	C7	-	-
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	91	69	A5	71	-
	CTS4_1		68	46	F8	-	-
	CTS4_2		85	63	B7	-	-
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	96	74	C4	76	60
	SIN5_2		15	93	F3	-	-
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • I_{OH} = - 4mA, I_{OL} = 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input

List of Pin Status

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enabled	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*[1]/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*[1]/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or resource other than above selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	Vcc	Vss - 0.5	Vss + 6.5	V	
Power supply voltage (for USB) *1, *3	USBVcc	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage*1, *4	AVcc	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage*1, *4	AVRH	Vss - 0.5	Vss + 6.5	V	
Input voltage*1	V_I	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	Except for USB pin
		Vss - 0.5	USBVcc + 0.5 (≤ 6.5V)	V	USB pin
		Vss - 0.5	Vss + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	Vss - 0.5	AVcc + 0.5 (≤ 6.5V)	V	
Output voltage*1	V_O	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
"L" level maximum output current*5	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80, P81
"L" level average output current*6	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			18.5	mA	P80, P81
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*5	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80, P81
"H" level average output current*6	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 20.5	mA	P80, P81
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that Vss = AVss = 0.0V.

*2: Vcc must not drop below Vss - 0.5V.

*3: USBVcc must not drop below Vss - 0.5V.

*4: Be careful not to exceed Vcc + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

12.4.4 Operating Conditions of Main PLL and USB PLL (In the case of using main clock for input clock of PLL)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	
USB clock frequency*3	$F_{CLKSPLL}$	-	-	48	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

*3: For more information about USB clock, see "Chapter 2-2: USB Clock Generation" in "FM3 Family Peripheral Manual Communication Macro Part".

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in high speed CR for the input clock of the main PLL)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

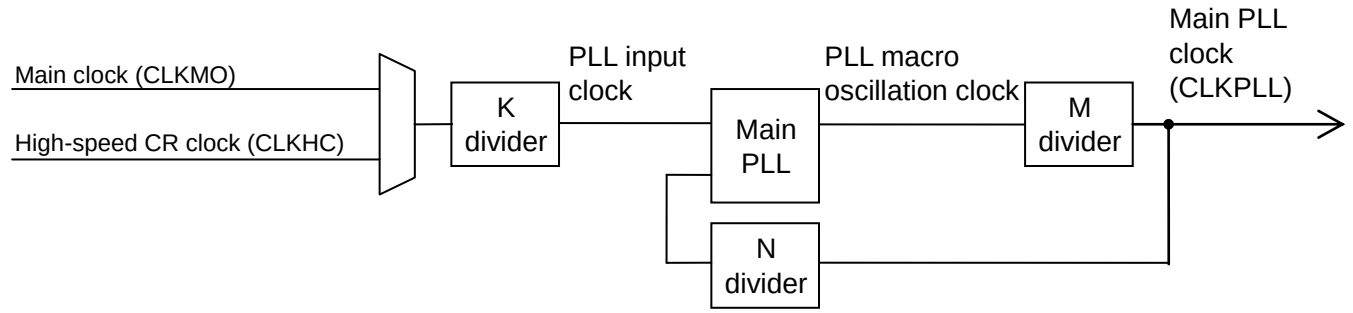
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*1	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	300	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



12.4.8 External Bus Timing

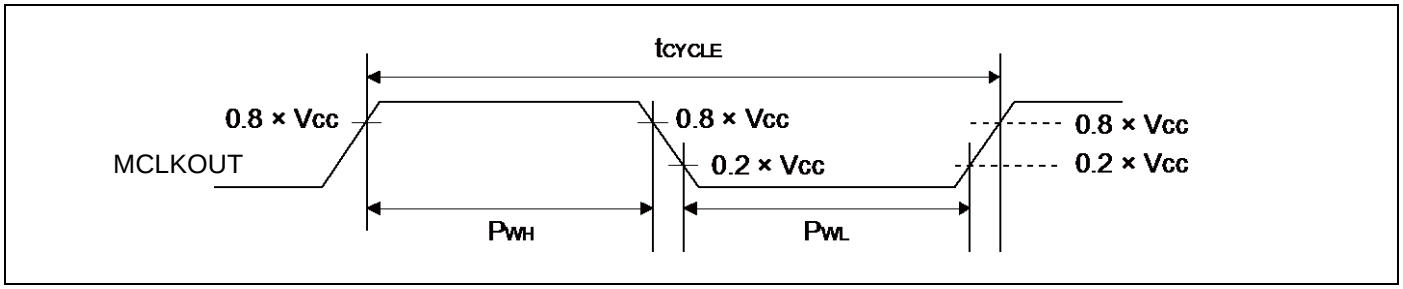
External bus clock output characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT	Vcc ≥ 4.5 V	-	40	MHz
			Vcc < 4.5 V	-	32	MHz
Minimum clock cycle time	-		Vcc ≥ 4.5 V	25	-	ns
			Vcc < 4.5 V	31.25	-	ns

Note: The external bus clock output is a divided clock of HCLK. For more information about setting of clock divider, see "Chapter 12: External Bus Interface" in "FM3 Family Peripheral Manual"

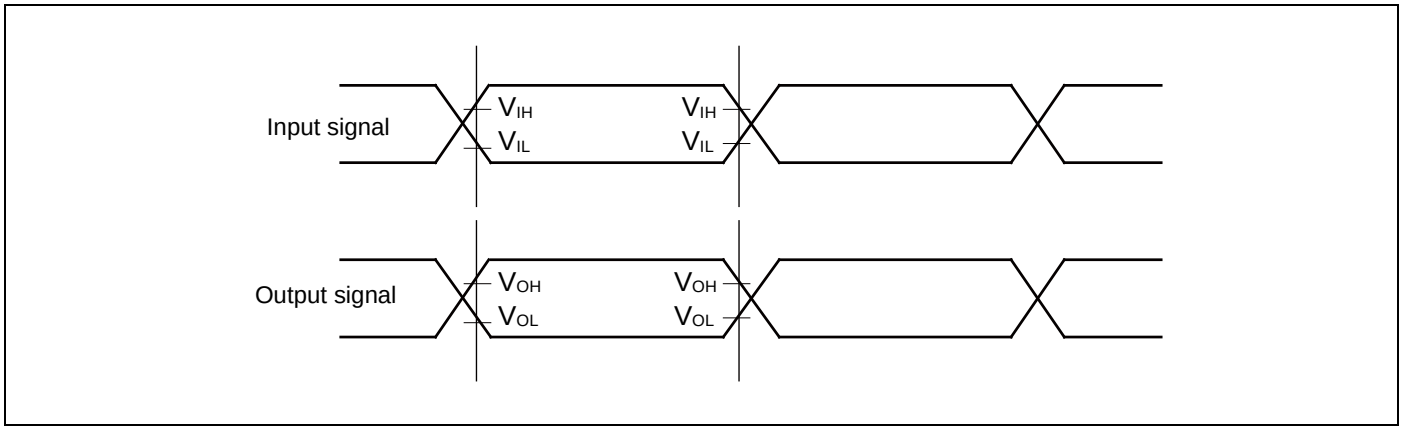
When external bus clock is not output, this characteristic does not give any effect on external bus operation.



External bus signal input/output characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



12.4.10 CSIO/UART Timing

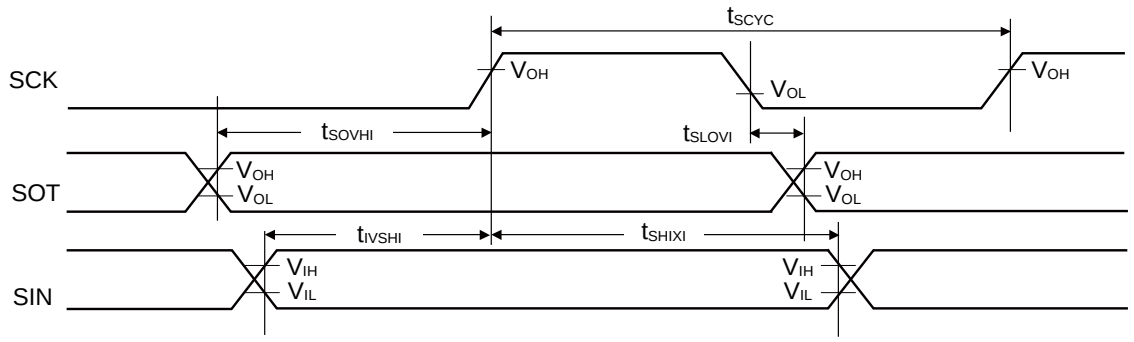
CSIO (SPI = 0, SCINV = 0)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

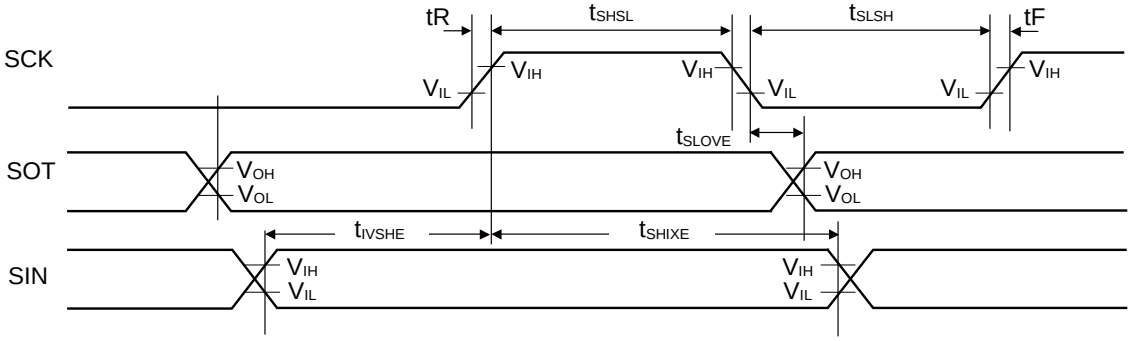
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑→ SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



Master mode

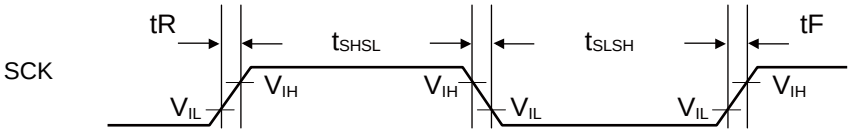


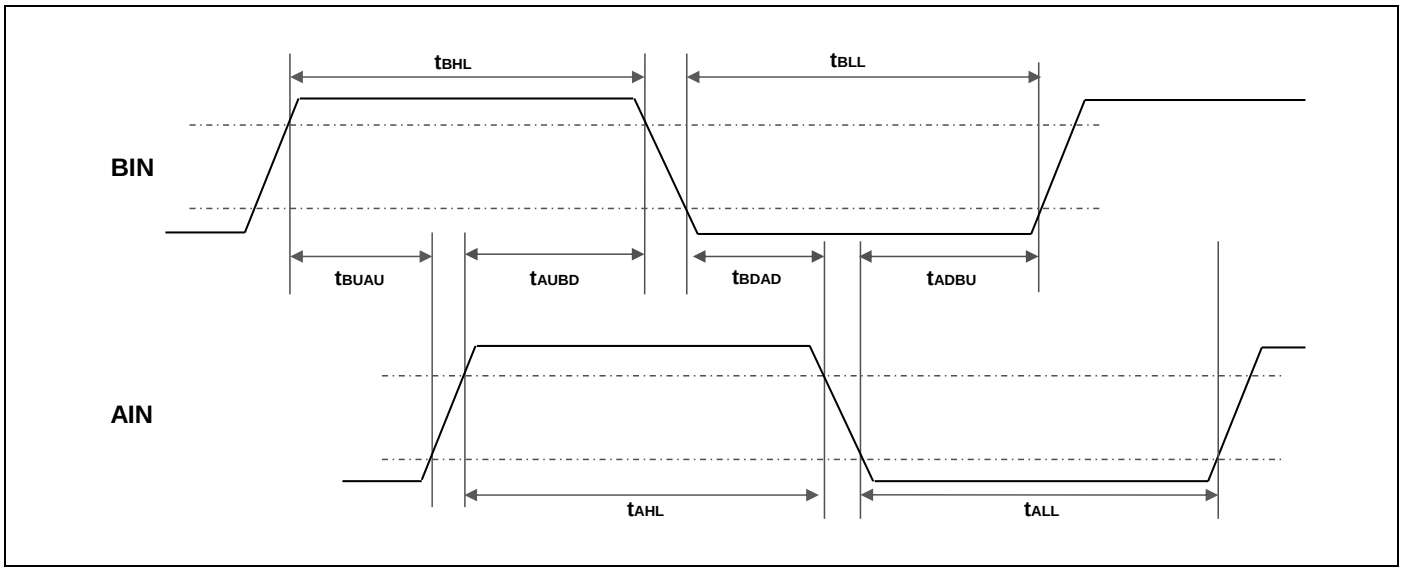
Slave mode

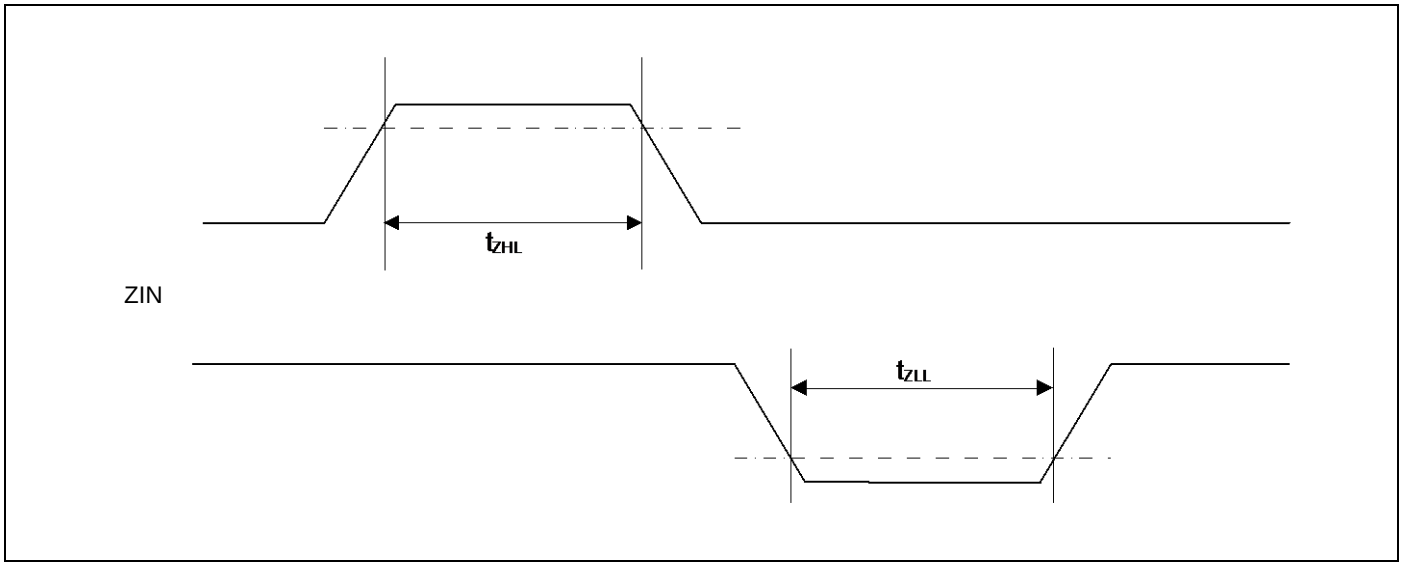
UART external clock input (EXT = 1)

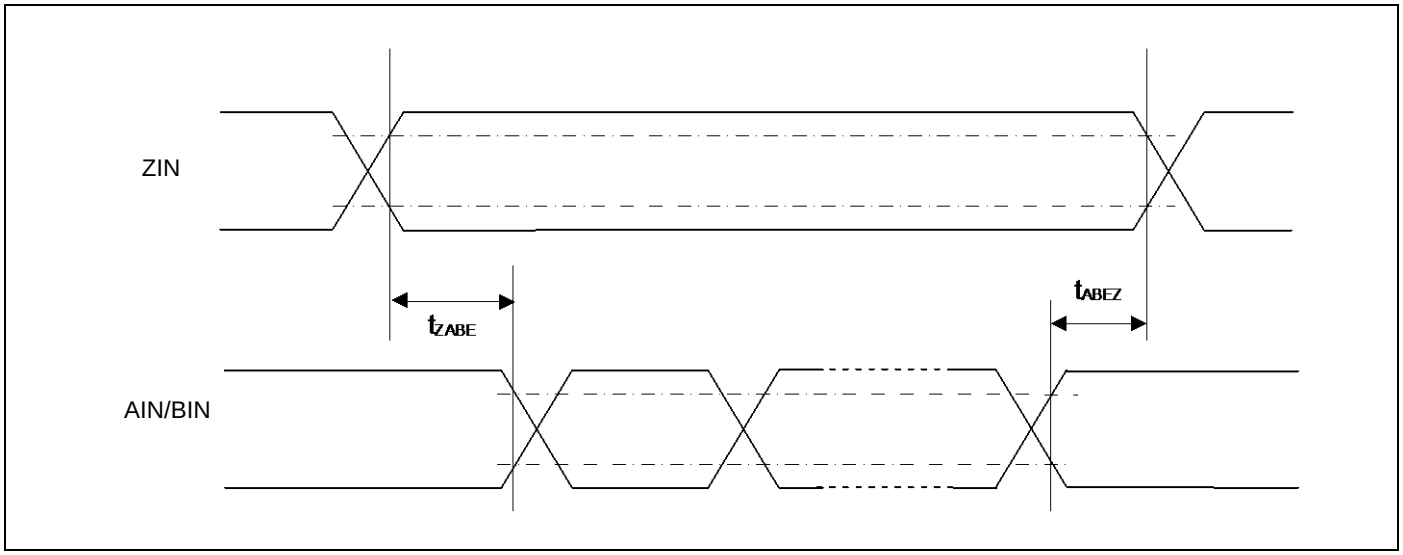
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t_{SLSH}	C_L = 30pF	tcycp + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		tcycp + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



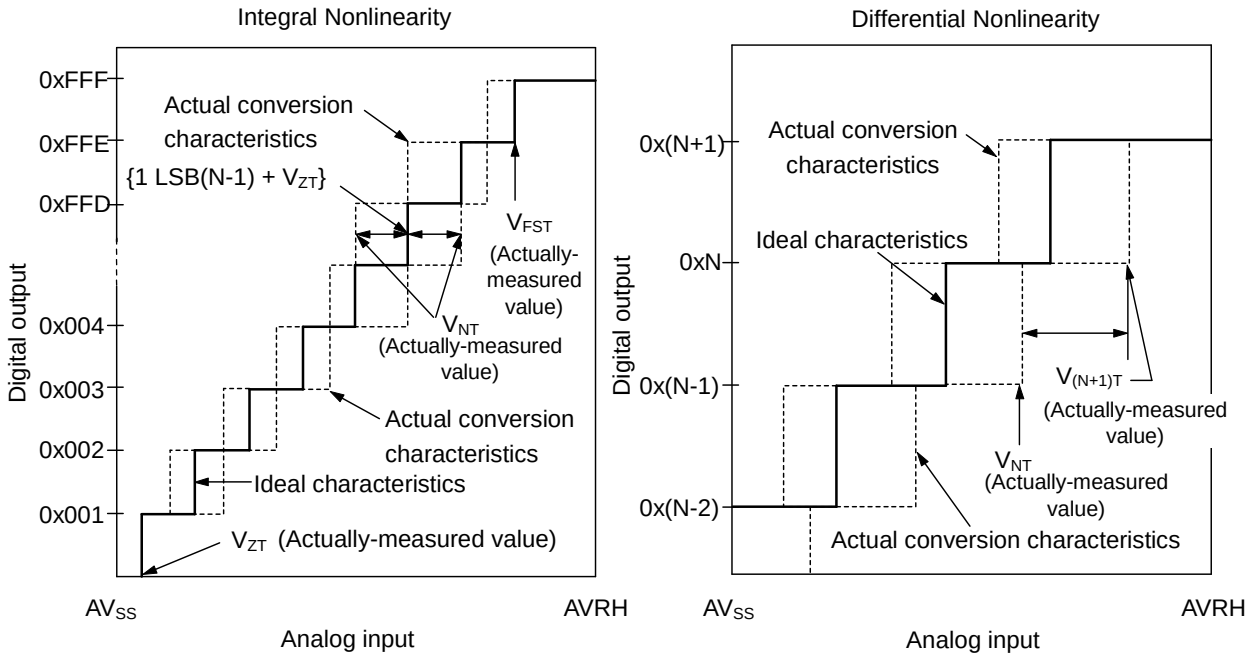

tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

Definition of 12-bit A/D Converter Terms

- ■ Resolution : Analog variation that is recognized by an A/D converter.
- ■ Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
- ■ Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

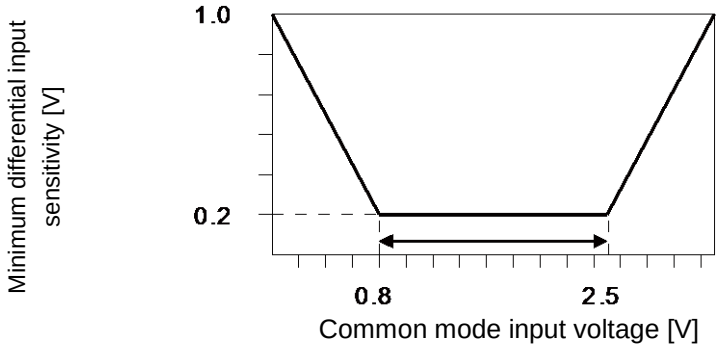
12.6 USB characteristics

(Vcc = 2.7V to 5.5V, USBVcc = 3.0V to 3.6V, Vss = 0V, Ta = - 40°C to + 105°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input High level voltage	V_{IH}	UDP0, UDM0	-	2.0	USBVcc + 0.3	V	*1
	Input Low level voltage	V_{IL}		-	Vss - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}		External pull-down resistance = 15kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}		External pull-up resistance = 1.5kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full Speed	4	20	ns	*5
	Falling time	t_{FF}		Full Speed	4	20	ns	*5
	Rise/fall time matching	t_{FRFM}		Full Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low Speed	75	300	ns	*7
	Falling time	t_{LF}		Low Speed	75	300	ns	*7
	Rise/fall time matching	t_{LRFM}		Low Speed	80	125	%	*7

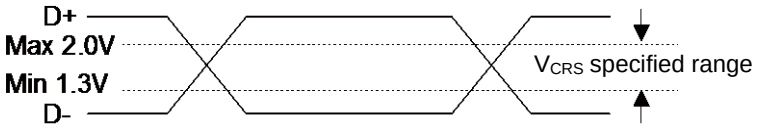
*1: The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hystereses to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.

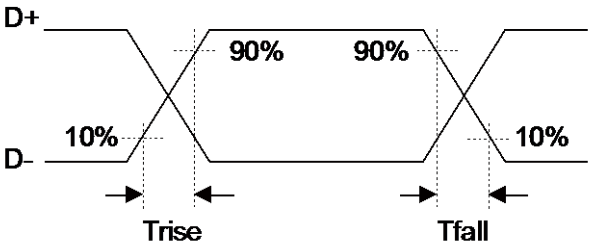


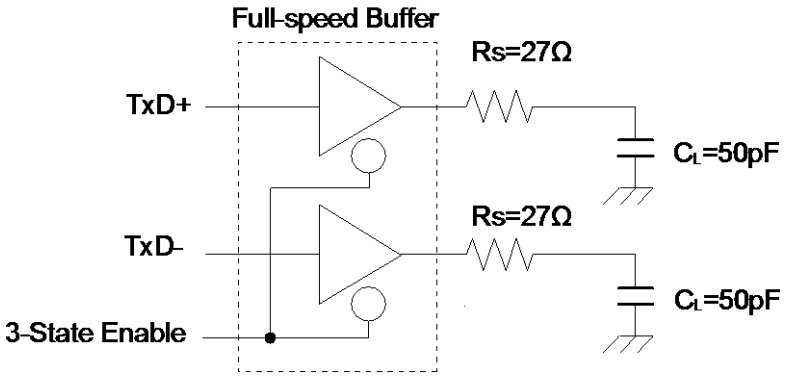
*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the ground and 1.5 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



*5: They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.





12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

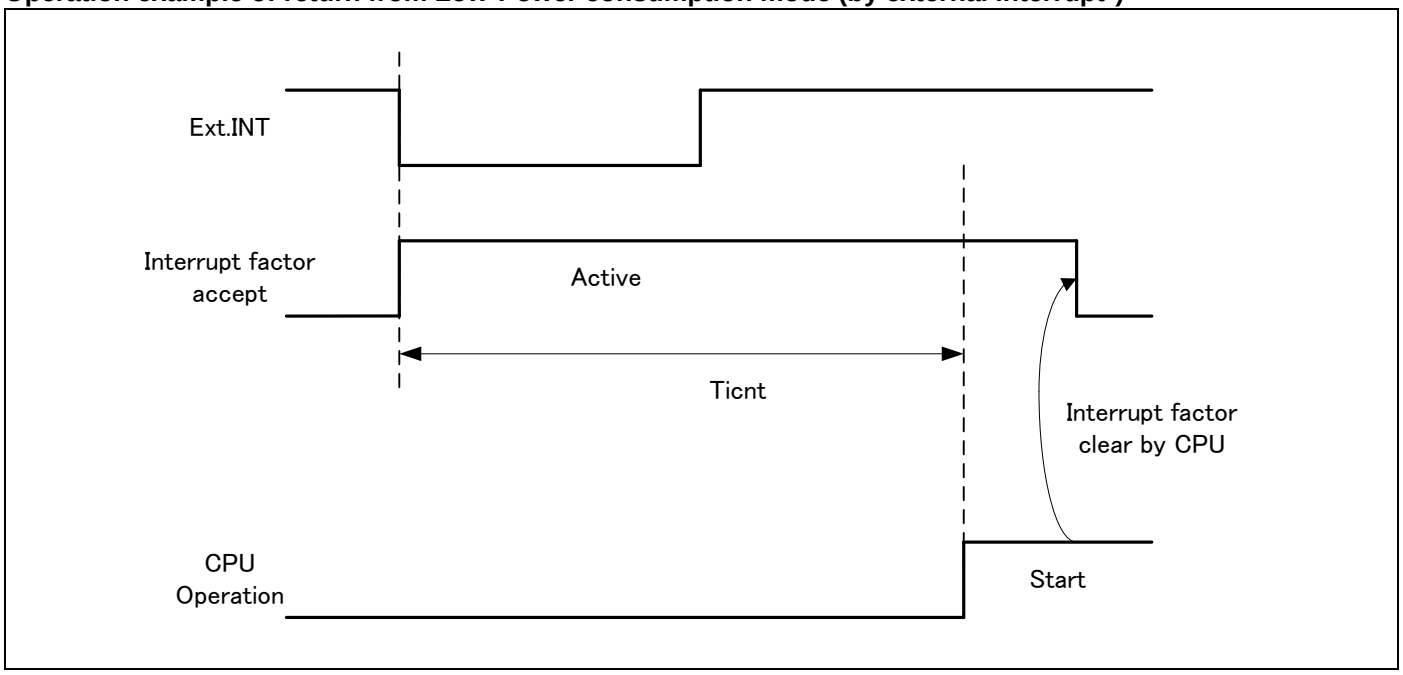
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		40	80	µs	
Low-speed CR TIMER mode		453	737	µs	
Sub TIMER mode		453	737	µs	
STOP mode		453	737	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)

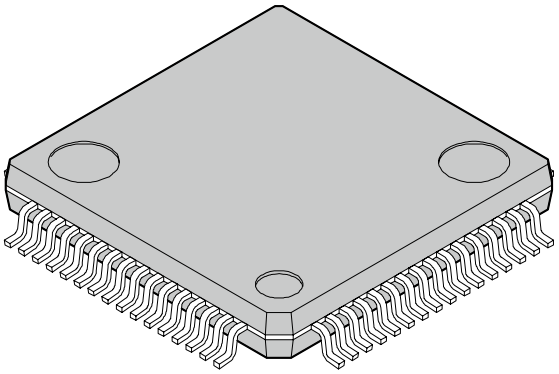


*: External interrupt is set to detecting fall edge.

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF311LAPMC1-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),64-pin (FPT-64P-M38)	Tray
MB9AF312LAPMC1-G-JNE2	128Kbyte	16Kbyte		
MB9AF314LAPMC1-G-JNE2	256Kbyte	32Kbyte		
MB9AF311LAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.65mm pitch),64-pin (FPT-64P-M39)	
MB9AF312LAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314LAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF311LAQN-G-AVE2	64Kbyte	16Kbyte	Plastic □ QFN (0.5mm pitch),64-pin (LCC-64P-M24)	
MB9AF312LAQN-G-AVE2	128Kbyte	16Kbyte		
MB9AF314LAQN-G-AVE2	256Kbyte	32Kbyte		
MB9AF311MAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),80-pin (FPT-80P-M37)	
MB9AF312MAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314MAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF315MAPMC-G-JNE2	384Kbyte	32Kbyte		
MB9AF316MAPMC-G-JNE2	512Kbyte	32Kbyte		
MB9AF311NAPMC-G-JNE2	64Kbyte	16Kbyte	Plastic □ LQFP (0.5mm pitch),100-pin (FPT-100P-M23)	
MB9AF312NAPMC-G-JNE2	128Kbyte	16Kbyte		
MB9AF314NAPMC-G-JNE2	256Kbyte	32Kbyte		
MB9AF315NAPMC-G-JNE2	384Kbyte	32Kbyte		
MB9AF316NAPMC-G-JNE2	512Kbyte	32Kbyte		
MB9AF311NAPF-G-JNE1	64Kbyte	16Kbyte	Plastic □ QFP (0.65mm pitch), 100-pin (FPT-100P-M06)	
MB9AF312NAPF-G-JNE1	128Kbyte	16Kbyte		
MB9AF314NAPF-G-JNE1	256Kbyte	32Kbyte		
MB9AF315NAPF-G-JNE1	384Kbyte	32Kbyte		
MB9AF316NAPF-G-JNE1	512Kbyte	32Kbyte		
MB9AF311NABGL-GE1	64Kbyte	16Kbyte	Plastic □ PFBGA (0.8mm pitch),112-pin (BGA-112P-M04)	
MB9AF312NABGL-GE1	128Kbyte	16Kbyte		
MB9AF314NABGL-GE1	256Kbyte	32Kbyte		

64-pin plastic LQFP

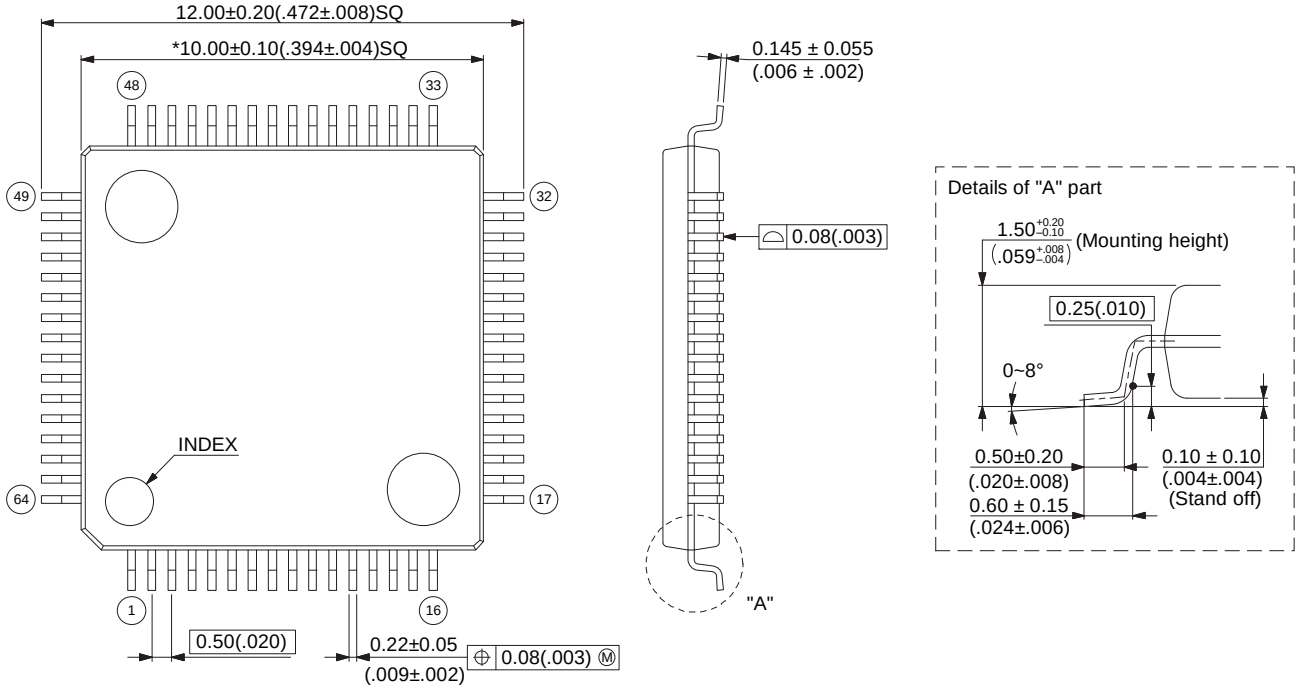


(FPT-64P-M38)

Lead pitch	0.50 mm
Package width × package length	10.00 mm × 10.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.