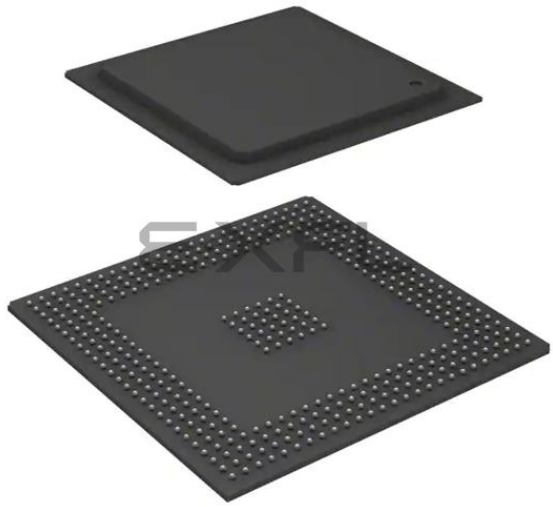

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V4E
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	99
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5484cvr200

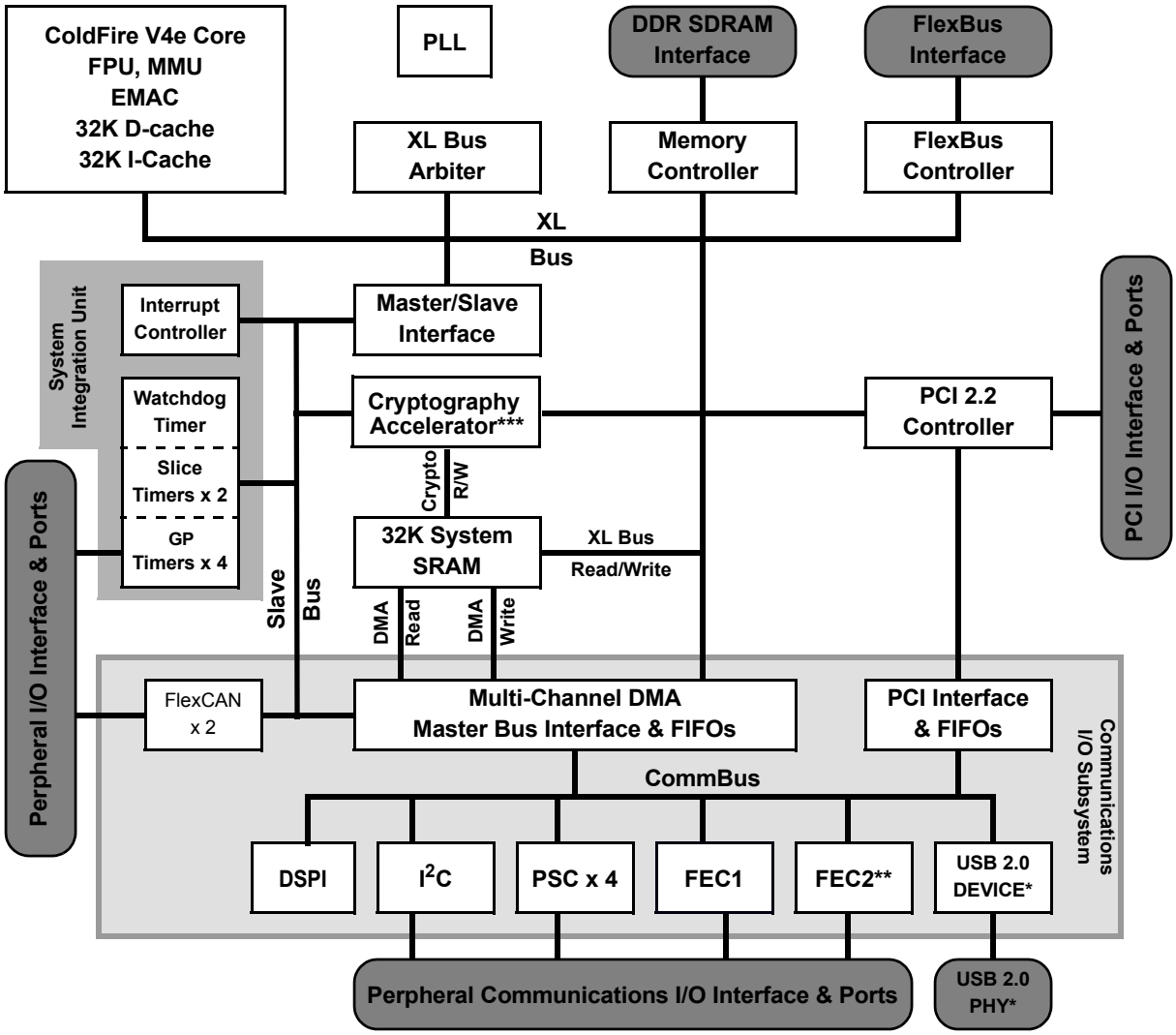


Figure 1. MCF548X Block Diagram

1 Maximum Ratings

Table 1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 1. Absolute Maximum Ratings

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	EV_{DD}	–0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	–0.5 to +2.0	V
Memory (I/O pads) supply voltage (2.5-V power pins)	SD V_{DD}	–0.3 to +4.0 SDR Memory –0.3 to +2.8 DDR Memory	V
PLL supply voltage	PLL V_{DD}	–0.5 to +2.0	V
Internal logic supply voltage, input voltage level	V_{in}	–0.5 to +3.6	V
Storage temperature range	T_{stg}	–55 to +150	°C

2 Thermal Characteristics

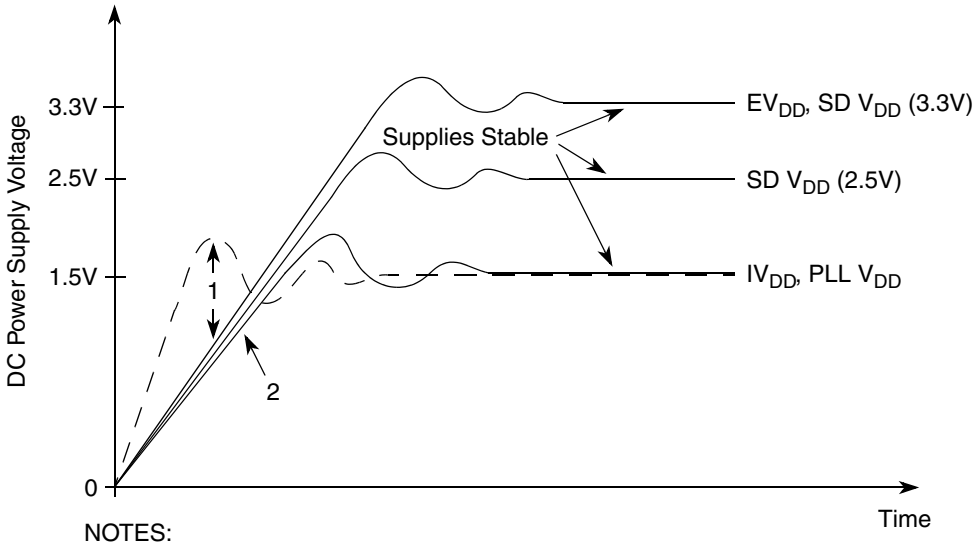
2.1 Operating Temperatures

Table 2 lists junction and ambient operating temperatures.

Table 2. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T_j	105	°C
Maximum operating ambient temperature	T_{Amax}	<85[1]	°C
Minimum operating ambient temperature	T_{Amin}	–40	°C

1 This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.



NOTES:
1. IVDD should not exceed EVDD or SD VDD by more than 0.4V at any time, including power-up.
2. Recommended that IVDD/PLL VDD should track EVDD/SD VDD up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EVDD, SD VDD, IVDD, or PLL VDD) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

The relationship between SD V_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SD V_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

4.2.1 Power Up Sequence

If EV_{DD}/SD V_{DD} are powered up with the IV_{DD} at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SD V_{DD} to be in a high impedance state. There is no limit to how long after EV_{DD}/SD V_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SD V_{DD}, or PLL V_{DD} by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PLL V_{DD} and EV_{DD}/SD V_{DD} should track up to 0.9V, then separate for the completion of ramps with EV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

4.2.2 Power Down Sequence

If IV_{DD}PLL V_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PLL V_{DD} power down before EV_{DD} or SD V_{DD} must power down. IV_{DD} should not lag EV_{DD}, SD V_{DD}, or PLL V_{DD} going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PLL V_{DD} to 0V
2. Drop EV_{DD}/SD V_{DD} supplies

4.4 USB Power Filtering

To minimize noise, an external filter is required for each of the USB power pins. The filter shown in Figure 6 should be connected between the board EV_{DD} or IV_{DD} and each of the USB V_{DD} pins.

- The resistor and capacitors should be placed as close to the dedicated USB V_{DD} pin as possible.
- A separate filter circuit should be included for each USB V_{DD} pin, a total of five circuits.
- All traces should be as low impedance as possible, especially ground pins to the ground plane.
- The filter for USB_PHYVDD to VSS should be connected to the power and ground planes, respectively, not fingers of the planes.
- In addition to keeping the filter components for the USB_PLLVDD as close as practical to the body of the processor as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the processor.
- The capacitors for C2 in the table below should be rated X5R or better due to temperature performance.

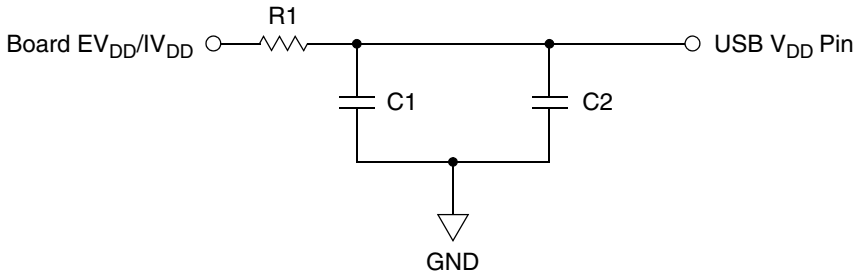


Figure 6. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

Table 5 lists the resistor values and supply voltages to be used in the circuit for each of the USB V_{DD} pins.

Table 5. USB Filter Circuit Values

USB V_{DD} Pin	Nominal Voltage	R1 (Ω)	C1 (μF)	C2 (μF)
USBVDD (Bias generator supply)	3.3V	10	10	0.1
USB_PHYVDD (Main transceiver supply)	3.3V	0	10	0.1
USB_PLLVDD (PLL supply)	1.5V	10	1	0.1
USB_OSCVDD (Oscillator supply)	3.3V	0	10	0.1
USB_OSCAVDD (Oscillator analog supply)	1.5V	0	10	0.1

4.4.1 Bias Resistor

The USBRBIAS resistor should be placed as close to the dedicated USB 2.0 pins as possible. The tolerance should be ±1%.

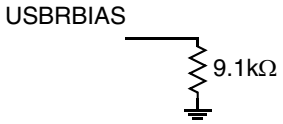


Figure 7. USBRBIAS Connection

5 Output Driver Capability and Loading

Table 6 lists values for drive capability and output loading.

Table 6. I/O Driver Capability[1]

Signal	Drive Capability	Output Load (C_L)
SDRAMC (SDADDR[12:0], SDDATA[31:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, SDDM[3:0], $\overline{\text{SDWE}}$, SDBA[1:0]	24 mA	15 pF
SDRAMC DQS and clocks (SDDQS[3:0], SDRDQS, SDCLK[1:0], $\overline{\text{SDCLK}}$[1:0], SDCKE)	24 mA	15 pF
SDRAMC chip selects ($\overline{\text{SDCS}}$[3:0])	24 mA	15 pF
FlexBus (AD[31:0], $\overline{\text{FBCS}}$[5:0], ALE, R/$\overline{\text{W}}$, $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$)	16 mA	30 pF
FEC (E*n*MDIO, E*n*MDC, E*n*TXEN, E*n*TXD[3:0], E*n*TXER	8 mA	15 pF
Timer (TOUT[3:0])	8 mA	50 pF
FlexCAN (CANTX)	8 mA	30 pF
$\overline{\text{DACK}}$[1:0]	8 mA	30 pF
PSC (PSC*n*TXD[3:0], $\overline{\text{PSC}n\text{RTS}}$/PSC*n*FSYNC,	8 mA	30 pF
DSPI (DSPISOUT, DSPICS0/SS, DSPICS[2:3], DSPICS5/PCSS)	24 mA	50 pF
PCI (PCIAD[31:0], PCIBG[4:1], PCIBG0/PCIREQOUT, PCIDEVSEL, PCICXBE[3:0], PCIFRM, PCIPERR, PCIRESET, PCISERR, PCISTOP, PCIPAR, PCITRDY, PCIIRDY	16 mA	50 pF
I2C (SCL, SDA)	8 mA	50 pF
BDM (PSTCLK, PSTDDATA[7:0], DSO/TDO,	8 mA	25 pF
RSTO	8 mA	50 pF

1 The device's pads have balanced sink and source current. The drive capability is the same as the sink capability.

6 PLL Timing Specifications

The specifications in Table 7 are for the CLKIN pin.

Table 7. Clock Timing Specifications

Num	Characteristic	Min	Max	Units
C1	Cycle time	20	40	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

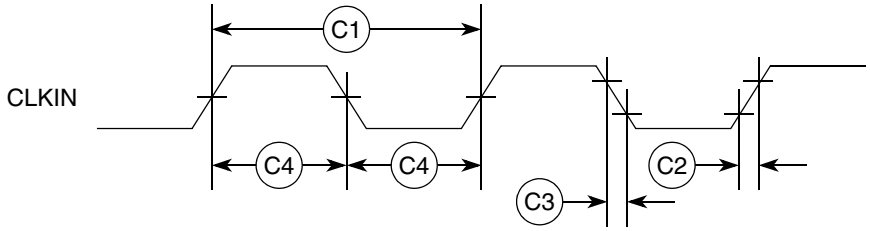


Figure 8. Input Clock Timing Diagram

Table 8 shows the supported PLL encodings.

Table 8. MCF548x Divide Ratio Encodings

AD[12:8][1]	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.67–50.0	83.33–100	166.66–200
00101	1:2	25.0–41.67	50.0–83.33[2]	100.0–166.66
01111	1:4	25.0	100	200

1 All other values of AD[12:8] are reserved.

2 DDR memories typically have a minimum speed of 83 MHz. Some vendors specifiy down to 75 MHz. Check with the memory component specifications to verify.

Figure 9 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

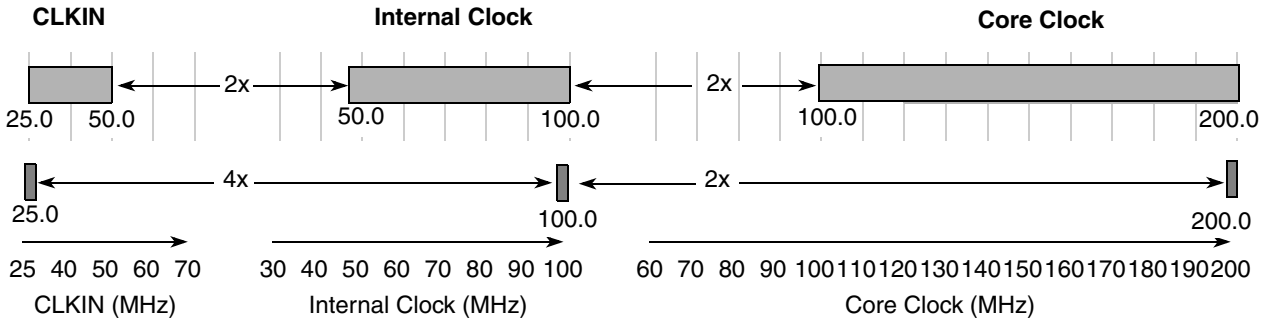


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 10. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	50	Mhz	1
FB1	Clock Period (CLKIN)	20	40	ns	2
FB2	Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, ALE, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	—	7.0	ns	3
FB3	Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, ALE, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	1	—	ns	3, 4
FB4	Data Input Setup	3.5	—	ns	
FB5	Data Input Hold	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	0	—	ns	
FB8	Address Output Valid (PCIAD[31:0])	—	7.0	ns	5
FB9	Address Output Hold (PCIAD[31:0])	0	—	ns	5

1 The frequency of operation is the same as the PCI frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI.

2 Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

3 Timing for chip selects only applies to the FBCS[5:0] signals. Please see Section 9.2, “DDR SDRAM AC Timing Characteristics” for SDCS[3:0] timing.

4 The FlexBus supports programming an extension of the address hold. Please consult the MCF548X specification manual for more information.

5 These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

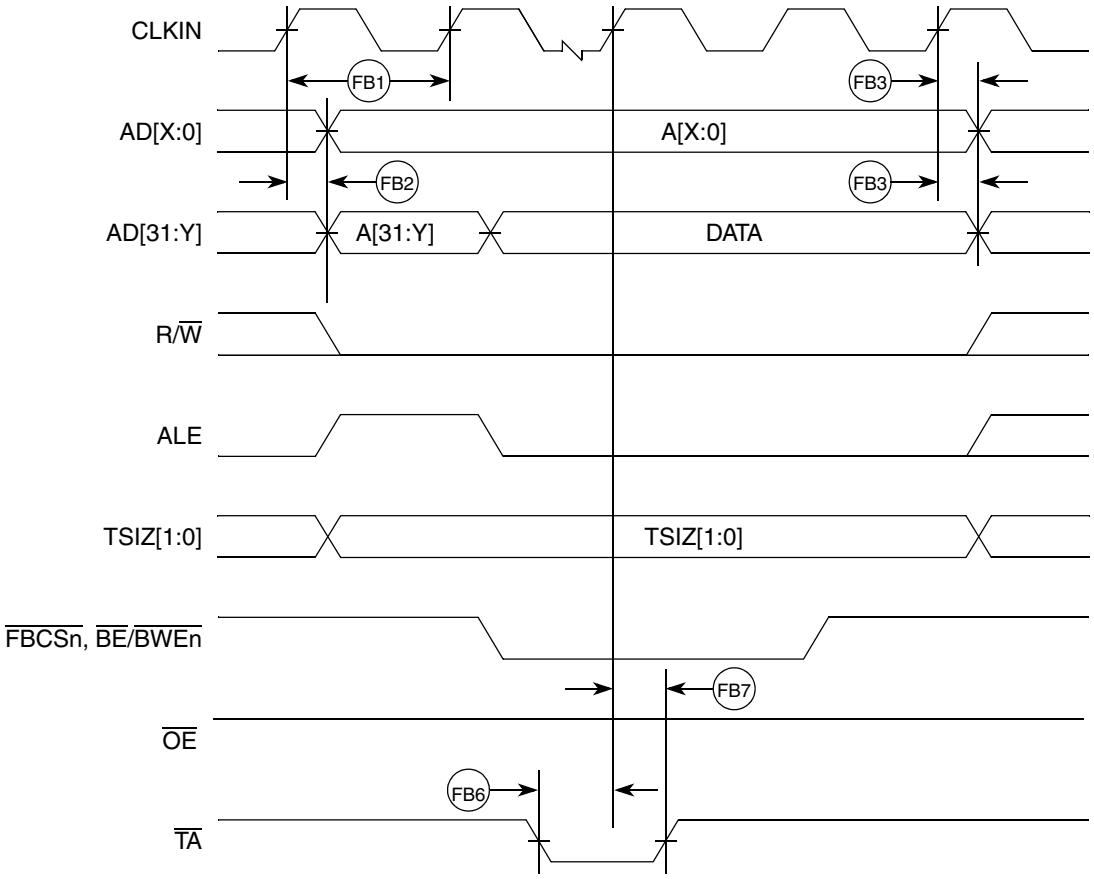


Figure 12. FlexBus Write Timing

9 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

9.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SDR_DQS on read cycles. The MCF548*x* SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must be supplied to the MCF548*x* for each data beat of an SDR read. The MCF548*x* accomplishes this by asserting a signal called SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR_DQS signal and its usage.

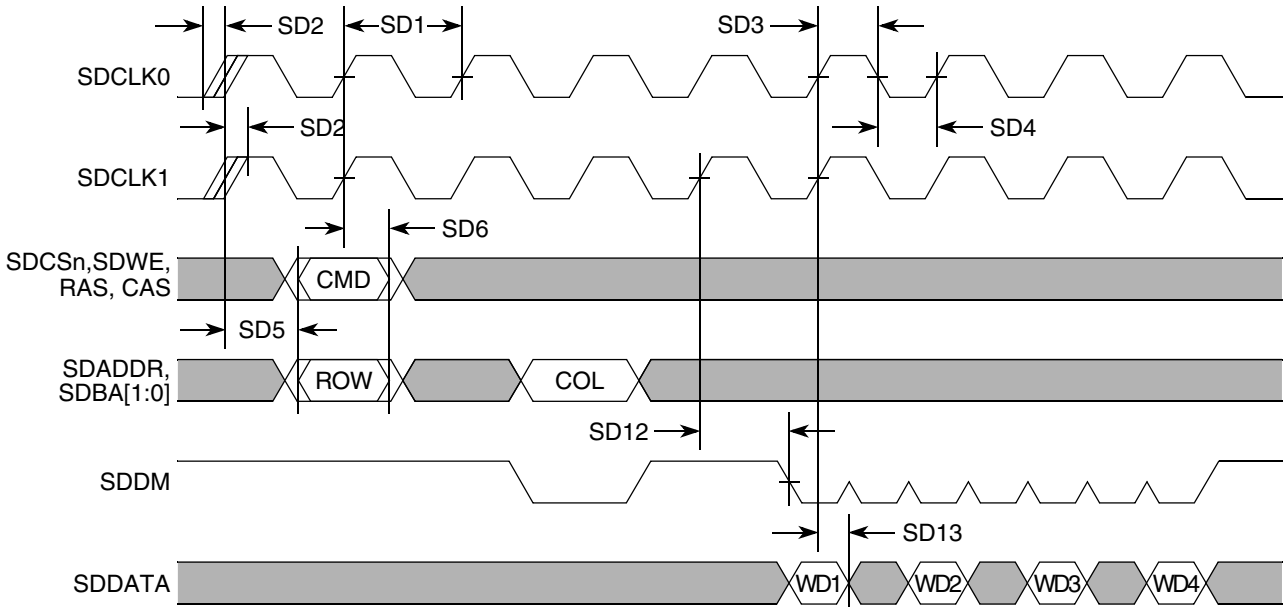


Figure 13. SDR Write Timing

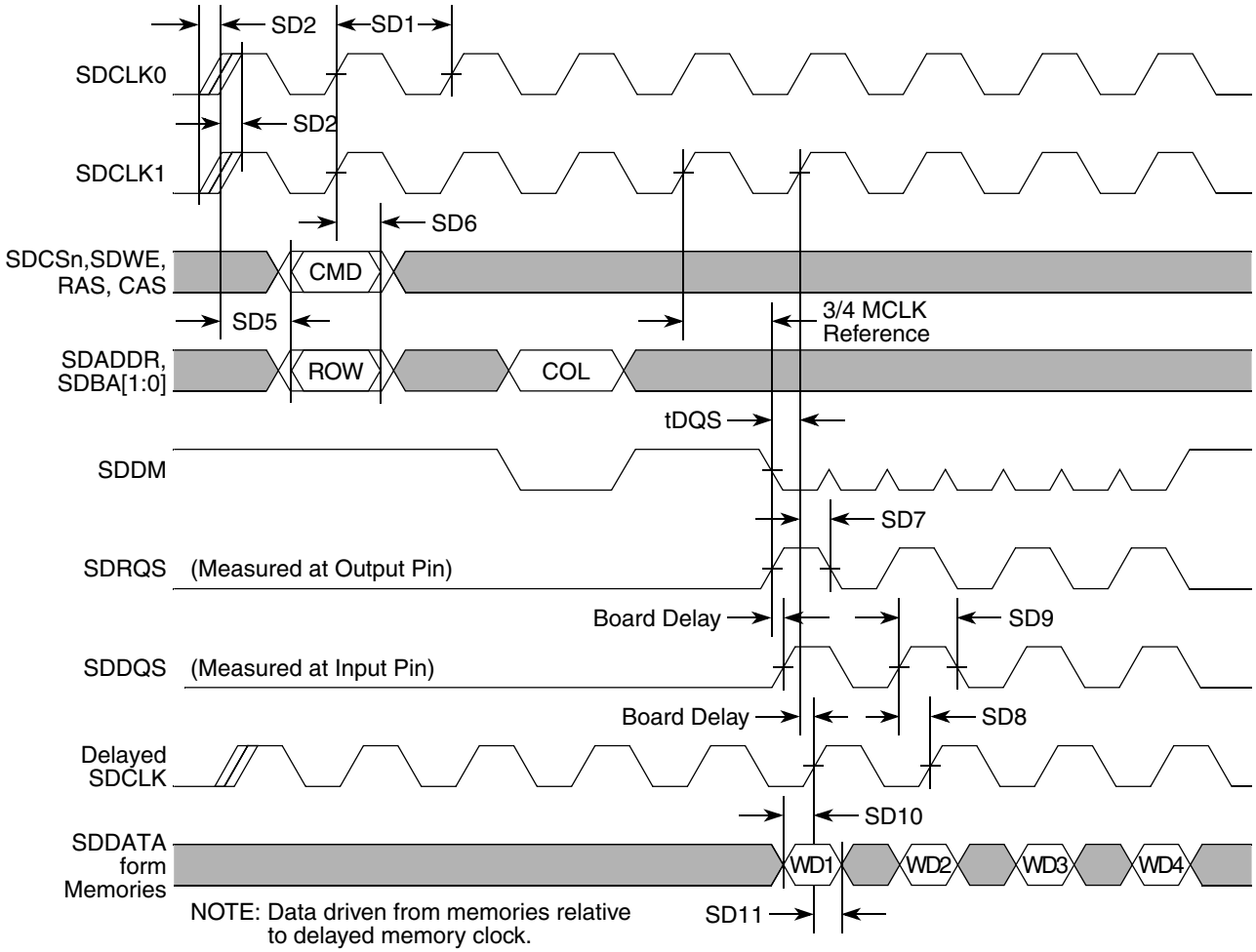


Figure 14. SDR Read Timing

Table 13. DDR Timing Specifications (continued)

Symbol	Characteristic	Min	Max	Unit	Notes
DD13	DQS input read preamble width (t_{RPRE})	0.9	1.1	SDCLK	
DD14	DQS input read postamble width (t_{RPST})	0.4	0.6	SDCLK	
DD15	DQS output write preamble width (t_{WPRE})	0.25	—	SDCLK	
DD16	DQS output write postamble width (t_{WPST})	0.4	0.6	SDCLK	

1 DDR memories typically have a minimum speed specification of 83 MHz. Check memory component specifications to verify.

2 The frequency of operation is 2x or 4x the CLKIN frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF548x Reference Manual*.

3 SDCLK is one memory clock in (ns).

4 Pulse width high plus pulse width low cannot exceed max clock period.

5 Pulse width high plus pulse width low cannot exceed max clock period.

6 Command output valid should be 1/2 the memory bus clock (SDCLK) plus some minor adjustments for process, temperature, and voltage variations.

7 This specification relates to the required input setup time of today’s DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

8 The first data beat is valid before the first rising edge of SDDQS and after the SDDQS write preamble. The remaining data beats is valid for each subsequent SDDQS edge.

9 This specification relates to the required hold time of today’s DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

10 Data input skew is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

11 Data input hold is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the first data line becomes invalid.

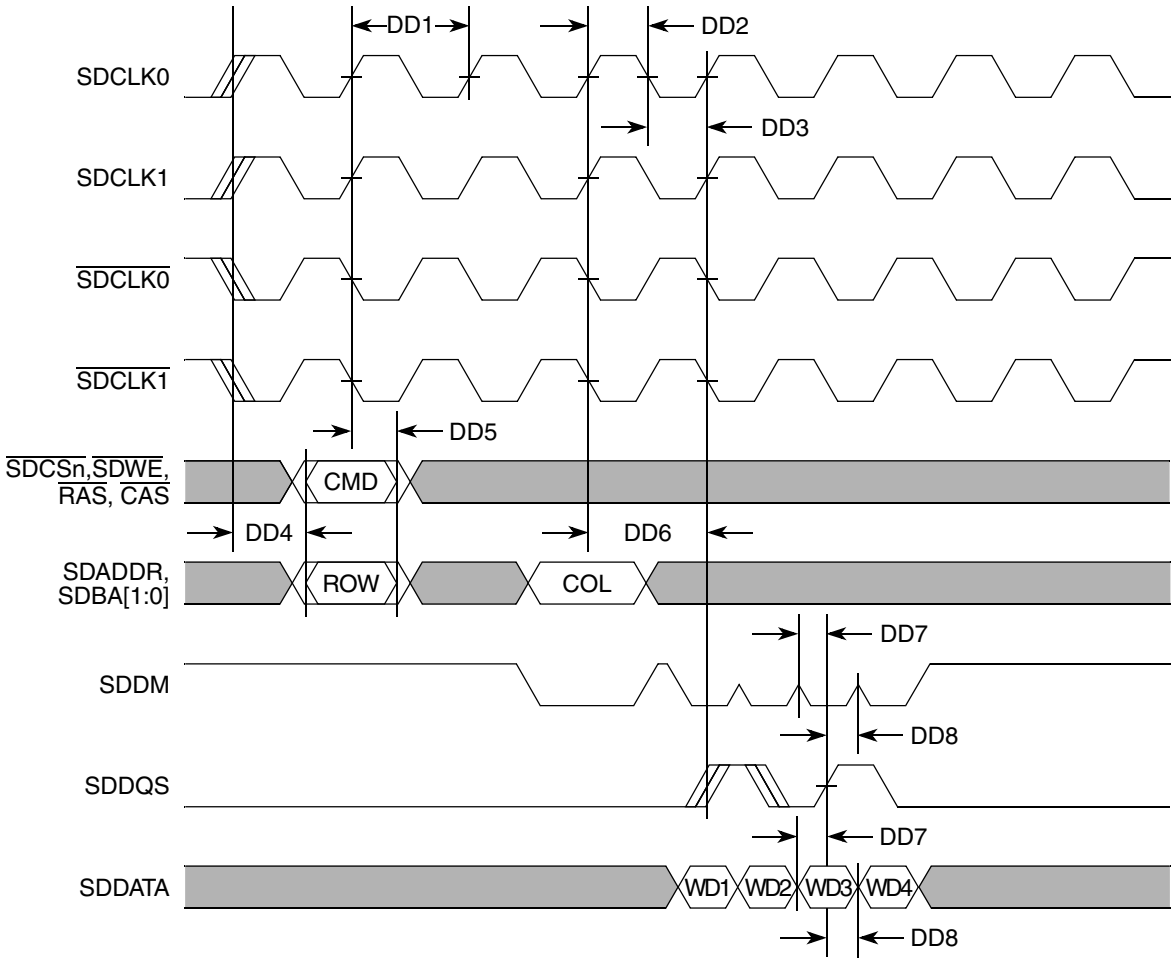


Figure 16. DDR Write Timing

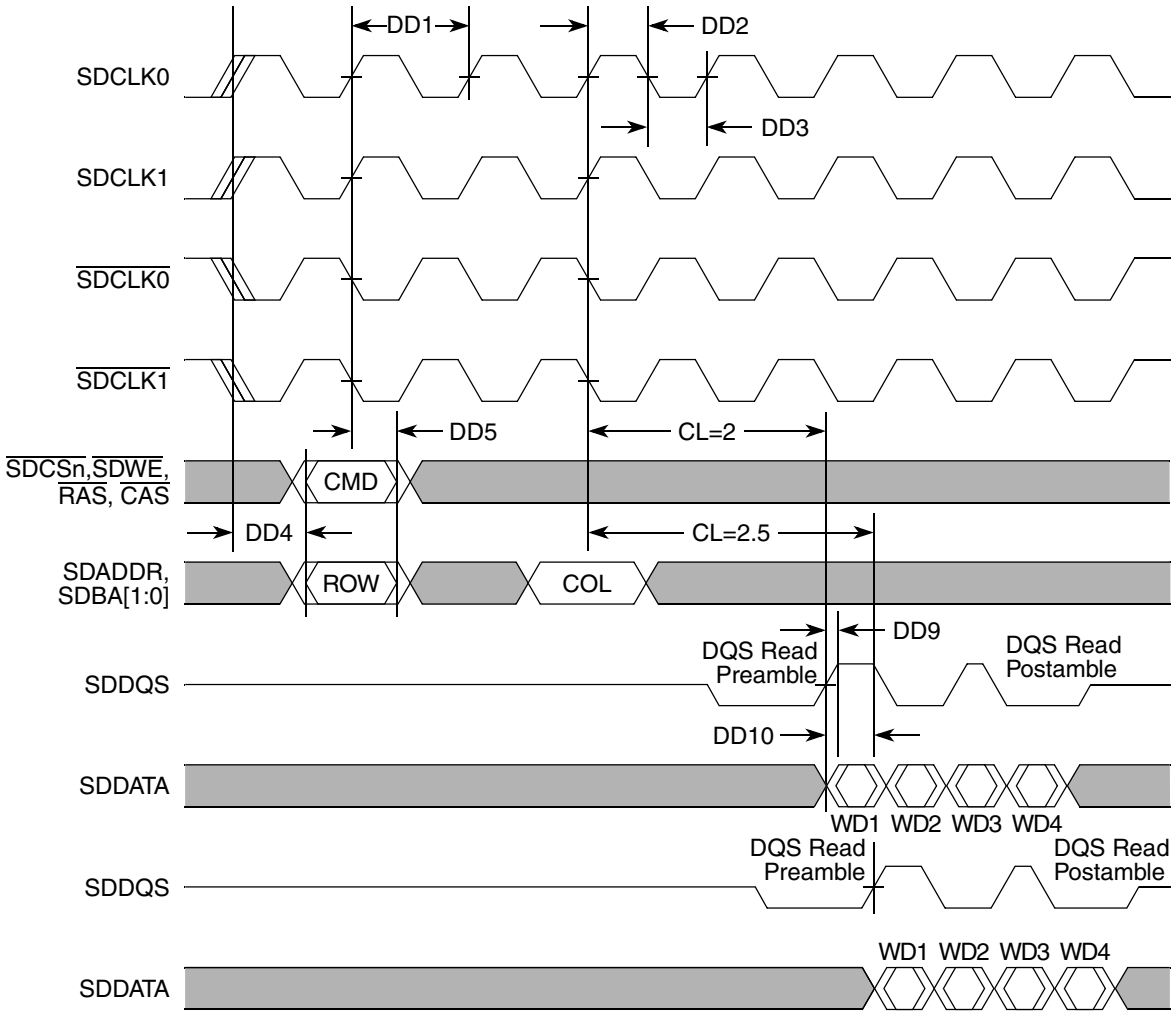


Figure 17. DDR Read Timing

10 PCI Bus

The PCI bus on the MCF548*x* is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	50	MHz	1
P1	Clock Period (t_{CK})	20	40	ns	2
P2	Address, Data, and Command (33< PCI ≤ 50 Mhz)—Input Setup (t_{IS})	3.0	—	ns	
P3	Address, Data, and Command (0 < PCI ≤ 33 Mhz)—Input Setup (t_{IS})	7.0	—	ns	
P4	Address, Data, and Command (33–50 Mhz)—Output Valid (t_{DV})	—	6.0	ns	3
P5	Address, Data, and Command (0–33 Mhz) - Output Valid (t_{DV})	—	11.0	ns	
P6	PCI signals (0–50 Mhz) - Output Hold (t_{DH})	0	—	ns	4

Table 15. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
M2	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

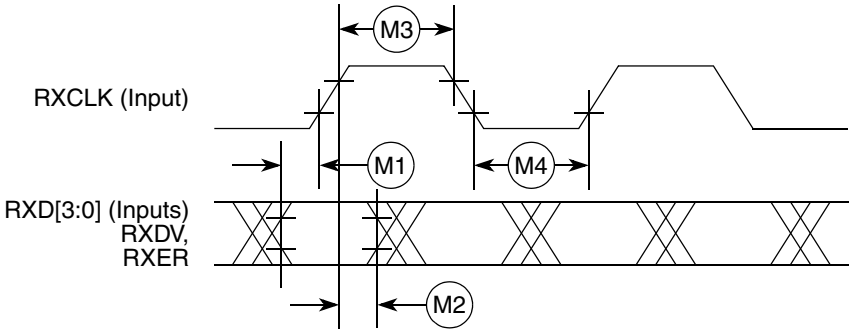


Figure 19. MII Receive Signal Timing Diagram

11.2 MII Transmit Signal Timing

Table 16. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	TXCLK to TXD[3:0], TXEN, TXER invalid	0	—	ns
M6	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

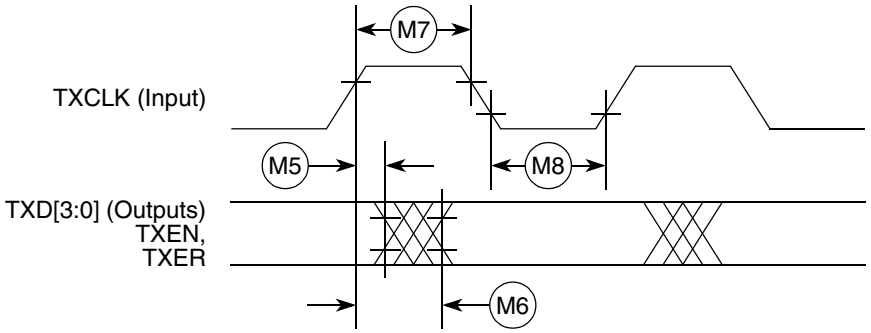


Figure 20. MII Transmit Signal Timing Diagram

11.3 MII Async Inputs Signal Timing (CRS, COL)

Table 17. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

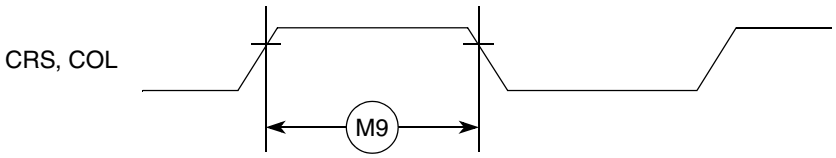


Figure 21. MII Async Inputs Timing Diagram

11.4 MII Serial Management Channel Timing (MDIO,MDC)

Table 18. MII Serial Management Channel Signal Timing

Num	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (min prop delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

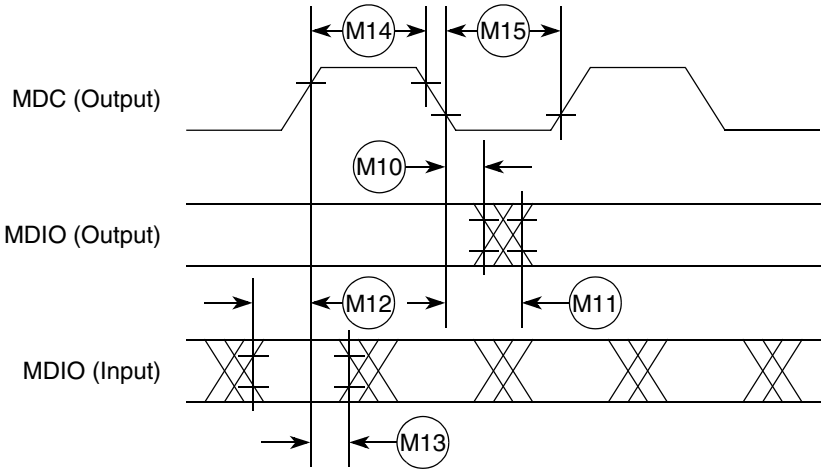


Figure 22. MII Serial Management Channel TIming Diagram

12 General Timing Specifications

Table 19 lists timing specifications for the GPIO, PSC, FlexCAN, $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and external interrupts.

Table 19. General AC Timing Specifications

Name	Characteristic	Min	Max	Unit
G1	CLKIN high to signal output valid	—	2	PSTCLK
G2	CLKIN high to signal invalid (output hold)	0	—	ns
G3	Signal input pulse width	2	—	PSTCLK

13 I^2C Input/Output Timing Specifications

Table 20 lists specifications for the I^2C input timing parameters shown in Figure 23.

Table 20. I^2C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	Bus clocks
I2	Clock low period	8	—	Bus clocks
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	mS
I6	Clock high time	4	—	Bus clocks
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	Bus clocks
I9	Stop condition setup time	2	—	Bus clocks

Table 21 lists specifications for the I^2C output timing parameters shown in Figure 23.

Table 21. I^2C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	Bus clocks
I2[1]	Clock low period	10	—	Bus clocks
I3[2]	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	μS
I4[1]	Data hold time	7	—	Bus clocks
I5[3]	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	10	—	Bus clocks
I7[1]	Data setup time	2	—	Bus clocks
I8[1]	Start condition setup time (for repeated start condition only)	20	—	Bus clocks
I9[1]	Stop condition setup time	10	—	Bus clocks

Table 23 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 23. Debug AC Timing Specifications

Num	Characteristic	50 MHz		Units
		Min	Max	
D1	PSTDDATA to PSTCLK setup	4.5	—	ns
D2	PSTCLK to PSTDDATA hold	4.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLKs
D4 [1]	DSCLK-to-DSO hold	4	—	PSTCLKs
D5	DSCLK cycle time	5	—	PSTCLKs

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 23.

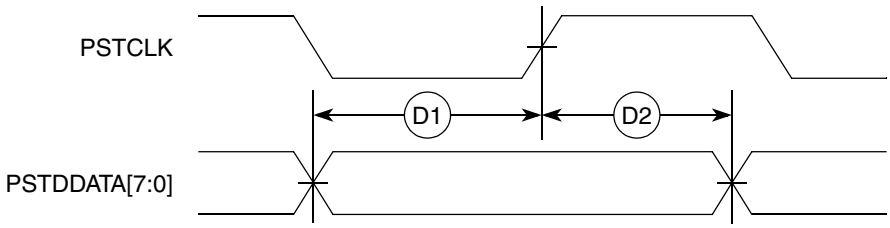


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 23.

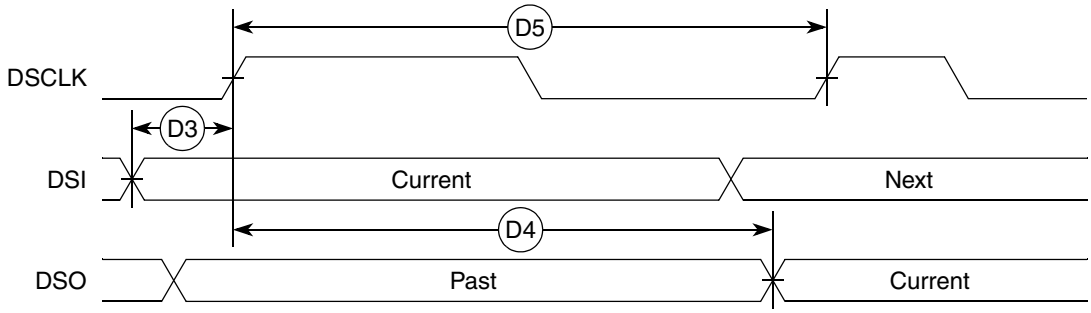


Figure 29. BDM Serial Port AC Timing

15 DSPI Electrical Specifications

Table 24 lists DSPI timings.

Table 24. DSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
DS1	DSPI_CS[3:0] to DSPI_CLK	1 × tck	510 × tck	ns
DS2	DSPI_CLK high to DSPI_DOUT valid.	—	12	ns
DS3	DSPI_CLK high to DSPI_DOUT invalid. (Output hold)	2	—	ns
DS4	DSPI_DIN to DSPI_CLK (Input setup)	10	—	ns
DS5	DSPI_DIN to DSPI_CLK (Input hold)	10	—	ns

The values in Table 24 correspond to Figure 30.

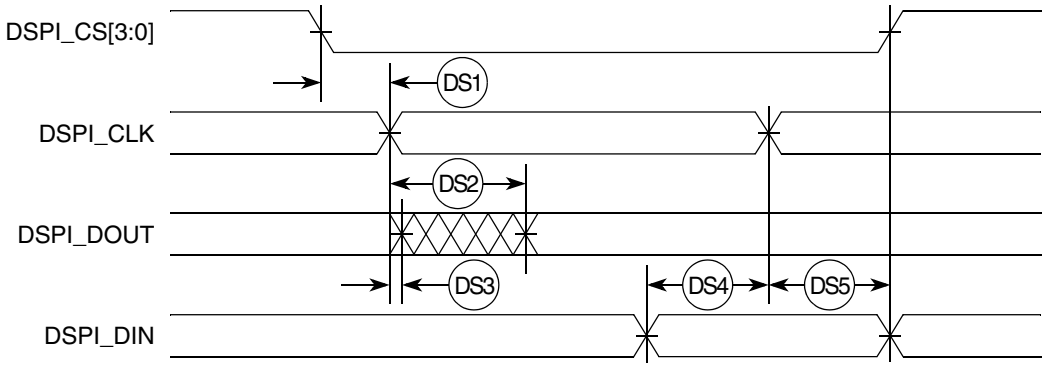


Figure 30. DSPI Timing

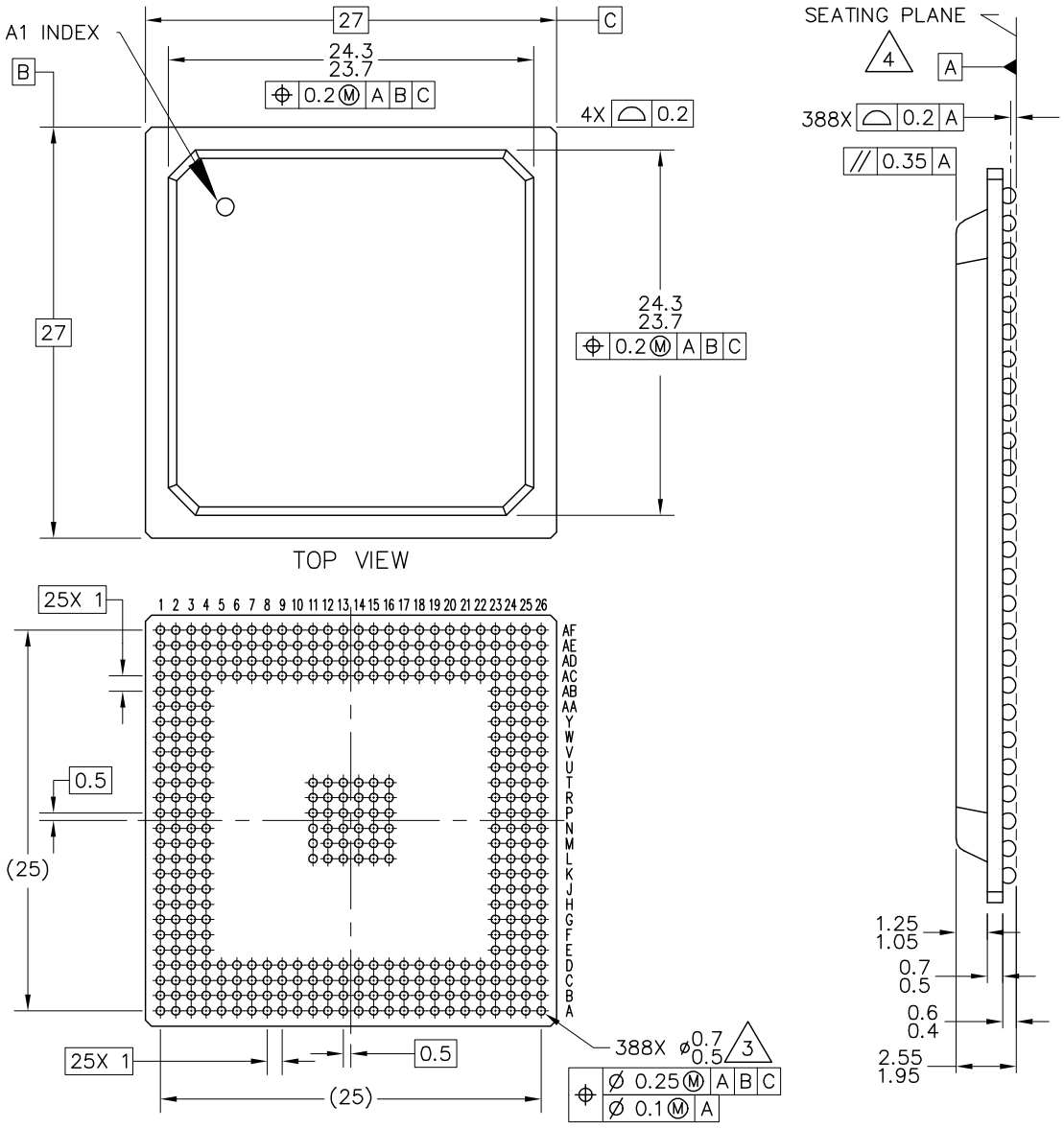
16 Timer Module AC Timing Specifications

Table 25 lists timer module AC timings.

Table 25. Timer Module AC Timing Specifications

Name	Characteristic	0–50 MHz		Unit
		Min	Max	
T1	TIN0 / TIN1 / TIN2 / TIN3 cycle time	3	—	PSTCLK
T2	TIN0 / TIN1 / TIN2 / TIN3 pulse width	1	—	PSTCLK

17 Case Drawing



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARS23880W	REV: C
388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1164–02	25 JAN 2007
	STANDARD: JEDEC MS–034 AAL–1	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES:
   5254 – 2 LAYER SUBSTRATE PACKAGE
   5367 – 4 LAYER SUBSTRATE PACKAGE

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	CASE NUMBER: 1164–02	25 JAN 2007
	STANDARD: JEDEC MS–034 AAL–1	

Figure 31. 388-pin BGA Case Outline

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