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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	Coldfire V4E
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	99
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5484czp200">https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5484czp200</a>

# 1 Maximum Ratings

Table 1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

**Table 1. Absolute Maximum Ratings**

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	$EV_{DD}$	−0.3 to +4.0	V
Internal logic supply voltage	$IV_{DD}$	−0.5 to +2.0	V
Memory (I/O pads) supply voltage (2.5-V power pins)	$SD V_{DD}$	−0.3 to +4.0 SDR Memory −0.3 to +2.8 DDR Memory	V
PLL supply voltage	$PLL V_{DD}$	−0.5 to +2.0	V
Internal logic supply voltage, input voltage level	$V_{in}$	−0.5 to +3.6	V
Storage temperature range	$T_{stg}$	−55 to +150	°C

## 2 Thermal Characteristics

### 2.1 Operating Temperatures

Table 2 lists junction and ambient operating temperatures.

**Table 2. Operating Temperatures**

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	$T_j$	105	°C
Maximum operating ambient temperature	$T_{Amax}$	<85 <sup>1</sup>	°C
Minimum operating ambient temperature	$T_{Amin}$	−40	°C

<sup>1</sup> This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

## 2.2 Thermal Resistance

Table 3 lists thermal resistance values.

**Table 3. Thermal Resistance**

Characteristic		Symbol	Value	Unit
324 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JA}$	20–22 <sup>1,2</sup>	°CW
388 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JA}$	19 <sup>1,2</sup>	°CW
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$\theta_{JA}$	16 <sup>1,2</sup>	°CW
Junction to board	—	$\theta_{JB}$	11 <sup>3</sup>	°CW
Junction to case	—	$\theta_{JC}$	7 <sup>4</sup>	°CW
Junction to top of package	Natural convection	$\Psi_{jt}$	2 <sup>1,5</sup>	°CW

<sup>1</sup>  $\theta_{JA}$  and  $\Psi_{jt}$  parameters are simulated in accordance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

<sup>2</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>3</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>4</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>5</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 3 DC Electrical Specifications

Table 4 lists DC electrical operating temperatures. This table is based on an operating voltage of  $EV_{DD} = 3.3 V_{DC} \pm 0.3 V_{DC}$  and  $IV_{DD}$  of  $1.5 \pm 0.07 V_{DC}$ .

**Table 4. DC Electrical Specifications**

Characteristic	Symbol	Min	Max	Units
External (I/O pads) operation voltage range	$EV_{DD}$	3.0	3.6	V
Memory (I/O pads) operation voltage range (DDR Memory)	$SD V_{DD}$	2.30	2.70	V
Internal logic operation voltage range <sup>1</sup>	$IV_{DD}$	1.43	1.58	V
PLL Analog operation voltage range <sup>1</sup>	$PLL V_{DD}$	1.43	1.58	V
USB oscillator operation voltage range	$USB\_OSV_{DD}$	3.0	3.6	V
USB digital logic operation voltage range	$USBV_{DD}$	3.0	3.6	V
USB PHY operation voltage range	$USB\_PHYV_{DD}$	3.0	3.6	V
USB oscillator analog operation voltage range	$USB\_OSCAV_{DD}$	1.43	1.58	V

Table 4. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Units
USB PLL operation voltage range	USB_PLLV <sub>DD</sub>	1.43	1.58	V
Input high voltage SSTL 3.3V/2.5V <sup>2</sup>	V <sub>IH</sub>	V <sub>REF</sub> + 0.3	SD V <sub>DD</sub> + 0.3	V
Input low voltage SSTL 3.3V/2.5V <sup>2</sup>	V <sub>IL</sub>	V <sub>SS</sub> - 0.3	V <sub>REF</sub> - 0.3	V
Input high voltage 3.3V I/O pins	V <sub>IH</sub>	0.7 x EV <sub>DD</sub>	EV <sub>DD</sub> + 0.3	V
Input low voltage 3.3V I/O pins	V <sub>IL</sub>	V <sub>SS</sub> - 0.3	0.35 x EV <sub>DD</sub>	V
Output high voltage I <sub>OH</sub> = 8 mA, 16 mA, 24 mA	V <sub>OH</sub>	2.4	—	V
Output low voltage I <sub>OL</sub> = 8 mA, 16 mA, 24 mA <sup>5</sup>	V <sub>OL</sub>	—	0.5	V
Capacitance <sup>3</sup> , V <sub>in</sub> = 0 V, f = 1 MHz	C <sub>IN</sub>	—	TBD	pF
Input leakage current	I <sub>in</sub>	-1.0	1.0	μA

<sup>1</sup> IV<sub>DD</sub> and PLL V<sub>DD</sub> should be at the same voltage. PLL V<sub>DD</sub> should have a filtered input. Please see Figure 2 for an example circuit. There are three PLL V<sub>DD</sub> inputs. A filter circuit should be used on each PLL V<sub>DD</sub> input.

<sup>2</sup> This specification is guaranteed by design and is not 100% tested.

<sup>3</sup> Capacitance C<sub>IN</sub> is periodically sampled rather than 100% tested.

## 4 Hardware Design Considerations

### 4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V<sub>DD</sub> pins. The filter shown in Figure 2 should be connected between the board V<sub>DD</sub> and the PLL V<sub>DD</sub> pins. The resistor and capacitors should be placed as close to the dedicated PLL V<sub>DD</sub> pin as possible.

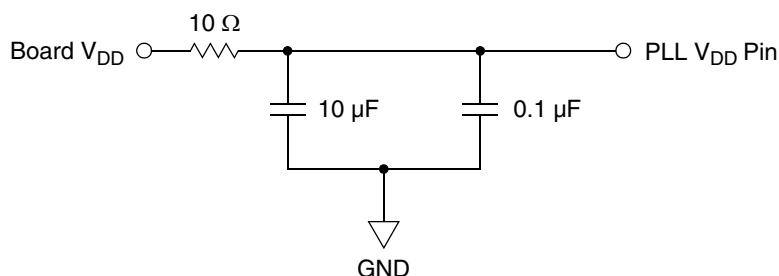
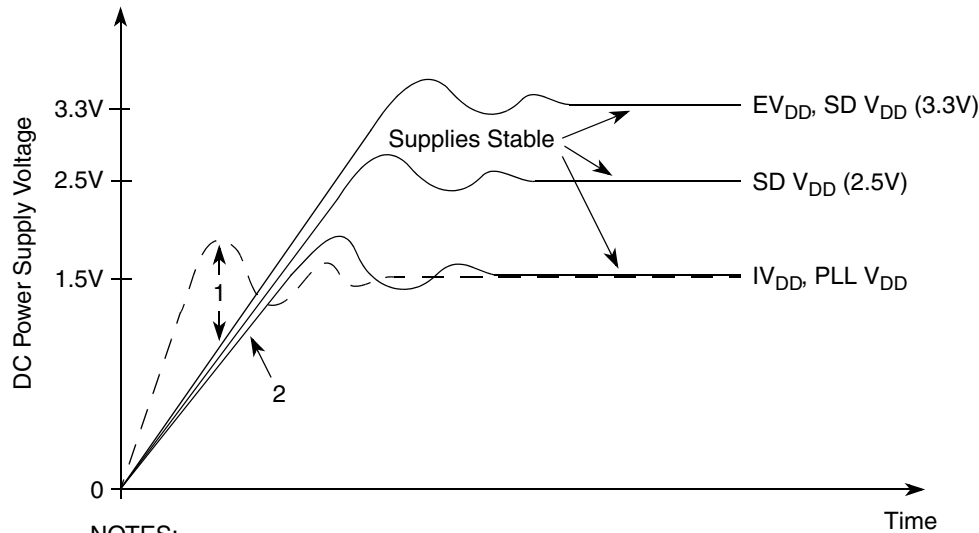


Figure 2. System PLL V<sub>DD</sub> Power Filter

### 4.2 Supply Voltage Sequencing and Separation Cautions

Figure 3 shows situations in sequencing the I/O V<sub>DD</sub> (EV<sub>DD</sub>), SDRAM V<sub>DD</sub> (SD V<sub>DD</sub>), PLL V<sub>DD</sub> (PLL V<sub>DD</sub>), and Core V<sub>DD</sub> (IV<sub>DD</sub>).



#### NOTES:

1. IVDD should not exceed EVDD or SD VDD by more than 0.4V at any time, including power-up.
2. Recommended that IVDD/PLL VDD should track EVDD/SD VDD up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EVDD, SD VDD, IVDD, or PLL VDD) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

**Figure 3. Supply Voltage Sequencing and Separation Cautions**

The relationship between SD VDD and EVDD is non-critical during power-up and power-down sequences. SD VDD (2.5V or 3.3V) and EVDD are specified relative to IVDD.

## 4.2.1 Power Up Sequence

If EVDD/SD VDD are powered up with the IVDD at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the EVDD/SD VDD to be in a high impedance state. There is no limit to how long after EVDD/SD VDD powers up before IVDD must power up. IVDD should not lead the EVDD, SD VDD, or PLL VDD by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IVDD/PLL VDD and EVDD/SD VDD should track up to 0.9V, then separate for the completion of ramps with EVDD/SD VDD going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

## 4.2.2 Power Down Sequence

If IVDD/PLL VDD are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IVDD and PLL VDD power down before EVDD or SD VDD must power down. IVDD should not lag EVDD, SD VDD, or PLL VDD going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IVDD/PLL VDD to 0V
2. Drop EVDD/SD VDD supplies

## 4.3 General USB Layout Guidelines

### 4.3.1 USB D+ and D- High-Speed Traces

1. High speed clock and the USBD+ and USBD- differential pair should be routed first.
2. Route USBD+ and USBD- signals on the top layer of the board.
3. The trace width and spacing of the USBD+ and USBD- signals should be such that the differential impedance is  $90\Omega$ .
4. Route traces over continuous planes (power and ground)—they should not pass over any power/ground plane slots or anti-etch. When placing connectors, make sure the ground plane clear-outs around each pin have ground continuity between all pins.
5. Maintain the parallelism (skew matched) between USBD+ and USBD-. These traces should be the same overall length.
6. Do not route USBD+ and USBD- traces under oscillators or parallel to clock traces and/or data buses. Minimize the lengths of high speed signals that run parallel to the USBD+ and USBD- pair. Maintain a minimum 50mil spacing to clock signals.
7. Keep USBD+ and USBD- traces as short as possible.
8. Route USBD+, USBD-, and USBVBUS signals with a minimum amount of vias and corners. Use  $45^\circ$  turns.
9. Stubs should be avoided as much as possible. If they cannot be avoided, stubs should be no greater than 200mils.

### 4.3.2 USB VBUS Traces

Connecting the USBVBUS pin directly to the 5V VBUS signal from the USB connector can cause long-term reliability problems in the ESD network of the processor. Therefore, use of an external voltage divider for VBUS is recommended. [Figure 4](#) and [Figure 5](#) depict possible connections for VBUS. Point A, marked in each figure, is where a 5V version of VBUS should connect. Point B, marked in each figure, is where a 3.3V version of VBUS should connect to the USBVBUS pin on the device.

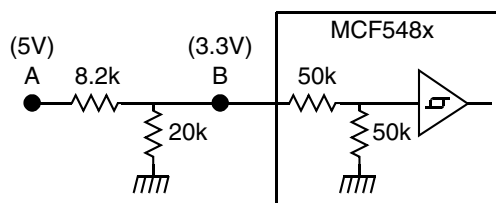


Figure 4. Preferred VBUS Connections

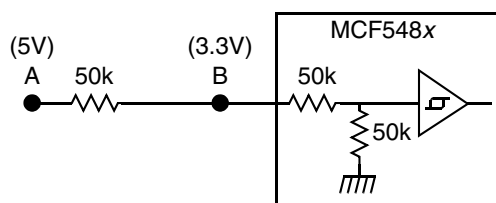


Figure 5. Alternate VBUS Connections

### 4.3.3 USB Receptacle Connections

It is recommended to connect the shield and the ground pin of the B USB receptacle for upstream ports to the board ground plane. The ground pin of the A USB receptacles for downstream ports should also be connected to the board ground plane, but industry practice varies widely on the connection of the shield of the A USB receptacles to other system grounds. Take precautions for control of ground loops between hosts and self-powered USB devices through the cable shield.

# 6 PLL Timing Specifications

The specifications in Table 7 are for the CLKIN pin.

Table 7. Clock Timing Specifications

Num	Characteristic	Min	Max	Units
C1	Cycle time	20	40	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

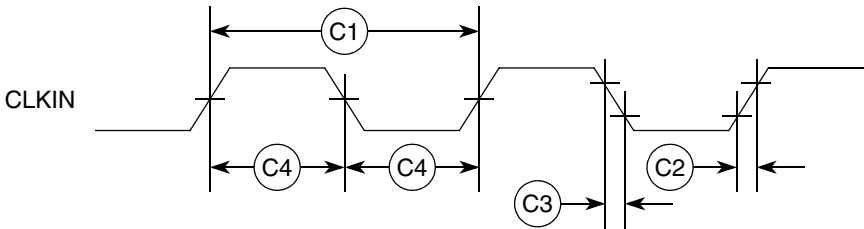


Figure 8. Input Clock Timing Diagram

Table 8 shows the supported PLL encodings.

Table 8. MCF548x Divide Ratio Encodings

AD[12:8] <sup>1</sup>	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.67–50.0	83.33–100	166.66–200
00101	1:2	25.0–41.67	50.0–83.33 <sup>2</sup>	100.0–166.66
01111	1:4	25.0	100	200

<sup>1</sup> All other values of AD[12:8] are reserved.  
<sup>2</sup> DDR memories typically have a minimum speed of 83 MHz. Some vendors specify down to 75 MHz. Check with the memory component specifications to verify.

Figure 9 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

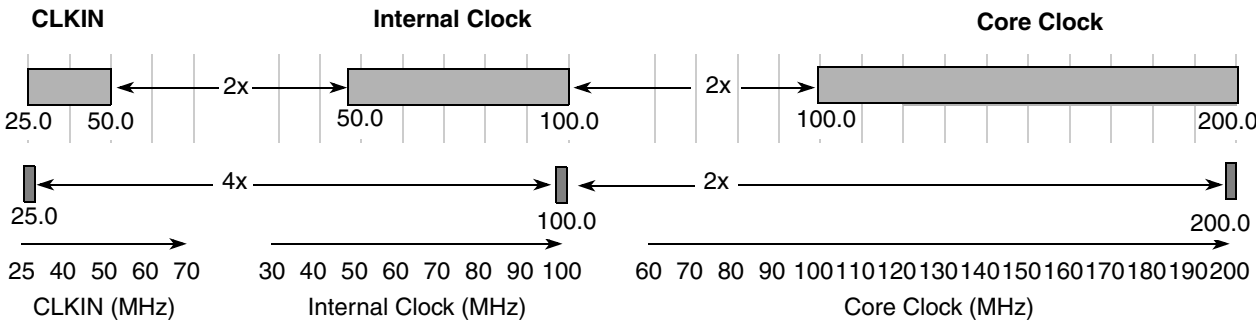


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

## 7 Reset Timing Specifications

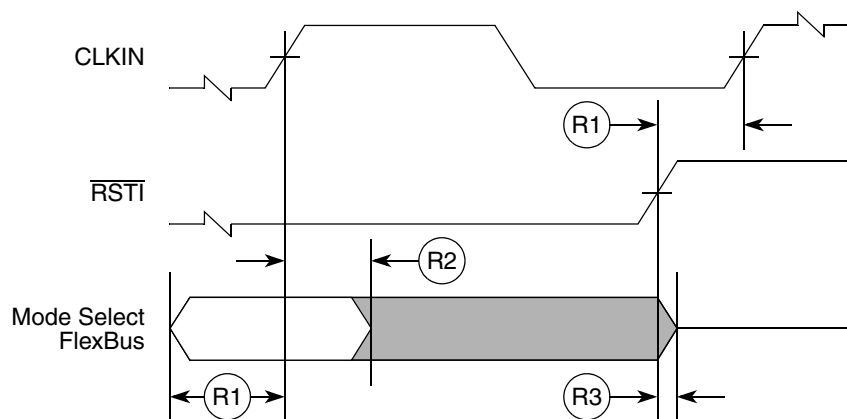
Table 9 lists specifications for the reset timing parameters shown in Figure 10

Table 9. Reset Timing Specifications

Num	Characteristic	50 MHz CLKIN		Units
		Min	Max	
R1 <sup>1</sup>	Valid to CLKIN (setup)	8	—	ns
R2	CLKIN to invalid (hold)	1.0	—	ns
R3	$\overline{\text{RSTI}}$ to invalid (hold)	1.0	—	ns
	$\overline{\text{RSTI}}$ pulse duration	5	—	CLKIN cycles

<sup>1</sup>  $\overline{\text{RSTI}}$  and FlexBus data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 10 shows reset timing for the values in Table 9.



NOTE:

Mode selects are registered on the rising clock edge before the cycle in which  $\overline{\text{RSTI}}$  is recognized as being negated.

Figure 10. Reset Timing

## 8 FlexBus

A multi-function external bus interface called FlexBus is provided on the MCF5482 with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ( $\overline{\text{FBCS}}[5:0]$ ). Chip-select  $\overline{\text{FBCS0}}$  can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM / flash memories.



## 8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

**Table 10. FlexBus AC Timing Specifications**

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	50	Mhz	<sup>1</sup>
FB1	Clock Period (CLKIN)	20	40	ns	<sup>2</sup>
FB2	Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}[5:0]$ , R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\text{BWE}[3:0]$ , $\overline{\text{OE}}$ , and $\overline{\text{TBST}}$ )	—	7.0	ns	<sup>3</sup>
FB3	Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}[5:0]$ , R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\text{BWE}[3:0]$ , $\overline{\text{OE}}$ , and $\overline{\text{TBST}}$ )	1	—	ns	<sup>3, 4</sup>
FB4	Data Input Setup	3.5	—	ns	
FB5	Data Input Hold	0	—	ns	
FB6	Transfer Acknowledge ( $\overline{\text{TA}}$ ) Input Setup	4	—	ns	
FB7	Transfer Acknowledge ( $\overline{\text{TA}}$ ) Input Hold	0	—	ns	
FB8	Address Output Valid (PCIAD[31:0])	—	7.0	ns	<sup>5</sup>
FB9	Address Output Hold (PCIAD[31:0])	0	—	ns	<sup>5</sup>

<sup>1</sup> The frequency of operation is the same as the PCI frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI.

<sup>2</sup> Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

<sup>3</sup> Timing for chip selects only applies to the  $\overline{\text{FBCS}}[5:0]$  signals. Please see [Section 9.2, “DDR SDRAM AC Timing Characteristics”](#) for SDCS[3:0] timing.

<sup>4</sup> The FlexBus supports programming an extension of the address hold. Please consult the MCF548X specification manual for more information.

<sup>5</sup> These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

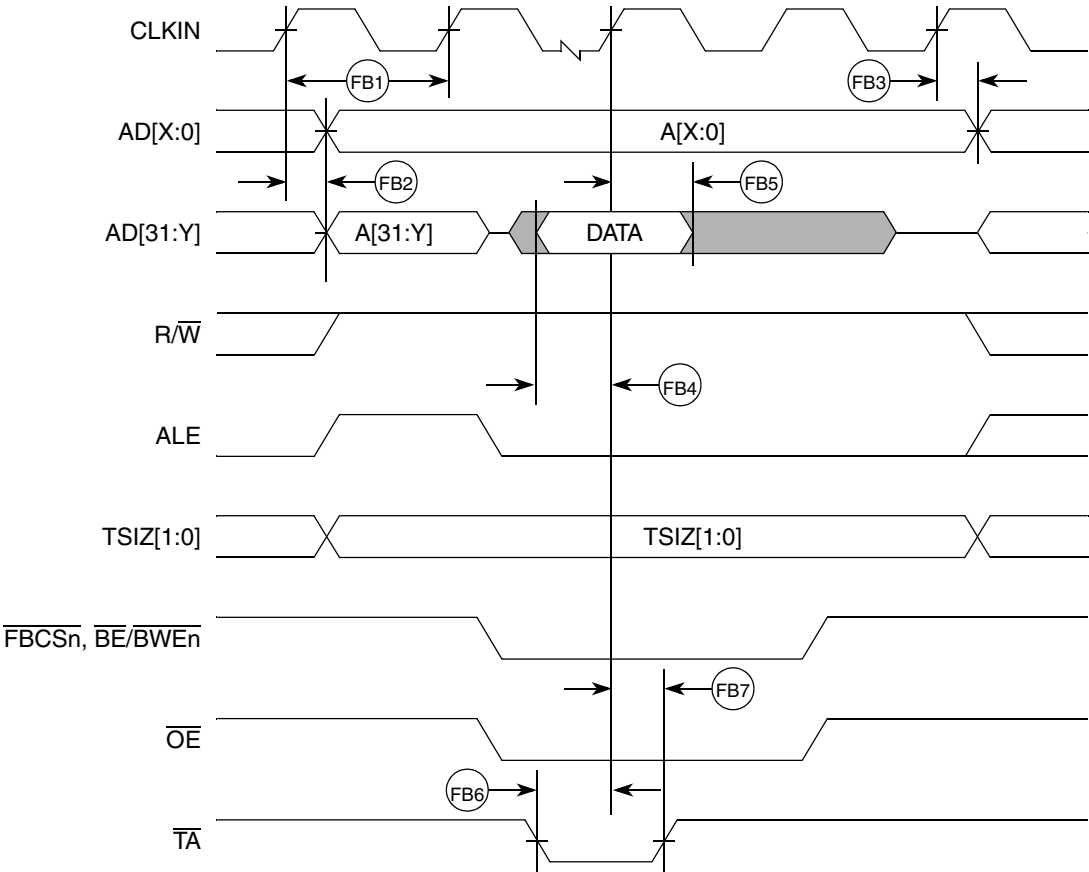


Figure 11. FlexBus Read Timing

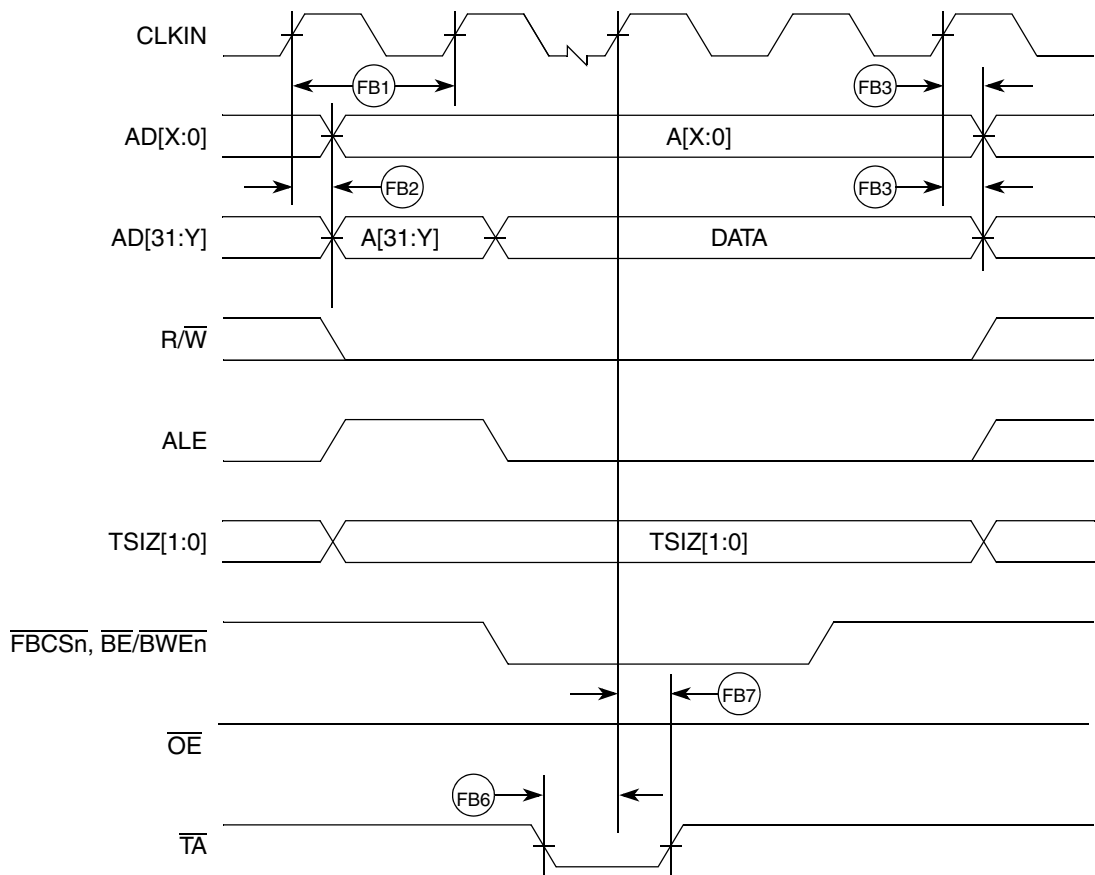


Figure 12. FlexBus Write Timing

# 9 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

## 9.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SDR\_DQS on read cycles. The MCF548x SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must be supplied to the MCF548x for each data beat of an SDR read. The MCF548x accomplishes this by asserting a signal called SDR\_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR\_DQS signal and its usage.

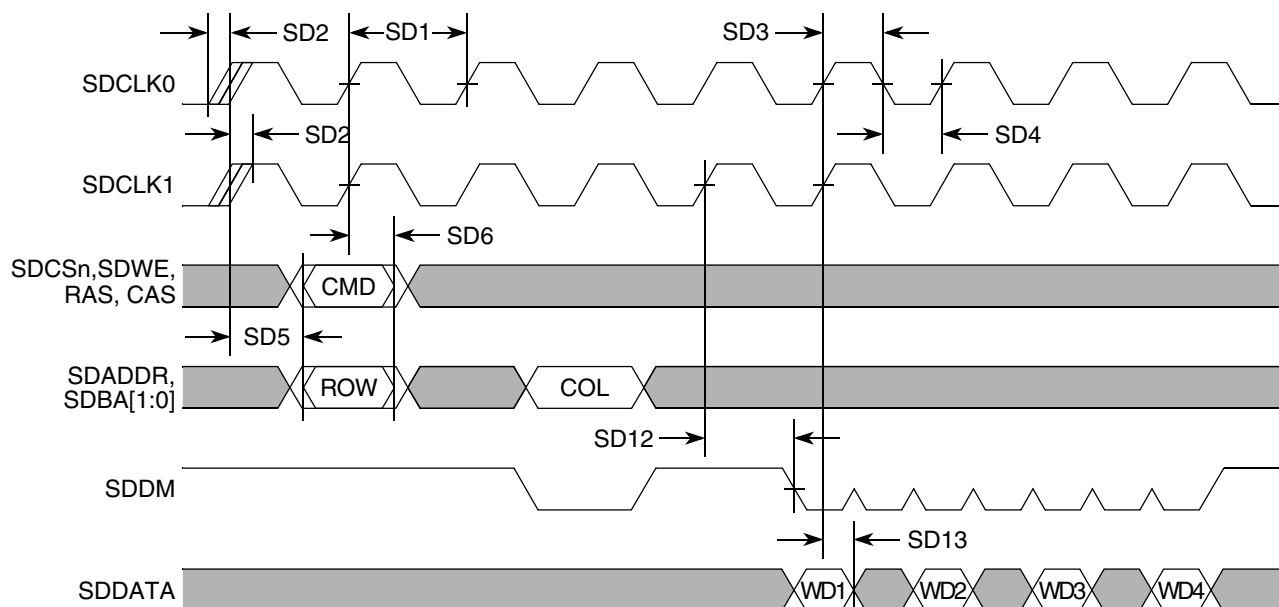


Figure 13. SDR Write Timing

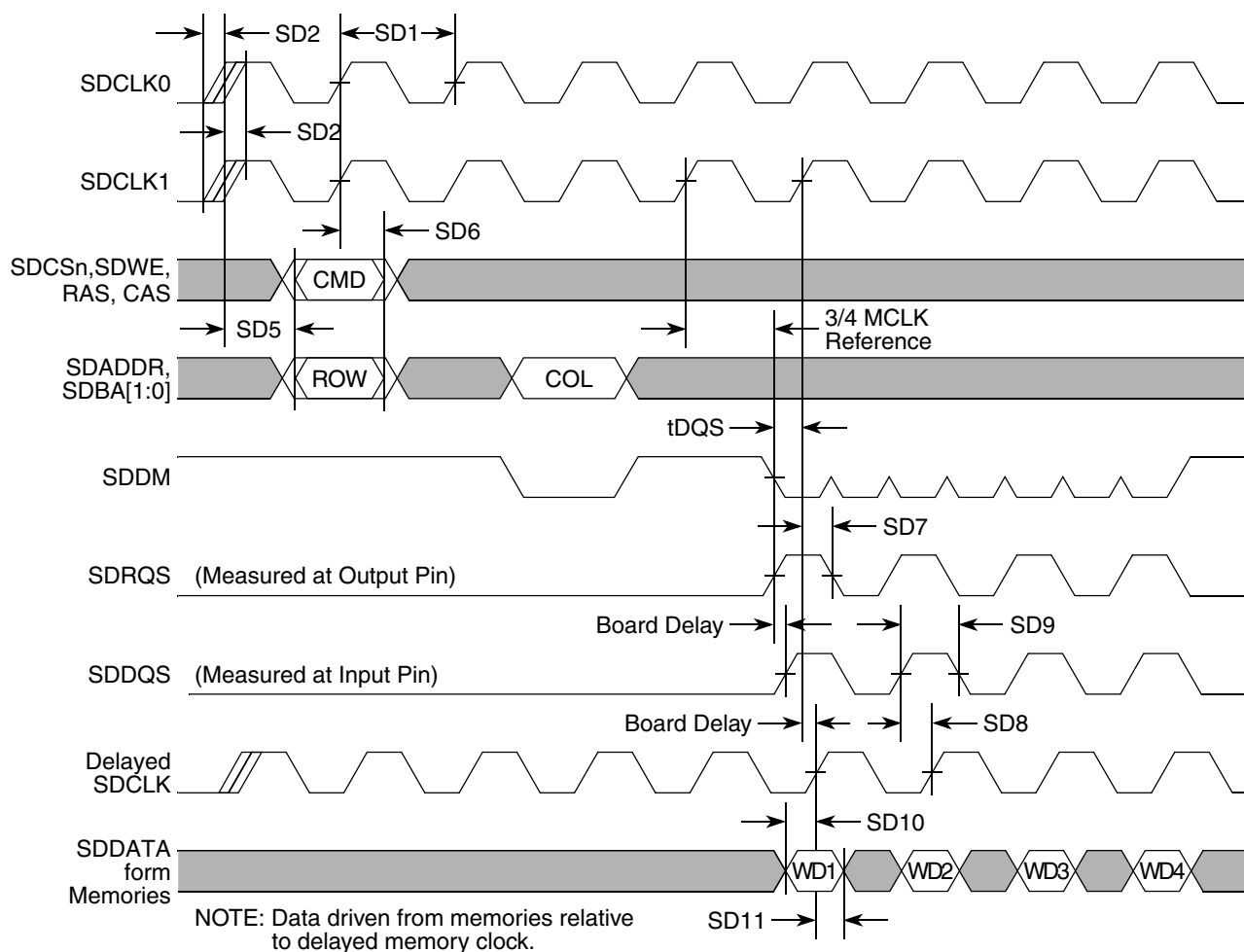


Figure 14. SDR Read Timing

Table 13. DDR Timing Specifications (continued)

Symbol	Characteristic	Min	Max	Unit	Notes
DD13	DQS input read preamble width ( $t_{RPRE}$ )	0.9	1.1	SDCLK	
DD14	DQS input read postamble width ( $t_{RPST}$ )	0.4	0.6	SDCLK	
DD15	DQS output write preamble width ( $t_{WPRE}$ )	0.25	—	SDCLK	
DD16	DQS output write postamble width ( $t_{WPST}$ )	0.4	0.6	SDCLK	

<sup>1</sup> DDR memories typically have a minimum speed specification of 83 MHz. Check memory component specifications to verify.

<sup>2</sup> The frequency of operation is 2x or 4x the CLKIN frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF548x Reference Manual*.

<sup>3</sup> SDCLK is one memory clock in (ns).

<sup>4</sup> Pulse width high plus pulse width low cannot exceed max clock period.

<sup>5</sup> Pulse width high plus pulse width low cannot exceed max clock period.

<sup>6</sup> Command output valid should be 1/2 the memory bus clock (SDCLK) plus some minor adjustments for process, temperature, and voltage variations.

<sup>7</sup> This specification relates to the required input setup time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

<sup>8</sup> The first data beat is valid before the first rising edge of SDDQS and after the SDDQS write preamble. The remaining data beats is valid for each subsequent SDDQS edge.

<sup>9</sup> This specification relates to the required hold time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

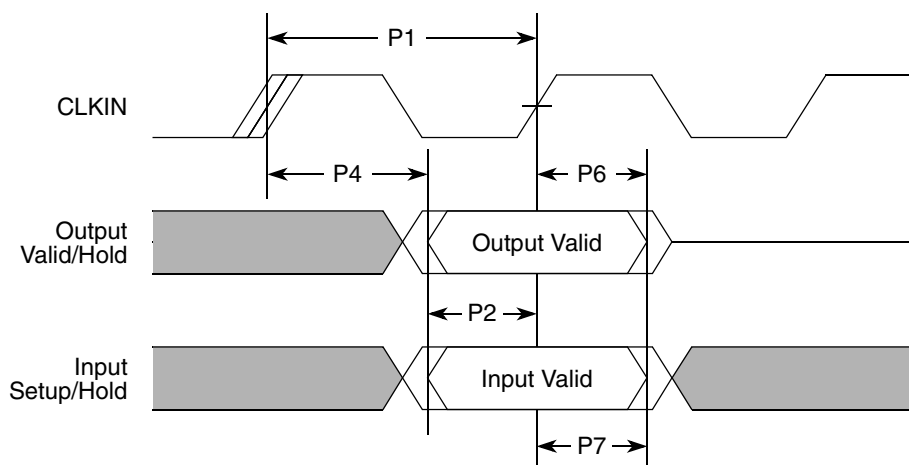
<sup>10</sup> Data input skew is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

<sup>11</sup> Data input hold is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the first data line becomes invalid.

**Table 14. PCI Timing Specifications (continued)**

Num	Characteristic	Min	Max	Unit	Notes
P7	PCI signals (0–50 Mhz) - Input Hold ( $t_{IH}$ )	0	—	ns	<sup>5</sup>
P8	PCI REQ/GNT (33 < PCI ≤ 50Mhz) - Output valid ( $t_{DV}$ )	—	6	ns	<sup>6</sup>
P9	PCI REQ/GNT (0 < PCI ≤ 33Mhz) - Output valid ( $t_{DV}$ )	—	12	ns	
P10	PCI REQ/GNT (33 < PCI ≤ 50Mhz) - Input Setup ( $t_{IS}$ )	—	5	ns	
P11	PCI REQ (0 < PCI ≤ 33Mhz) - Input Setup ( $t_{IS}$ )	12	—	ns	
P12	PCI GNT (0 < PCI ≤ 33Mhz) - Input Setup ( $t_{IS}$ )	10	—	ns	

- <sup>1</sup> Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF548x Reference Manual*. Also specific guidelines may need to be followed when operating the system PLL below certain frequencies.
- <sup>2</sup> Max cycle rate is determined by CLKIN and how the user has the system PLL configured.
- <sup>3</sup> All signals defined as PCI based signals. Does not include PTP (point-to-point) signals.
- <sup>4</sup> PCI 2.2 spec does not require an output hold time. Although the MCF548X may provide a slight amount of hold, it is not required or guaranteed.
- <sup>5</sup> PCI 2.2 spec requires zero input hold.
- <sup>6</sup> These signals are defined at PTP (Point-to-point) in the PCI 2.2 spec.



**Figure 18. PCI Timing**

## 11 Fast Ethernet AC Timing Specifications

### 11.1 MII/7-WIRE Interface Timing Specs

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the EMAC\_10\_100 I/O signals.

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices. If this interface is to be used with a specific transceiver device the timing specs may be altered to match that specific transceiver.

Table 15. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
M2	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

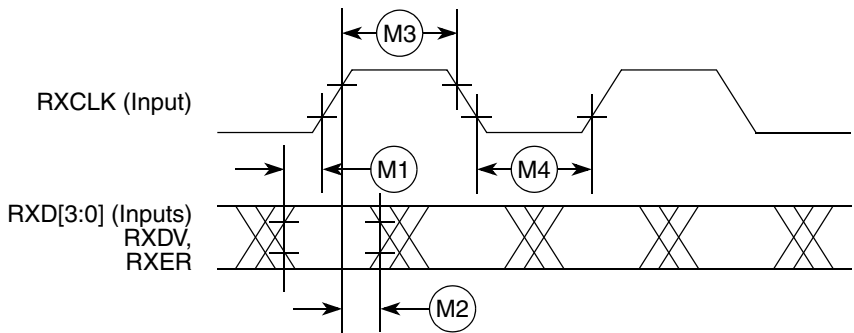


Figure 19. MII Receive Signal Timing Diagram

## 11.2 MII Transmit Signal Timing

Table 16. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	TXCLK to TXD[3:0], TXEN, TXER invalid	0	—	ns
M6	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

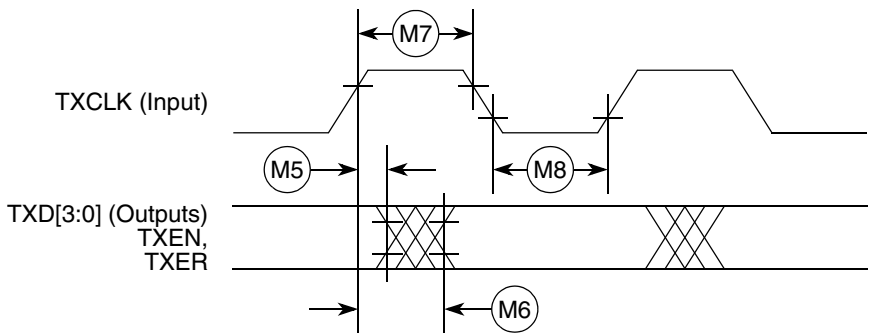


Figure 20. MII Transmit Signal Timing Diagram

## 12 General Timing Specifications

Table 19 lists timing specifications for the GPIO, PSC, FlexCAN,  $\overline{\text{DREQ}}$ ,  $\overline{\text{DACK}}$ , and external interrupts.

**Table 19. General AC Timing Specifications**

Name	Characteristic	Min	Max	Unit
G1	CLKIN high to signal output valid	—	2	PSTCLK
G2	CLKIN high to signal invalid (output hold)	0	—	ns
G3	Signal input pulse width	2	—	PSTCLK

## 13 I<sup>2</sup>C Input/Output Timing Specifications

Table 20 lists specifications for the I<sup>2</sup>C input timing parameters shown in Figure 23.

**Table 20. I<sup>2</sup>C Input Timing Specifications between SCL and SDA**

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	Bus clocks
I2	Clock low period	8	—	Bus clocks
I3	SCL/SDA rise time ( $V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$ )	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ( $V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$ )	—	1	mS
I6	Clock high time	4	—	Bus clocks
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	Bus clocks
I9	Stop condition setup time	2	—	Bus clocks

Table 21 lists specifications for the I<sup>2</sup>C output timing parameters shown in Figure 23.

**Table 21. I<sup>2</sup>C Output Timing Specifications between SCL and SDA**

Num	Characteristic	Min	Max	Units
I1 <sup>1</sup>	Start condition hold time	6	—	Bus clocks
I2 <sup>1</sup>	Clock low period	10	—	Bus clocks
I3 <sup>2</sup>	SCL/SDA rise time ( $V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$ )	—	—	$\mu\text{S}$
I4 <sup>1</sup>	Data hold time	7	—	Bus clocks
I5 <sup>3</sup>	SCL/SDA fall time ( $V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$ )	—	3	ns
I6 <sup>1</sup>	Clock high time	10	—	Bus clocks
I7 <sup>1</sup>	Data setup time	2	—	Bus clocks
I8 <sup>1</sup>	Start condition setup time (for repeated start condition only)	20	—	Bus clocks
I9 <sup>1</sup>	Stop condition setup time	10	—	Bus clocks



## JTAG and Boundary Scan Timing

- <sup>1</sup> Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 21. The I<sup>2</sup>C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 21 are minimum values.
- <sup>2</sup> Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- <sup>3</sup> Specified at a nominal 50-pF load.

Figure 23 shows timing for the values in Table 20 and Table 21.

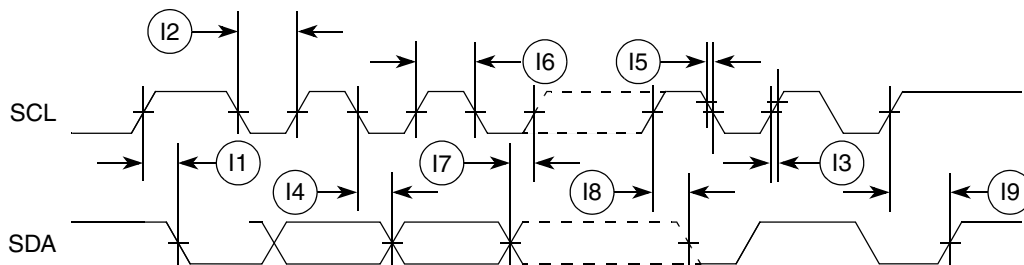


Figure 23. I<sup>2</sup>C Input/Output Timings

## 14 JTAG and Boundary Scan Timing

Table 22. JTAG and Boundary Scan Timing

Num	Characteristics <sup>1</sup>	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	$f_{JCYC}$	DC	10	MHz
J2	TCLK Cycle Period	$t_{JCYC}$	2	—	$t_{CK}$
J3	TCLK Clock Pulse Width	$t_{JCW}$	15.15	—	ns
J4	TCLK Rise and Fall Times	$t_{JCRF}$	0.0	3.0	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	$t_{BSDST}$	5.0	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	$t_{BSDHT}$	24.0	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	$t_{BSDV}$	0.0	15.0	ns
J8	TCLK Low to Boundary Scan Output High Z	$t_{BSDZ}$	0.0	15.0	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	$t_{TAPBST}$	5.0	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	$t_{TAPBHT}$	10.0	—	ns
J11	TCLK Low to TDO Data Valid	$t_{TDODV}$	0.0	20.0	ns
J12	TCLK Low to TDO High Z	$t_{TDODZ}$	0.0	15.0	ns
J13	$\overline{TRST}$ Assert Time	$t_{TRSTAT}$	100.0	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	$t_{TRSTST}$	10.0	—	ns

<sup>1</sup> MTMOD is expected to be a static signal. Hence, it is not associated with any timing

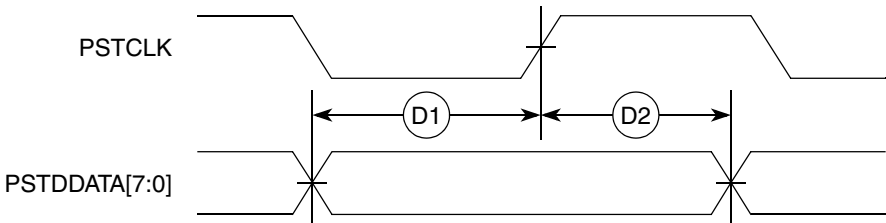
Table 23 lists specifications for the debug AC timing parameters shown in Figure 29.

**Table 23. Debug AC Timing Specifications**

Num	Characteristic	50 MHz		Units
		Min	Max	
D1	PSTDDATA to PSTCLK setup	4.5	—	ns
D2	PSTCLK to PSTDDATA hold	4.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLKs
D4 <sup>1</sup>	DSCLK-to-DSO hold	4	—	PSTCLKs
D5	DSCLK cycle time	5	—	PSTCLKs

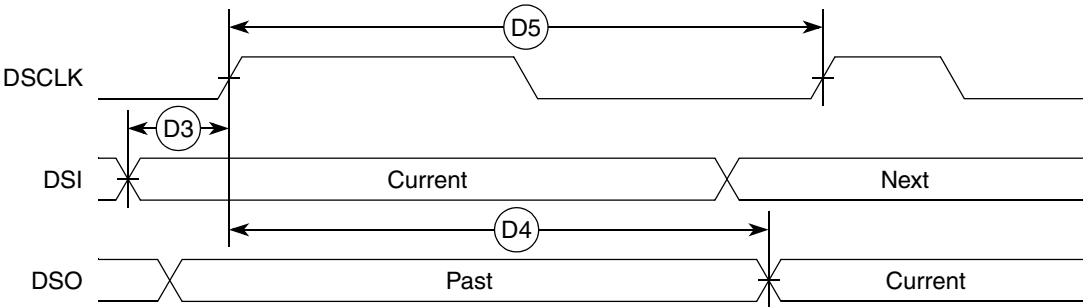
<sup>1</sup> DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 23.



**Figure 28. Real-Time Trace AC Timing**

Figure 29 shows BDM serial port AC timing for the values in Table 23.



**Figure 29. BDM Serial Port AC Timing**

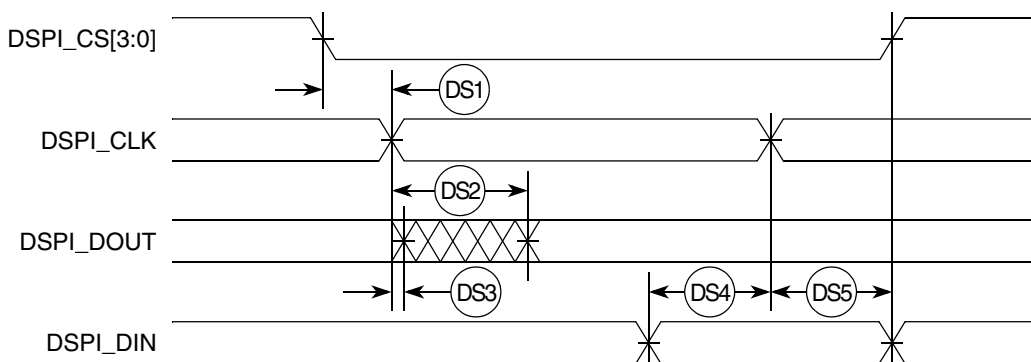
# 15 DSPI Electrical Specifications

Table 24 lists DSPI timings.

**Table 24. DSPI Modules AC Timing Specifications**

Name	Characteristic	Min	Max	Unit
DS1	DSPI_CS[3:0] to DSPI_CLK	$1 \times t_{ck}$	$510 \times t_{ck}$	ns
DS2	DSPI_CLK high to DSPI_DOUT valid.	—	12	ns
DS3	DSPI_CLK high to DSPI_DOUT invalid. (Output hold)	2	—	ns
DS4	DSPI_DIN to DSPI_CLK (Input setup)	10	—	ns
DS5	DSPI_DIN to DSPI_CLK (Input hold)	10	—	ns

The values in Table 24 correspond to Figure 30.



**Figure 30. DSPI Timing**

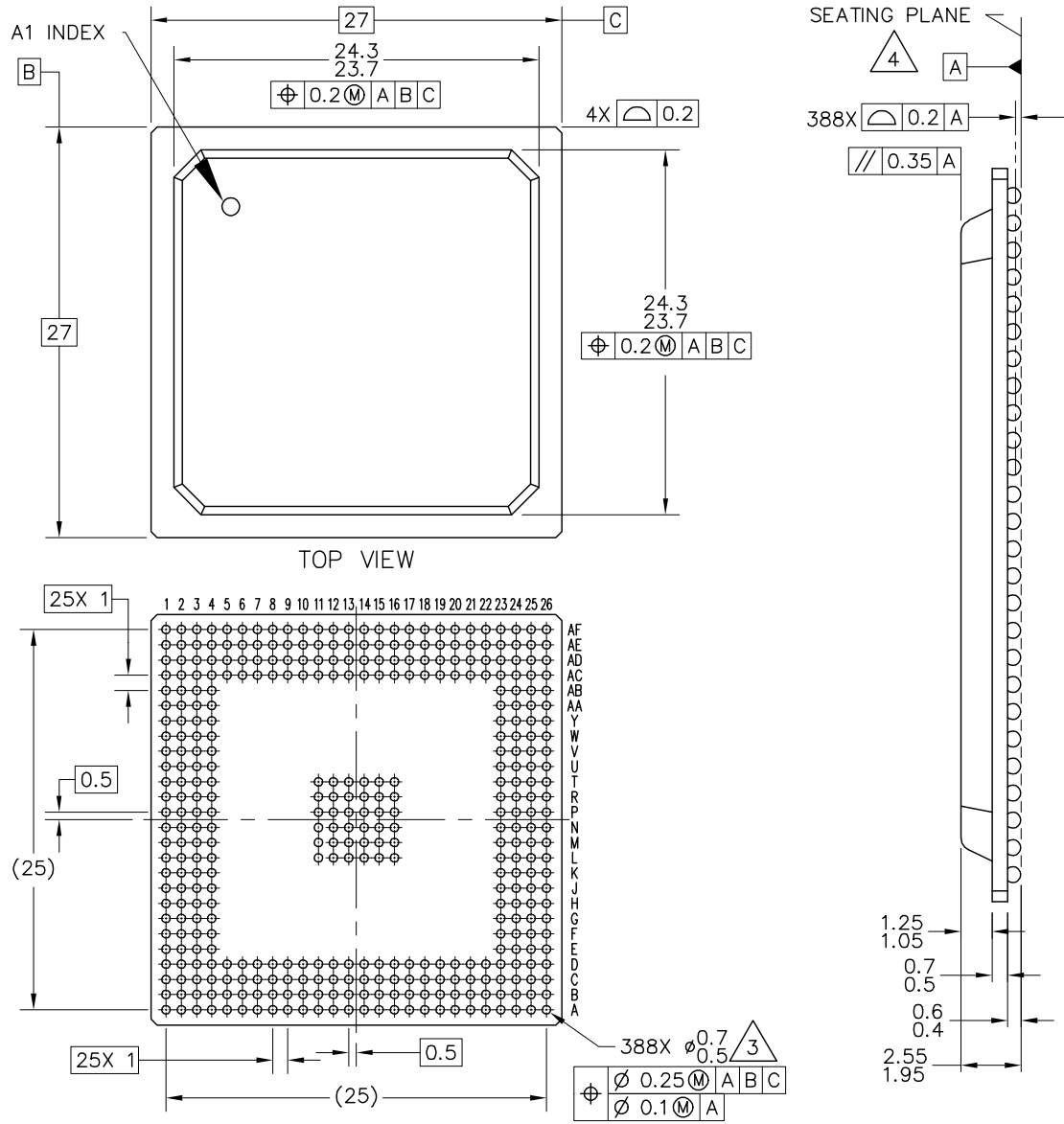
# 16 Timer Module AC Timing Specifications

Table 25 lists timer module AC timings.

**Table 25. Timer Module AC Timing Specifications**

Name	Characteristic	0–50 MHz		Unit
		Min	Max	
T1	TIN0 / TIN1 / TIN2 / TIN3 cycle time	3	—	PSTCLK
T2	TIN0 / TIN1 / TIN2 / TIN3 pulse width	1	—	PSTCLK

# 17 Case Drawing



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TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)		DOCUMENT NO: 98ARS23880W		REV: C	
		CASE NUMBER: 1164-02		25 JAN 2007	
		STANDARD: JEDEC MS-034 AAL-1			

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Document Number: MCF5485EC

Rev. 4

12/2007