NXP USA Inc. - FS32K142URT0VLHT Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k142urt0vlht

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

- 5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
- 6. Open drain outputs must be pulled to V_{DD} .
- 7. When input pad voltage levels are close to V_{DD} or V_{SS} , practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter			Unit	
		Min.	Тур.	Max.	
T _{A C-Grade Part}	Ambient temperature under bias	-40	—	85 ¹	°C
T _{J C-Grade Part}	Junction temperature under bias	-40	—	105 ¹	°C
T _{A V-Grade Part}	Ambient temperature under bias	-40	—	105 ¹	°C
T _{J V-Grade Part}	Junction temperature under bias	-40	—	125 ¹	°C
T _{A M-Grade Part}	Ambient temperature under bias	-40	—	125 ²	°C
T _{J M-Grade Part}	Junction temperature under bias	-40	—	135 ²	°C

1. Values mentioned are measured at \leq 112 MHz in HSRUN mode.

2. Values mentioned are measured at \leq 80 MHz in RUN mode.

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.			Dev	vice			Un
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	μA
		85	TBD	TBD	110	170	180	240	μA
		105	TBD	TBD	230	330	350	490	μA
		125	TBD	TBD	570	680	810	1250	μA
VLPS and LPUART	Clock source: SIRC	25	TBD	TBD	230	230	250	250	μA
TX/RX	 Transmiting or receiving continuously using DMA 	85	TBD	TBD	320	400	410	490	μA
	Baudrate: 19.2 kbps	105	TBD	TBD	490	550	600	850	μA
	125	TBD	TBD	890	1070	1250	1960	μA	
VLPS and LPUART	LPUART • Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	μA
wake-up		85	TBD	TBD	170	240	280	350	μA
		105	TBD	TBD	260	400	480	600	μA
		125	TBD	TBD	530	580	1000	1280	μA
VLPS and LPI2C	Clock Source: SIRC	25	TBD	TBD	670	690	820	900	μA
master	 Transmit/receive using DMA Baudrate: 100 kHz 	85	TBD	TBD	880	960	1220	1370	μA
		105	TBD	TBD	1080	1250	1660	2060	μA
		125	TBD	TBD	1970	1980	2860	3690	μA
VLPS and LPI2C	Clock source: SIRC	25	TBD	TBD	250	250	270	280	μA
slave wake-up	 Wake-up address feature enabled Baudrate: 100 kHz 	85	TBD	TBD	340	340	410	510	μA
		105	TBD	TBD	430	430	610	810	μA
		125	TBD	TBD	740	760	1170	1540	μA
VLPS and LPSPI	Clock source: SIRC	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
master	 Iransmit/receive using DMA Baudrate: 500 kHz 	85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mĀ
VLPS and LPIT	Clock source: SIRC	25	TBD	TBD	100	100	120	130	μA
	 1 cnannel enable Mode: 32-bit periodic counter 	85	TBD	TBD	190	250	260	320	μA
		105	TBD	TBD	310	410	440	570	μA
		125	TBD	TBD	640	750	910	1280	μĀ

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R _S	R _S Series resistor					
	Low-gain mode (HGO=0)	_	0	_	kΩ	
	High-gain mode (HGO=1)	_	0	—	kΩ	
V _{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	_	1.0	_	V	1
	High-gain mode (HGO=1)	_	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC} > 5 * gm_{crit}$. The gm_crit is defined as:

gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

where:

2.

- g_{mXOSC} is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- F is the external crystal oscillation frequency
- C₀ is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2 / (C_1 + C_2)]$
- C_s is stray or parasitic capacitance on the pin due to any PCB traces
- C1, C2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

- When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
 - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
- 3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Symbol	Descrip	otion ¹	S32	K142	S3	2K144	S32	K146	S32	K148		
			Тур	Max	Тур	Max	Тур	Max	Тур	Max	Unit	Notes
	setting (32-bit write complete, ready for next 32-bit write)	Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550	200	550		
t _{quickwr} Clnup	Quick Write Cleanup execution time		—	(# of Quick Writes) * 2.0		(# of Quick Writes) * 2.0		(# of Quick Writes) * 2.0		(# of Quick Writes) * 2.0	ms	7

Table 23. Flash command timing specifications for S32K14x (continued)

- 1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
- 2. Maximum times for erase parameters based on expectations at cycling end-of-life.
- For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
- 4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2× the times shown.
- 5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
- 6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
- 7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 24. Flash command timing specifications for S32K11x

Symbol	Descripti	on ¹	S32	K116	Sa	32K118		_
			Тур	Max	Тур	Max	Unit	Notes
t _{rd1blk}	Read 1 Block execution	32 KB flash	-	0.36	-	0.36	ms	
	time	64 KB flash	—	—	—	—		
		128 KB flash	—	1.2	—	—		
		256 KB flash	—	_	—	2	-	
		512 KB flash	—	—	—	—		
t _{rd1sec} Rea exe	Read 1 Section	2 KB flash	—	75	—	75	μs	
	execution time	4 KB flash	—	100	—	100		
t _{pgmchk}	Program Check execution time	—	_	100	_	100	μs	
t _{pgm8}	Program Phrase execution time	—	90	225	90	225	μs	
t _{ersblk}	Erase Flash Block	32 KB flash	15	300	15	300	ms	2
	execution time	64 KB flash	—	—	—	—		
		128 KB flash	120	1100	—	—		
		256 KB flash	—	_	250	2125		
		512 KB flash	_	_	_	_]	

Table continues on the next page ...

Table 25.	NVM reliability	/ S	pecifications	(continued))
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Symbol	Description		Тур.	Max.	Unit	Notes
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
t _{nvmretee}	Data retention	5	—	—	years	4
n _{nvmwree16}	Write endurance EEPROM backup to FlexRAM ratio = 16 	100 K	_	_	writes	5, 6, 7
n _{nvmwree256}	 EEPROM backup to FlexRAM ratio = 256 	1.6 M	—	—	writes	

- 1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
- 2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
- 3. Cycling endurance is per DFlash or PFlash Sector.
- 4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
- FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
- 6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
- 7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The "In Spec" portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn't have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
f _{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f _{CONV}	ADC conversion frequency	No ADC hardware averaging. ⁵ Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. ⁵ Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

Table 27. 12-bit ADC operating conditions (continued)

- 1. Typical values assume $V_{DDA} = 5 V$, Temp = 25 °C, $f_{ADCK} = 40 \text{ MHz}$, $R_{AS}=20 \Omega$, and $C_{AS}=10 \text{ nF}$ unless otherwise stated. Typical values are for reference only, and are not tested in production.
- For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
- 3. Clock and compare cycle need to be set according to the guidelines mentioned in the Reference Manual .
- 4. ADC conversion will become less reliable above maximum frequency.
- 5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
- 6. Numbers based on the minimum sampling time of 275 ns.
- 7. For guidelines and examples of conversion rate calculation, see the Reference Manual section 'Calibration function'



Figure 13. ADC input impedance equivalency diagram

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6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V _{DDA}	Supply voltage		2.7	—	3	V	
I _{DDA_ADC}	Supply current per ADC			0.6	_	mA	3
SMPLTS	Sample Time		275	_	Refer to the <i>Reference</i> <i>Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity			±1.0	_	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity			±2.0		LSB ⁵	6, 7, 8, 9

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

- 1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
- 2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω , and C_{AS}=10 nF.
- 3. The ADC supply current depends on the ADC conversion rate.
- 4. Represents total static error, which includes offset and full scale error.
- 5. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
- For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
- 8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
- 9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V _{DDA}	Supply voltage		3	—	5.5	V	
I _{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	_	Refer to the <i>Reference</i> <i>Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity			±1.0	—	LSB ⁵	6, 7, 8, 9

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

- 1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
- 2. Typical values assume $V_{DDA} = 5.0 \text{ V}$, Temp = 25 °C, $f_{ADCK} = 40 \text{ MHz}$, $R_{AS}=20 \Omega$, and $C_{AS}=10 \text{ nF}$ unless otherwise stated.
- 3. The ADC supply current depends on the ADC conversion rate.
- 4. Represents total static error, which includes offset and full scale error.
- 5. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
- For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
- 8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
- 9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Symbol	Description	Min.	Тур.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	_	23	80	
V _{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	_	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	_	32	120	
I _{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	_	6	9	μA
	5V Reference Voltage	_	10	16	μA
INL ⁵	8-bit DAC integral non-linearity	-0.75	—	0.75	LSB ⁶
DNL	8-bit DAC differential non-linearity	-0.5	—	0.5	LSB ⁶
t _{DDAC}	Initialization and switching settling time	_	—	30	μs

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

1. Difference at input > 200mV

2. Applied \pm (100 mV + V_{HYST0/1/2/3}+ max. of V_{AIO}) around switch point.

3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$ + max. of V_{AIO}) around switch point.

4. Applied \pm (100 mV + V_{HYST0/1/2/3}).

5. Calculation method used: Linear Regression Least Square Method

6. 1 LSB = $V_{reference}/256$

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/ EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).





Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)



Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

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Table 32. LPSPI electrical specifications1 (continued)

N	um	Symbol	Description	Conditions		Run	Mode ²			HSRU	N Mode ²			VLPR	Mode		Unit
					5.0	V IO	3.3	V IO	5.0	V IO	3.3	V IO	5.0	V IO	3.3	/ 10	
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	4	t _{Lag} 9	Enable lag	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			time (After	Master		-		-		-		-		-		-	
				Master Loopback ⁵	- 25		- 25		- 25		- 25		- 50		- 50		
				Master Loopback(slow) ⁶	(SCKPCS+1)*t _{periph}		(SCKPCS+1)*t _{periph}		(SCKPCS+1)*t _{periph}		(SCKPCS+1)*t _{periph}		(SCKPCS+1)*t _{periph}		(SCKPCS+1)*t _{periph}		
	5 t _{WSPSCK} ¹⁰ Clock(SPSCK	Slave													ns		
) high or low time (SPSCK duty cycle) Master Loopback ⁵) high or low time (SPSCK	ဂု	ς +3	ကို	с +3	ကို	ς +3	ကို	ς + γ	2-5	1-2	- 2	+2	
	duty cy			Master Loopback ⁵	SPSCK/	sPSCK/2	SPSCK	sPSCK/2	SPSCK	sPSCK/2	SPSCK/2	sPSCK/2	SPSCK/2	sPSCK/2	SPSCK	spsck/2	
				Master Loopback(slow) ⁶	t t	÷,	1	<u>ب</u>	1	<u>ب</u>	t	ů,	4	ů,	t t	ţ	
	6	t _{SU}	Data setup	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			time(inputs)	Master	29	-	38	-	26	-	37 ¹¹ 32 ¹²	-	72	-	78	-	
				Master Loopback ⁵	7	-	8	-	5	-	7	-	20	-	20	-	
				Master Loopback(slow) ⁶	8	-	10	-	7	-	9	-	20	-	20	-	
	7 t _{HI}	Data hold	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns	
			time(inputs)	Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback ⁵	3	-	3	-	2	-	3	-	11	-	11	-		
				Master Loopback(slow) ⁶	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

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Table 32. LPSPI electrical specifications1 (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²			VLPR Mode				Unit	
				5.0 V IO		5.0 V IO 3.3 V IO		5.0	5.0 V IO 3.3 V IO		5.0 V IO		3.3 V IO			
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master Loopback(slow) 6	-		-		-		-		-		-		

- 1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
- 2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
- 3. f_{periph} = LPSPI peripheral clock
- 4. $t_{periph} = 1/f_{periph}$
- 5. Master Loopback mode In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
- 6. Master Loopback (slow) In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
- 7. This is the maximum operating frequency (f_{op}) for LPSPI0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
- 8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
- 9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
- 10. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
- 11. Maximum operating frequency (fop) is 12 MHz irrespective of PAD type and LPSPI instance.
- 12. Applicable for LPSPI0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.

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Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Symbol	Description	Min.	Max.	Unit
_	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	_	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	_	ns
—	TXCLK frequency	_	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2		ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	_	25	ns

Table 35. MII signal switching specifications

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Table 40. JTAG electrical specifications

Symbol	Description	Run Mode			HSRUN Mode				VLPR Mode					
		5.0 V IO		3.3	V IO	5.0	V IO	3.3	V IO	5.0	V IO	3.3	V IO]
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
JI	TCLK frequency of operation		!		·!	!		•			!		- <u>I</u>	MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	1
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	1
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	ns
JЗ	TCLK clock pulse width	1			-	1	1				-1		-	ns
	Boundary Scan	ю	ى س	ы	Q	ы	ى س	ы	ц.	ы	Q	10	Q	1
	JTAG	J2/2 -	J2/2 +	J2/2 - {	J2/2 +	J2/2 -	J2/2 +	J2/2 - 1	J2/2 +	J2/2 - 1	J2/2 +	J2/2 - 1	J2/2 +	
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

Debug modules





7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_{J} = T_{A} + (R_{\theta JA} \times P_{D})$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	 Updated descpition of QSPI and Clock interfaces in Key Features section Updated figure: High-level architecture diagram for the S32K1xx family Updated figure: S32K1xx product series comparison Added note in section Selecting orderable part number Updated figure: Ordering information In table: Absolute maximum ratings : Added footnote to I_{INJPAD_DC} Updated description, max and min values for I_{INJSUM} Updated description, max and V_{IN} Removed V_{INA} and V_{IN} Added footnote "Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V Removed I_{NJSUM_AF} Updated footnotes in table Table 4 Updated conditions for VLPR Removed ldd/MHz for S32K142 Updated numbers for S32K142 Updated numbers for S32K142 and S32K148 Removed use case footnotes In section Modes configuration : Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet' In table: DC electrical specifications at

Table 43. Revision History

Table continues on the next page...

S32K1xx Data Sheet, Rev. 8, 06/2018

Rev. No.	Date	Substantial Changes
		 Fixed the typo in R_{SW1} In LPSPI electrical specifications : Updated t_{Lead} and t_{Lag} Added footnote in Figure: LPSPI slave mode timing (CPHA = 0) and Figure: LPSPI slave mode timing (CPHA = 1) In Thermal characteristics : Updated the name of table: Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package Deleted specs for R_{0JC} for 32 QFN package Added 'R_{0JCBottom}'
8	18 June 2018	 In attachement 'S32K1xx_Power_Modes _Configuration': Updated VLPR peripherals disabled and Peripherals Enabled use case #1, using 4 Mhz for System clock, 2 Mhz for bus clock, and 1Mhz for flash. Removed S32K116 from Notes In figure: S32K1xx product series comparison :

Rev. No.	Date	Substantial Changes
		 Updated specs for T_{JIT} Cycle-to-Cycle jitter to 300 ps In QuadSPI AC specifications : Updated specs for T_{iv} Data Output In-Valid Time In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area In CMP with 8-bit DAC electrical specifications : Removed '(VAIO)' from decription of V_{HYST0} In LPSPI electrical specifications : Added note 'Undefined' in figures 'LPSPI slave mode timing (CPHA = 0)' and 'LPSPI slave mode timing (CPHA = 1)'

Table 43. Revision History