NXP USA Inc. - FS32K144HAT0MLHR Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144hat0mlhr

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

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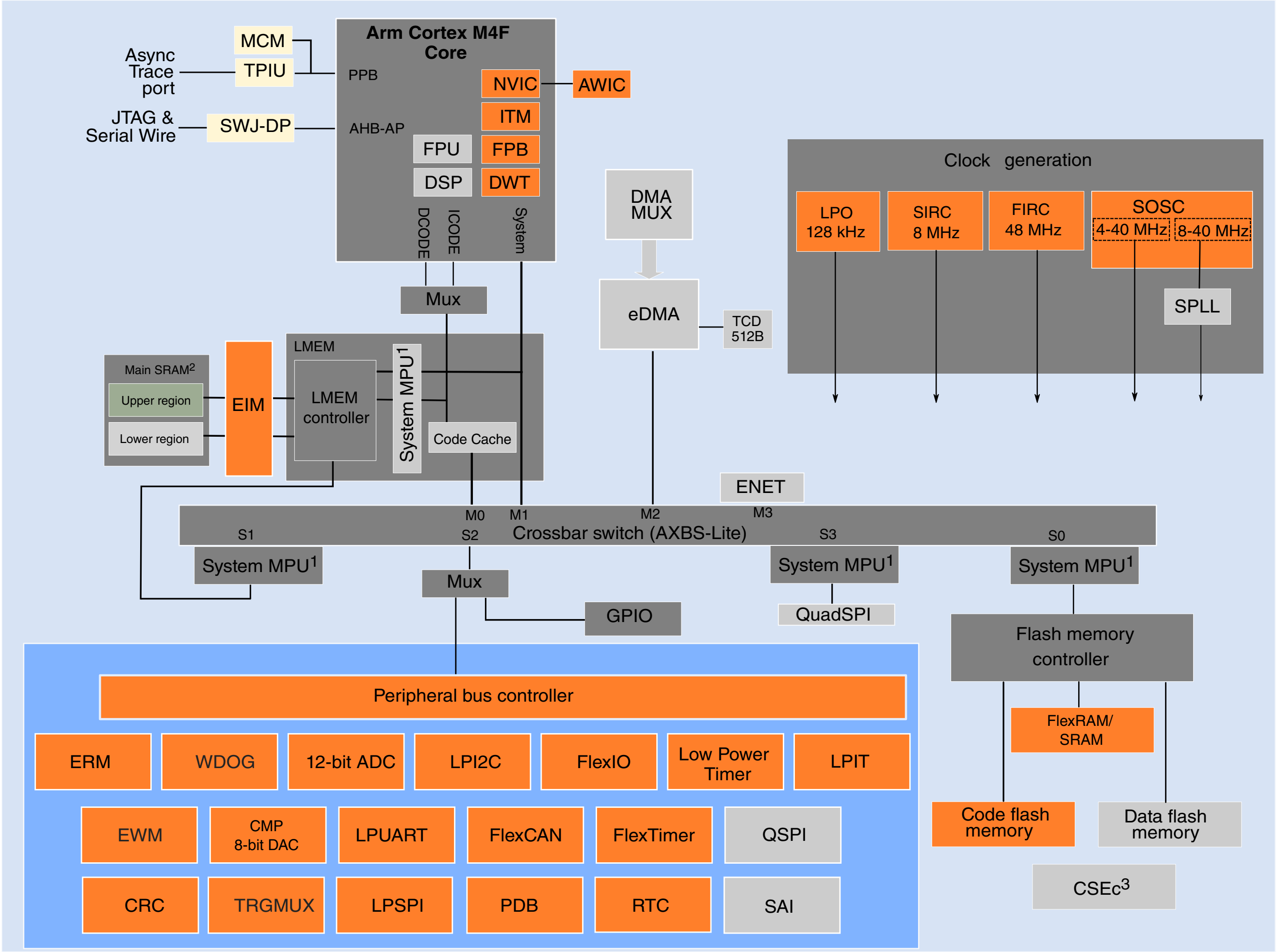
1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

Key:

- Device architectural IP on all S32K devices
- Peripherals present on all S32K devices
- Peripherals present on selected S32K devices (see the "Feature Comparison" section)

Figure 1. High-level architecture diagram for the S32K14x family

5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-Grade Part}}$	Ambient temperature under bias	–40	—	85[1]	℃
$T_{J\ C\text{-Grade Part}}$	Junction temperature under bias	–40	—	105[1]	℃
$T_{A\ V\text{-Grade Part}}$	Ambient temperature under bias	–40	—	105[1]	℃
$T_{J\ V\text{-Grade Part}}$	Junction temperature under bias	–40	—	125[1]	℃
$T_{A\ M\text{-Grade Part}}$	Ambient temperature under bias	–40	—	125[2]	℃
$T_{J\ M\text{-Grade Part}}$	Junction temperature under bias	–40	—	135[2]	℃

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

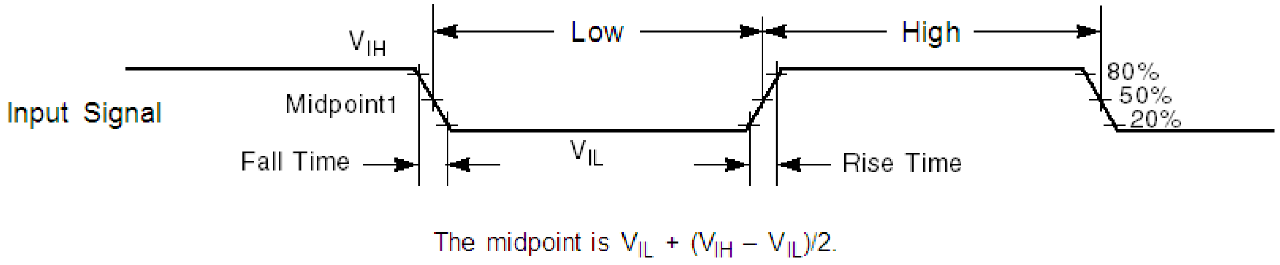


Figure 7. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be filtered by internal filter.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 11 and Table 12, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 11. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	14	—	—	mA	4
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	5
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	μA	
	High drive port pins [7]		0.010	0.5	μA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 16. Device clock specifications [1] (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

6.3.1.1 Flash timing specifications — commands

Table 23. Flash command timing specifications for S32K14x

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	—	2	—	—	—	—	—	—		
		512 KB flash	—	—	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	—	75	μs	
		4 KB flash	—	100	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	95	—	100	μs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	90	225	μs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	250	2125	—	—	—	—	—	—		
		512 KB flash	—	—	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	—	30	μs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	90	—	μs	
t_{ersall}	Erase All Blocks execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	—	35	—	35	μs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	70	—	—	—	ms	3
		64 KB EEPROM backup	71	—	71	—	71	—	150	—		

Table continues on the next page...

Table 25. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	4
	Write endurance					5, 6, 7
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	100 K	—	—	writes	
$n_{nvmwree256}$	• EEPROM backup to FlexRAM ratio = 256	1.6 M	—	—	writes	

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 26. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	-	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Table 32. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph}[3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14 [7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14 [7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-50$	-	$(PCSSCK+1)*t_{periph}-50$	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													

Table continues on the next page...

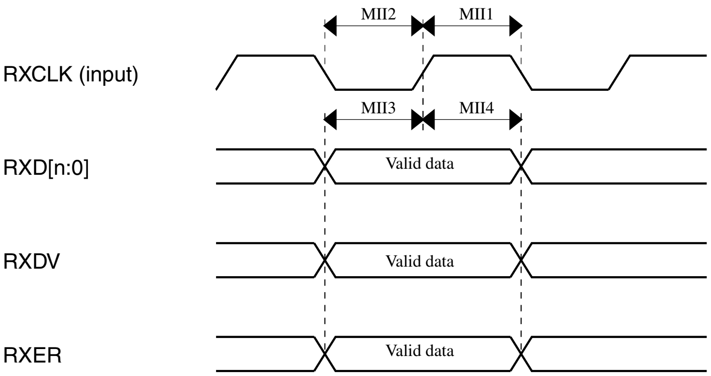


Figure 24. MII receive diagram

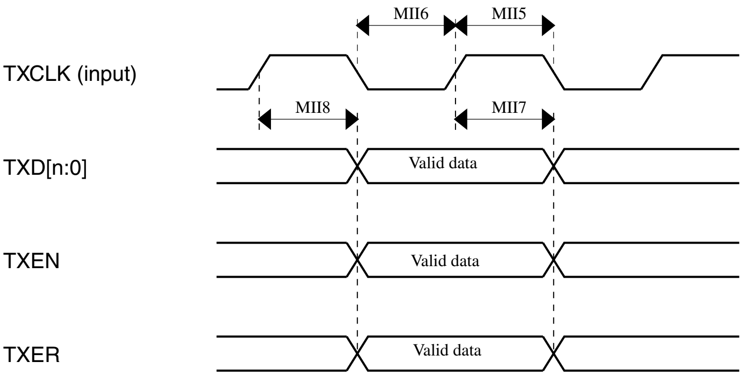


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

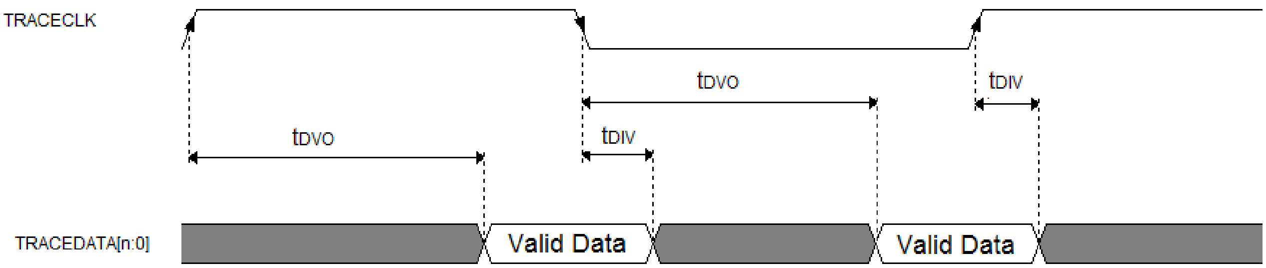


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) [1,2]	Single layer board (1s)	$R_{\theta JA}$	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) [1,2,3]	Four layer board (2s2p)	$R_{\theta JA}$	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) [1,2,3]	Single layer board (1s)	$R_{\theta JMA}$	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1,3]	Two layer board (2s2p)	$R_{\theta JMA}$	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center[6]	—	Ψ_{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center[7]	—	Ψ_{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Table 43. Revision History

<table>
<tr><th>Rev. No.</th><th>Date</th><th>Substantial Changes</th></tr>
<tr><td></td><td></td><td>

Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled'
Updated numbers for:

VLPR → VLPS
VLPS → VLPR
'RUN → Compute operation'
RUN → VLPS
RUN → VLPR

In Power consumption :

Updated specs for S32K142, S32K144, and S32K148
Updated footnote 'Typical current numbers are indicative ...'
Updated footnote 'The S32K148 data ...'
Removed footnote 'Above S32K148 data is preliminary targets only'
Added new table 'Power consumption at 3.3 V'

In General AC specifications :

Updated max value and footnote of WFRST
Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote

Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range
Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range
In Device clock specifications :

Updated f_{BUS} to 48 for 11x
Added footnote to f_{BUS} for 14x

In External System Oscillator frequency specifications :

Added specs for S32K11x
Updated 't_{dc_extal}' for S32K14x
Added footnote 'Frequecies below ... ' to 'f_{ec_extal}' and 't_{dc_extal}'

Splitted Flash timing specifications — commands for S32K14x and S32K11x
Updated Flash timing specifications — commands for S32K14x
In Reliability specifications :

Added footnote 'Data retention period ... ' for 'tnvmretp1k' and 'tnvmretee'
Minor update in footnote for 'nnvmwree16' 'nnvmwree256'

In QuadSPI AC specifications :

Updated 'MCR[SCLKCFG[5]]' value to 0
Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6
Updated 'Data Input Setup Time' DDR External DQS min. value to 2
Updated 'Data Input Hold Time' DDR External DQS min. value to 20
Upadted figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram'

In 12-bit ADC electrical characteristics :

Added note 'On reduced pin packages where ... '
Removed max. value of 'I_{DDA_ADC}'
Added note 'Due to triple ... '

In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}'
In CMP with 8-bit DAC electrical specifications :

Updated Typ. and Max. values of 'I_{DDLS}'
Upadted Typ. value of 't_{DHSB}'
Updated Typ. value of 'V_{HYST1}' , 'V_{HYST2}', and 'V_{HYST3}'

In LPSPI electrical specifications :

Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

</td></tr>
</table>

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Fixed the typo in R_{SW1} • In LPSPI electrical specifications : • Updated t_{Lead} and t_{Lag} • Added footnote in Figure: LPSPI slave mode timing (CPHA = 0) and Figure: LPSPI slave mode timing (CPHA = 1) • In Thermal characteristics : • Updated the name of table: Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package • Deleted specs for $R_{\theta JC}$ for 32 QFN package • Added '$R_{\theta JCBottom}$'
8	18 June 2018	• In attachement '*S32K1xx_Power_Modes _Configuration*': • Updated VLPR peripherals disabled and Peripherals Enabled use case #1, using 4 Mhz for System clock, 2 Mhz for bus clock, and 1Mhz for flash. • Removed S32K116 from Notes • In figure: S32K1xx product series comparison : • Added note 'Availability of peripherals depends on the pin availability ...' • Updated 'Ambient Operation Temperature' row • Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148 • In Ordering information : • Updated figure for 'Y: Optional feature' • Updated footnote 3 • In Power and ground pins : • In figure 'Power diagram', updtaed V_{Flash} frequency to 3.3 V • In Power mode transition operating behaviors : • Updated footnote for 'VLPS Mode: All clock sources disabled' • In Power consumption : • Added IDDs for S32K116 • Added VLPR Peripherals enabled use case 2 at 125 °C/Typicals • Renamed VLPR 'Peripherals enabled' to 'Peripherals enabled use case 1' • Added footnote 'Data collected using RAM' to VLPR 'Peripherals disabled' and VLPR 'Peripherals enabled use case 1' • Updated VLPS Peripherals enabled at 25 °C/Typicals for S32K142 and S32K144 to 40 μA and 42 μA respectively • Added table 'VLPS additional use-case power consumption at typical conditions' • In DC electrical specifications at 3.3 V Range : • Updated naming conventions • Added specs for GPIO-FAST pad • In DC electrical specifications at 5.0 V Range : • Updated naming conventions • Added specs for GPIO-FAST pad • In AC electrical specifications at 3.3 V range : • Updated naming conventions • Added specs for GPIO-FAST pad • In AC electrical specifications at 5 V range : • Updated naming conventions • Added specs for GPIO-FAST pad • In External System Oscillator electrical specifications : • Clarified description of g_{mXOSC} • Updated V_{IL} max. to 1.15 V • In Fast internal RC Oscillator (FIRC) electrical specifications :