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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144hft0vllr

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

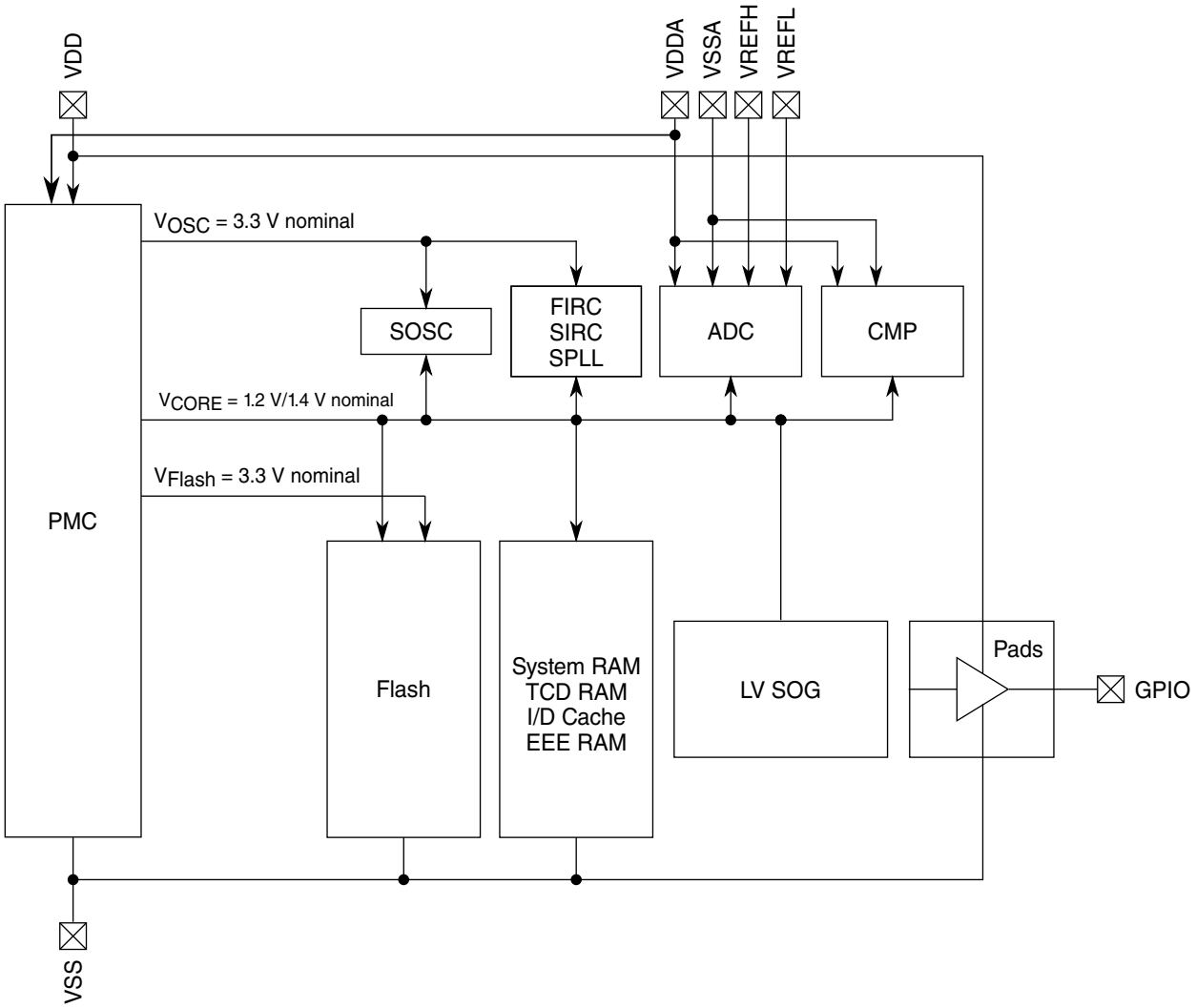
NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements 1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.



*Note: VSSA and VSS are shorted at package level

Figure 6. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1

Table continues on the next page...

Table 7. Power consumption (Typicals unless stated otherwise) 1

Chip/Device	Ambient Temperature (°C)		VLPS (µA) 2		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) 3		IDD/MHz (µA/MHz) 4
			Peripherals disabled 5	Peripherals enabled	Peripherals disabled 6	Peripherals enabled use case 1 6	Peripherals enabled use case 2 7			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
S32K116	25	Typ	26	40	1.05	1.07	TBD	6.3	7.2	11.8	20.3	NA						245
	85	Typ	76	93	1.1	1.11	TBD	6.6	7.5	12	20.6							251
		Max	287	300	1.39	1.4	NA	8	8.9	13.4	22.1							279
	105	Typ	139	164	1.15	1.16	TBD	6.8	7.7	12.3	20.8							255
		Max	590	603	1.68	1.69	NA	9.2	10.1	14.5	23.1							302
	125	Typ	NA	NA	NA	NA	TBD	NA	NA	NA	NA							NA
		Max	891	904	2.02	2.04	NA	10.4	11.3	15.6	24.1							325
S32K118	25	Typ	26	38	1.9	2.5	TBD	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	42							TBD
S32K142	25	Typ	29	40	1.17	1.21	2.19	6.4	7.4	17.3	24.6	24.5	31.3	28.8	37.5	40.5	52.2	360
	85	Typ	128	137	1.48	1.51	2.31	7	8	17.6	24.9	25	31.6	29.1	37.7	41.1	52.5	364
		Max	335	360	1.87	1.89	NA	8.6	9.4	22	28.2	26.9	33.5	32	40	44	55.6	400
	105	Typ	240	257	1.58	1.61	2.44	7.6	8.3	18.3	25.7	25.5	31.9	29.8	38	41.5	53.1	373
		Max	740	791	2.32	2.34	NA	9.9	10.9	23.1	30.2	27.8	35.3	33.8	40.7	44.9	57.4	423
	125	Typ	NA	NA	NA	NA	2.84	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA

Table continues on the next page...

6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					5
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	6
R_{PD}	Internal pulldown resistors	20		50	kΩ	7

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 16. Device clock specifications [1] (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms	3
		64 KB EEPROM backup	—	—	—	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2		
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	µs	

Table continues on the next page...

Table 25. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	4
$n_{nvmwree16}$	Write endurance • EEPROM backup to FlexRAM ratio = 16	100 K	—	—	writes	5, 6, 7
$n_{nvmwree256}$	• EEPROM backup to FlexRAM ratio = 256	1.6 M	—	—	writes	

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 26. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	-	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. [5] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'

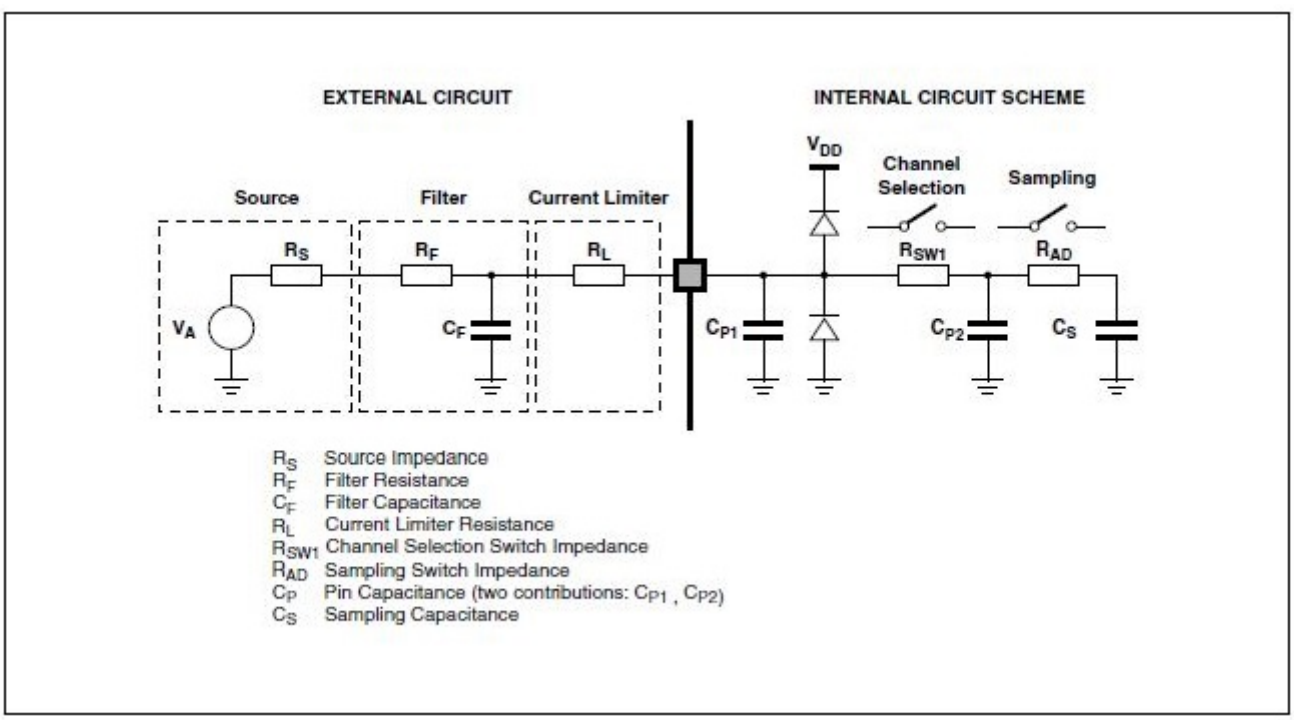


Figure 13. ADC input impedance equivalency diagram

6.4.2 CMP with 8-bit DAC electrical specifications

Table 31. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs
	-40 - 125 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	

Table continues on the next page...

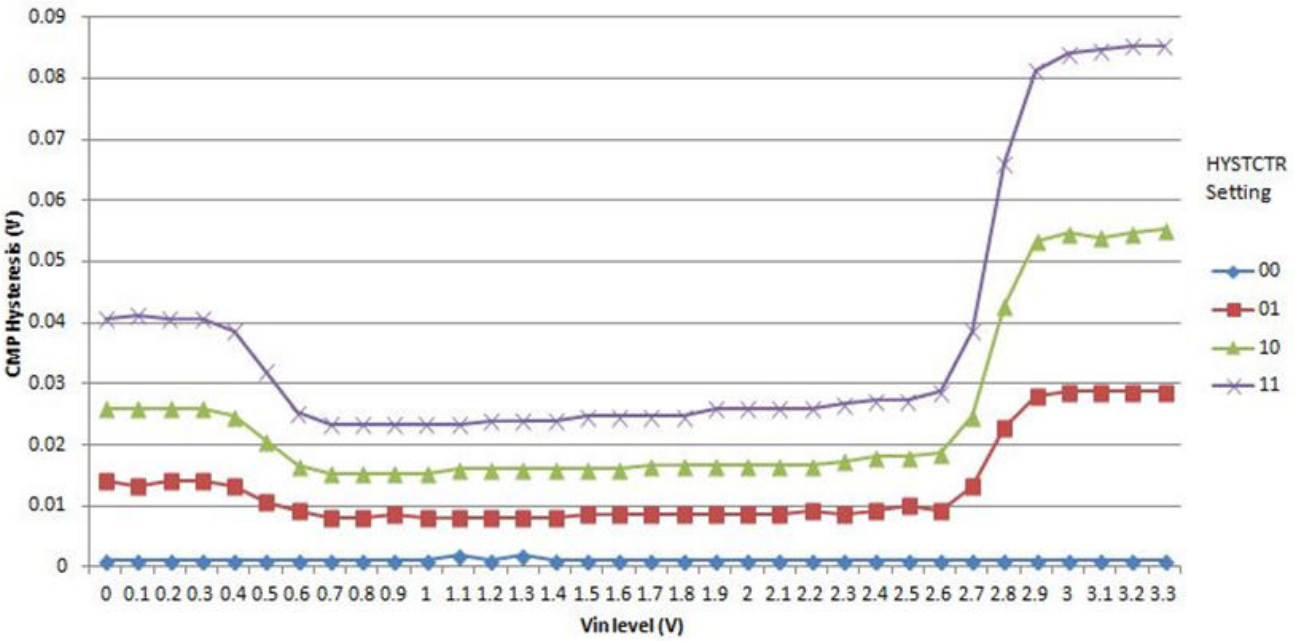


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

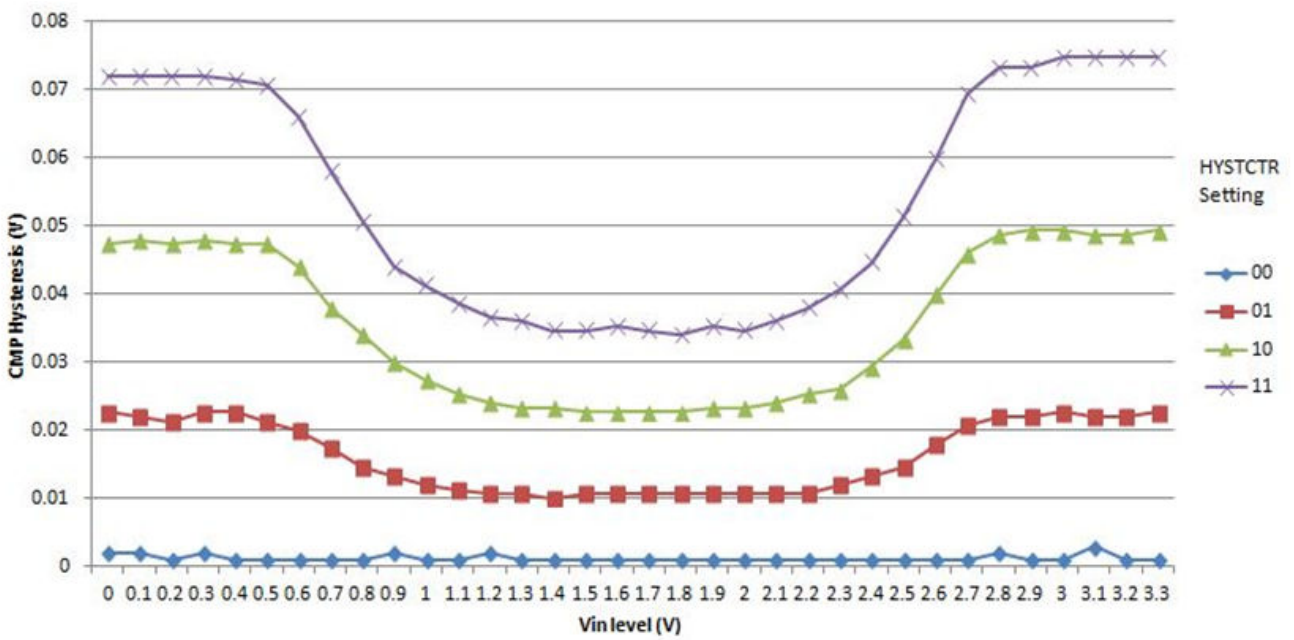


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32[12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

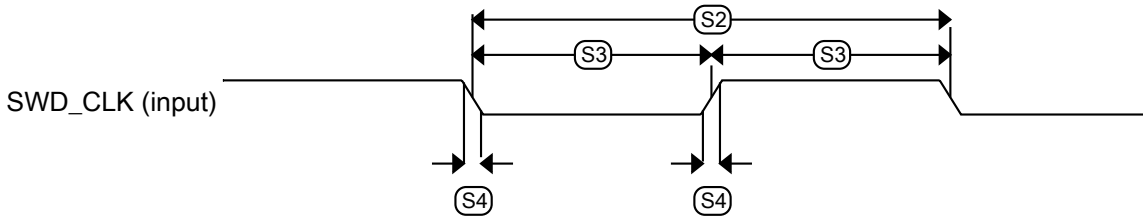


Figure 29. Serial wire clock input timing

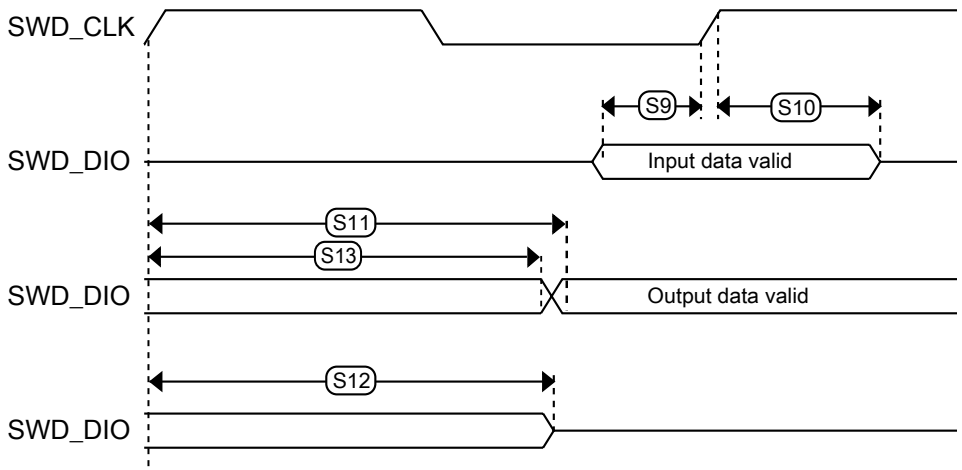


Figure 30. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 39. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

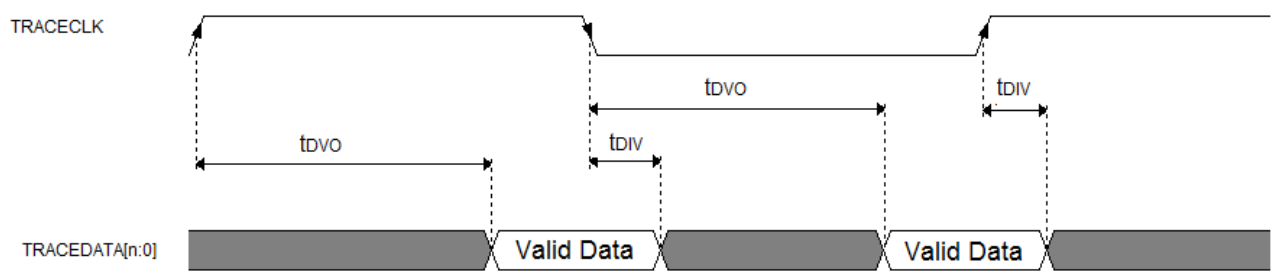


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

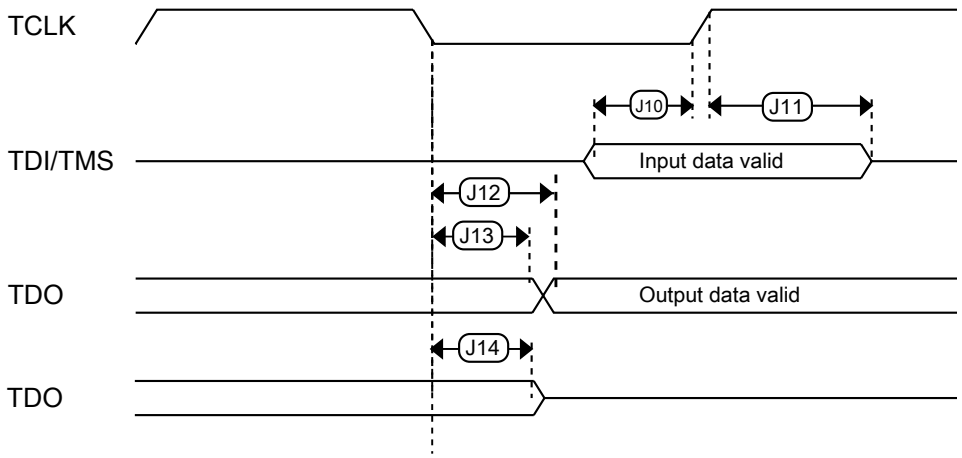


Figure 34. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
			144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnotes V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		• Updated table: AC electrical specifications at 3.3 V range
		• Updated table: AC electrical specifications at 5 V range
		• In table: Standard input pin capacitance
		  • Added footnote to Normal run mode (S32K14x series)
		• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme
		• In table: External System Oscillator electrical specifications
		  • Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz
		  • Removed rows for I_{lk_ext} EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL}
		  • Updated Typ. of R_S low-gain mode
		  • Updated description of R_F, R_S, and V_{PP}
		  • Removed footnote from R_F Feedback resistor
		  • Updated footnote for C_1 C_2 and R_F
		• In table: Table 18
		  • Removed mention of high-frequency
		  • Added HGO 0, 1 information
		• In table: Fast internal RC Oscillator electrical specifications
		  • Updated F_{FIRC}
		  • Updated description of ΔF
		  • Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Updated naming convention of I_{DDFIRC} Supply current
		  • Added footnote to I_{DDFIRC} Supply current
		  • Added footnote to column Parameter
		• In table: Slow internal RC oscillator (SIRC) electrical specifications
		  • Removed V_{DD} Supply current in 2 MHz Mode
		  • Removed footnote and updated description of ΔF
		  • Updated footnote to F_{SIRC} and I_{DDSIRC}
		• In table: SPLL electrical specifications
		  • Added row for F_{SPLL_REF} PLL Reference
		  • Updated naming convention throughout the table
		  • Updated the max value of T_{SPLL_LOCK} Lock detector detection time
		• In table: Flash timing specifications — commands
		  • Added footnotes:
		  • All command times assumes ...
		  • For all EEPROM Emulation terms ...
		  • 'First time' EERAM writes after a POR ...
		  • Removed footnote 'Assumes 25 MHz or ...'
		  • Updated Max of $t_{eewr32bers}$
		  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$
		• In table: Reliability specifications
		  • Removed Typ. values for all parameters
		  • Removed footnote 'Typical values represent ... '
		  • Added footnote 'Any other EEE driver usage ... '
		• Updated QuadSPI AC specifications
		• Removed topic: Reliability, Safety and Security modules
		• In table: 12-bit ADC operating conditions
		  • Updated V_{DDA}

Table continues on the next page...