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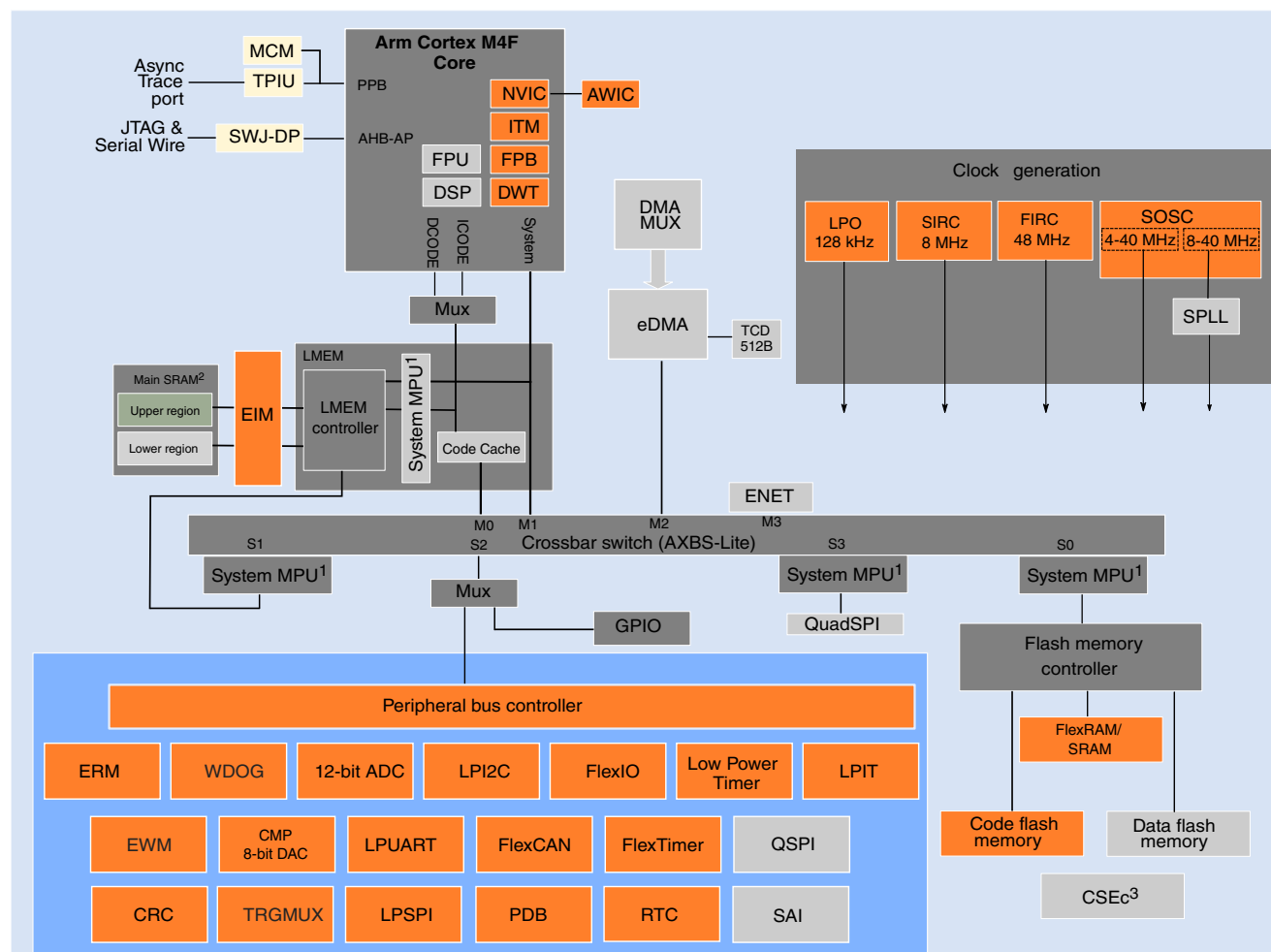
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144hnt0cllt

1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See [Feature comparison](#) for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

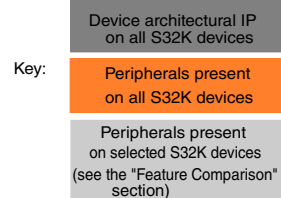


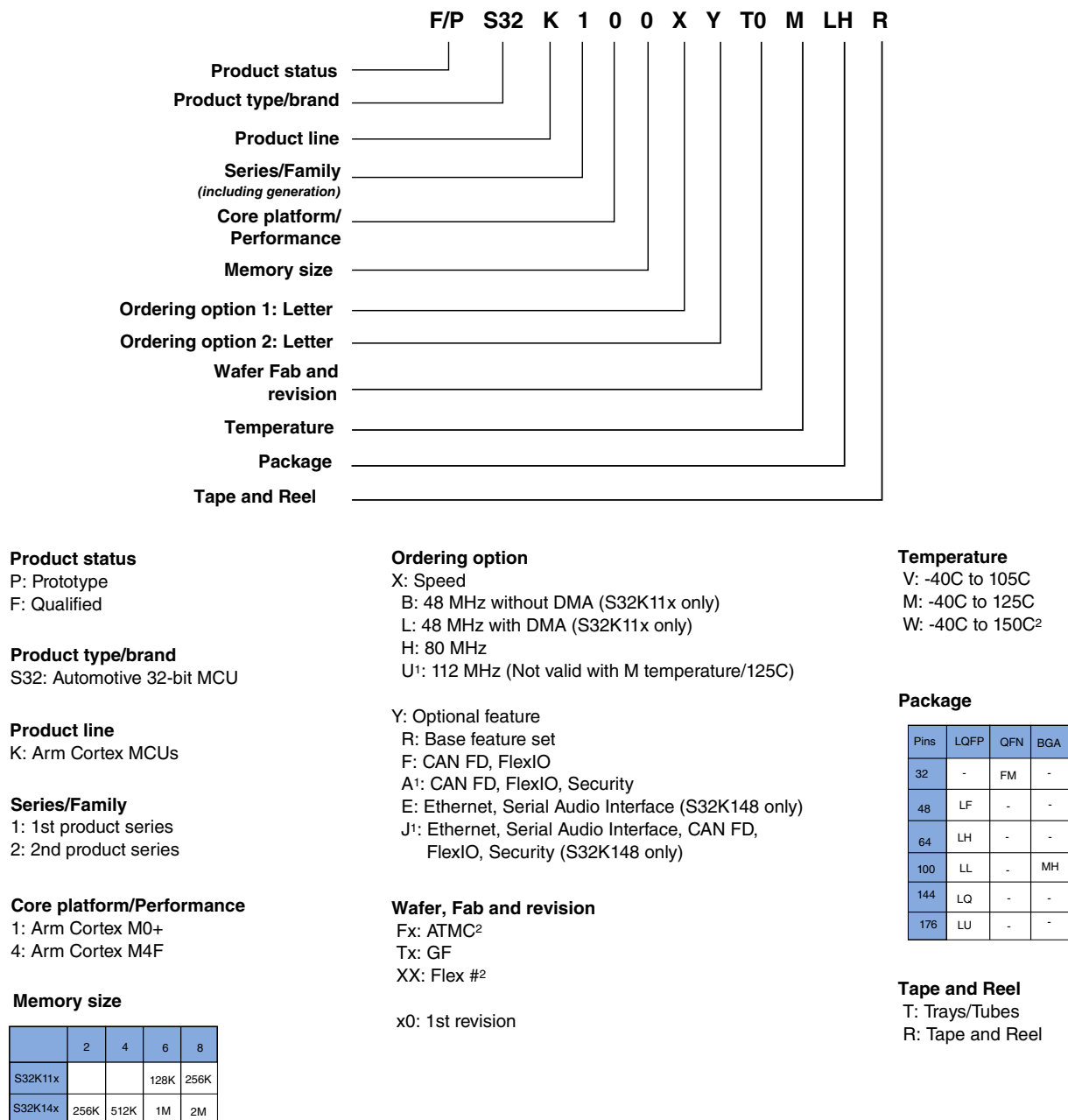
Figure 1. High-level architecture diagram for the S32K14x family

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

3.2 Ordering information



- CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
- Not supported yet
- Part numbers no longer offered as standard include:
Ordering Option X (M:64MHz); Ordering Option Y (N: limited RAM. 16KB for K142, 48KB for K144, 96KB for K146, 192KB for K148
S: Security); Temperature (C: -40C to 85C)

NOTE

Not all part number combinations are available. See S32K1xx_Orderable_Part_Number_List.xlsx attached with the Datasheet for list of standard orderable parts.

Figure 4. Ordering information

5. V_{REFH} should always be equal to or less than $V_{DDA} + 0.1\text{ V}$ and $V_{DD} + 0.1\text{ V}$
6. Open drain outputs must be pulled to V_{DD} .
7. When input pad voltage levels are close to V_{DD} or V_{SS} , practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T_A C-Grade Part	Ambient temperature under bias	-40	—	85 ¹	°C
T_J C-Grade Part	Junction temperature under bias	-40	—	105 ¹	°C
T_A V-Grade Part	Ambient temperature under bias	-40	—	105 ¹	°C
T_J V-Grade Part	Junction temperature under bias	-40	—	125 ¹	°C
T_A M-Grade Part	Ambient temperature under bias	-40	—	125 ²	°C
T_J M-Grade Part	Junction temperature under bias	-40	—	135 ²	°C

1. Values mentioned are measured at $\leq 112\text{ MHz}$ in HSRUN mode.
2. Values mentioned are measured at $\leq 80\text{ MHz}$ in RUN mode.

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- HSRUN Mode:
 - Clock source: SPL
 - SYS_CLK/CORE_CLK = 112 MHz
 - BUS_CLK = 56 MHz
 - FLASH_CLK = 28 MHz
- VLPR Mode:
 - Clock source: SIRC
 - SYS_CLK/CORE_CLK = 4 MHz
 - BUS_CLK = 4 MHz
 - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled ¹

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	μs

Table continues on the next page...

1.

- For S32K11x – FIRC/SOSC
- For S32K14x – FIRC/SOSC/SPLL

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ¹	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I _{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in [Table 11](#) and [Table 12](#), see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 11. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	2
V_{il}	Input Buffer Low Voltage	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	3
V_{hys}	Input Buffer Hysteresis	$0.06 \times V_{DD}$	—	—	V	
$I_{oh_{GPIO}}$ $I_{oh_{GPIO-HD_DSE_0}}$	I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$	3.5	—	—	mA	
$I_{ol_{GPIO}}$ $I_{ol_{GPIO-HD_DSE_0}}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	3	—	—	mA	
$I_{oh_{GPIO-HD_DSE_1}}$	I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$	14	—	—	mA	4
$I_{ol_{GPIO-HD_DSE_1}}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	12	—	—	mA	4
$I_{oh_{GPIO-FAST_DSE_0}}$	I/O current sink capability measured when pad $V_{oh}=V_{DD}-0.8 \text{ V}$	9.5	—	—	mA	5
$I_{ol_{GPIO-FAST_DSE_0}}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	10	—	—	mA	5
$I_{oh_{GPIO-FAST_DSE_1}}$	I/O current sink capability measured when pad $V_{oh}=V_{DD}-0.8 \text{ V}$	16	—	—	mA	5
$I_{ol_{GPIO-FAST_DSE_1}}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at $V_{DD} = 3.3 \text{ V}$					6
	All pins other than high drive port pins		0.005	0.5	μA	
	High drive port pins ⁷		0.010	0.5	μA	
R_{PU}	Internal pullup resistors	20		60	$k\Omega$	8
R_{PD}	Internal pulldown resistors	20		60	$k\Omega$	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the $I_{oh_Standard}$ value given above.
5. For reference only. Run simulations with the IBIS model and custom board for accurate results.

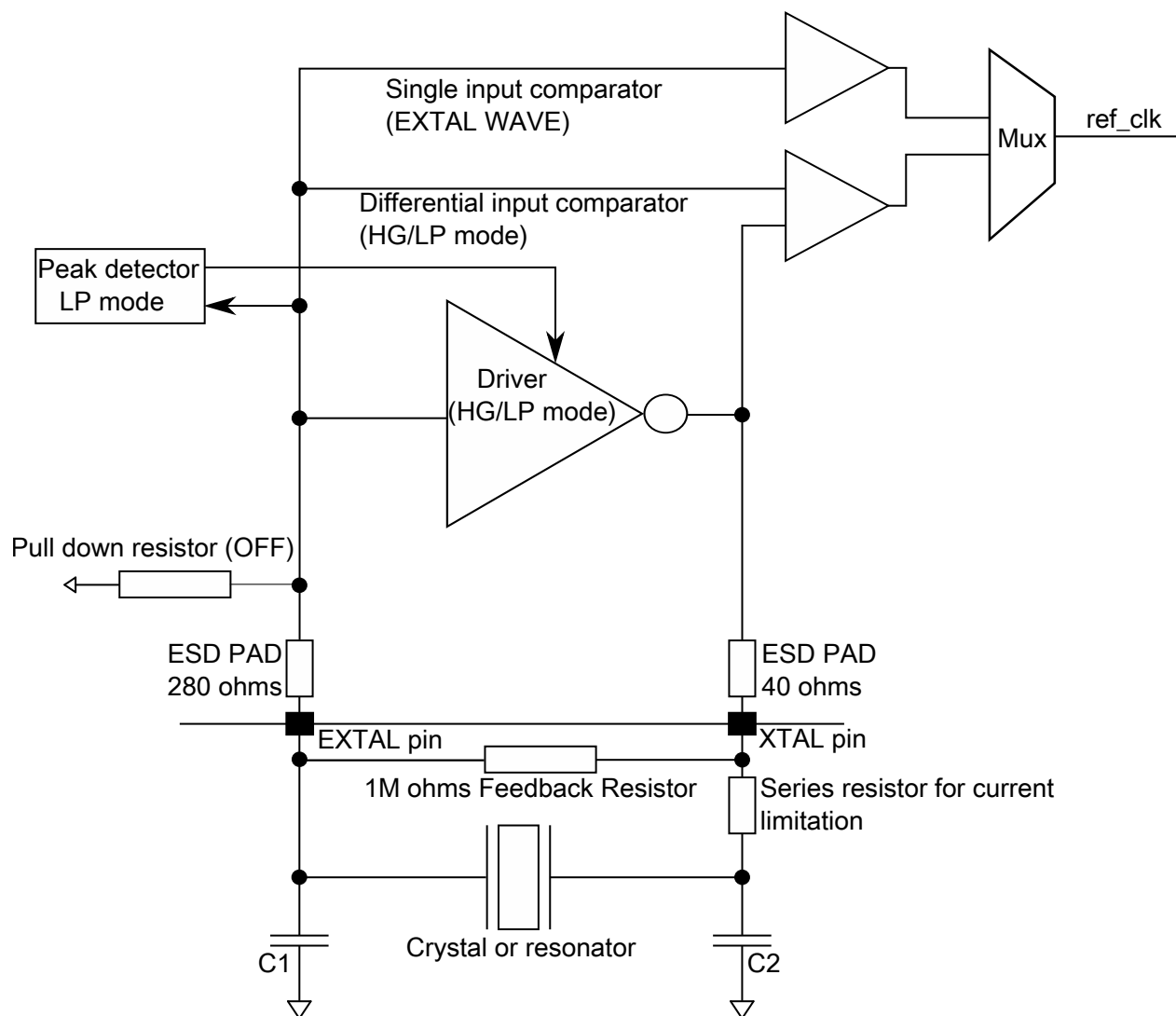


Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	$0.7 \cdot V_{DD}$	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 18. External System Oscillator frequency specifications

Symbol	Description	Min.		Typ.		Max.		Unit	Notes
		S32K14x	S32K11x	S32K14x	S32K11x	S32K14x	S32K11x		
f _{osc_hi}	Oscillator crystal or resonator frequency	4		—		40		MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—		—		50	48	MHz	1
t _{dc_extal}	Input clock duty cycle (external clock mode)	48		50		52		%	1
t _{cst}	Crystal Start-up Time								
	8 MHz low-gain mode (HGO=0)	—		1.5		—		ms	2
	8 MHz high-gain mode (HGO=1)	—		2.5		—			
	40 MHz low-gain mode (HGO=0)	—		2		—			
	40 MHz high-gain mode (HGO=1)	—		2		—			

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

Table 26. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN ¹						HSRUN ¹						RUN/HSRUN ²			
QuadSPI Mode			SDR						SDR						SDR		DDR ³	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	0		0		0		0		0		0		0		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f _{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20 ⁴
SCK Clock Period	t _{SCK}	ns	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	50.0	-	50.0 ⁴	-

Table continues on the next page...

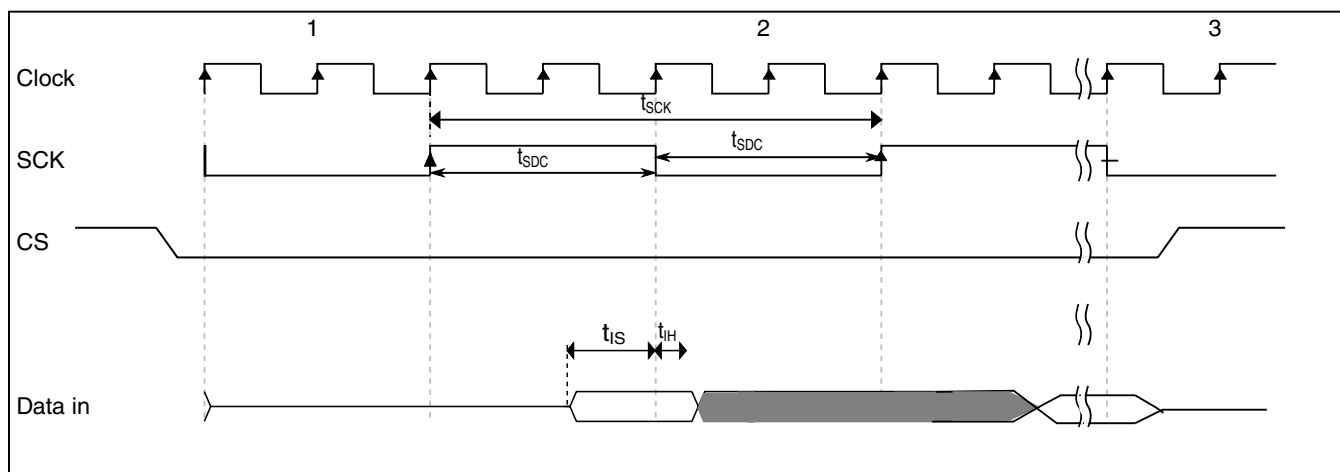


Figure 9. QuadSPI input timing (SDR mode) diagram

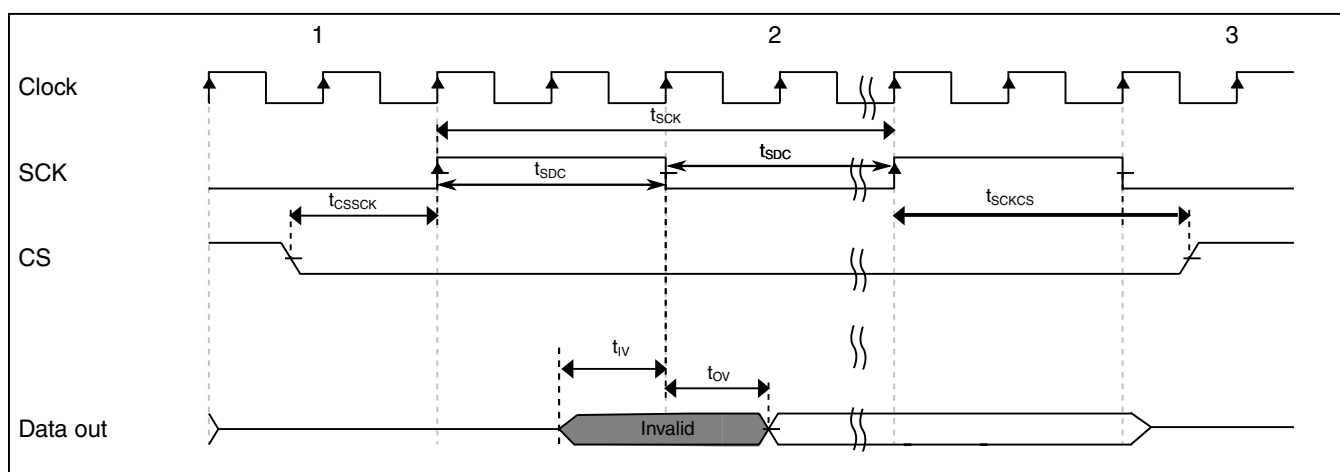
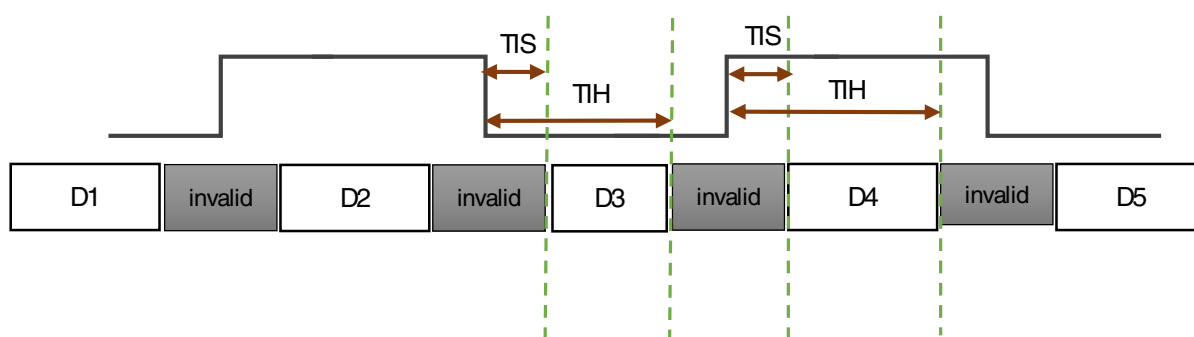


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time

TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

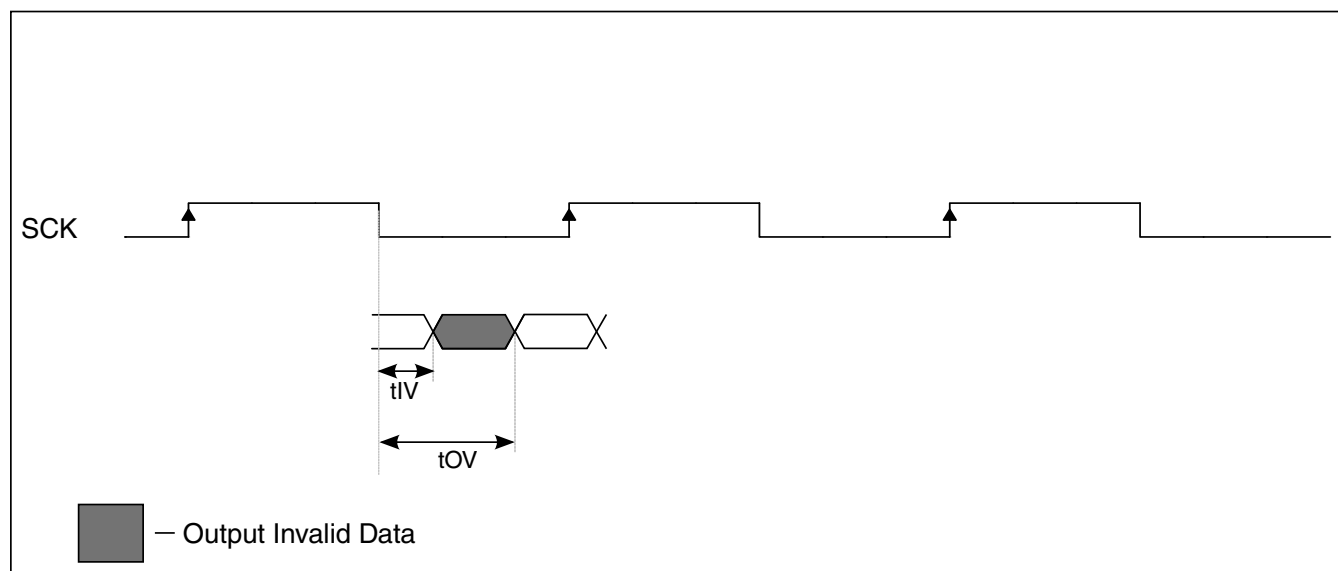


Figure 12. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 27. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		See Voltage and current operating requirements for values	V_{DDA}	See Voltage and current operating requirements for values	V	2
V_{REFL}	ADC reference voltage low		See Voltage and current operating requirements for values	0	See Voltage and current operating requirements for values	mV	2
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedandance	$f_{ADCK} < 4 \text{ MHz}$	—	—	5	k Ω	
R_{SW1}	Channel Selection Switch Impedance		—	0.75	1.2	k Ω	
R_{AD}	Sampling Switch Impedance		—	2	5	k Ω	
C_{P1}	Pin Capacitance		—	10	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	4	pF	
C_S	Sampling capacitance		—	4	5	pF	

Table continues on the next page...

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V _{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I _{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL ⁵	8-bit DAC integral non-linearity	−0.75	—	0.75	LSB ⁶
DNL	8-bit DAC differential non-linearity	−0.5	—	0.5	LSB ⁶
t _{DDAC}	Initialization and switching settling time	—	—	30	μs

1. Difference at input > 200mV
2. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
3. Applied $\pm (30 \text{ mV} + 2 \times V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
4. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3})$.
5. Calculation method used: Linear Regression Least Square Method
6. $1 \text{ LSB} = V_{\text{reference}}/256$

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

6.5.4 FlexCAN electrical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

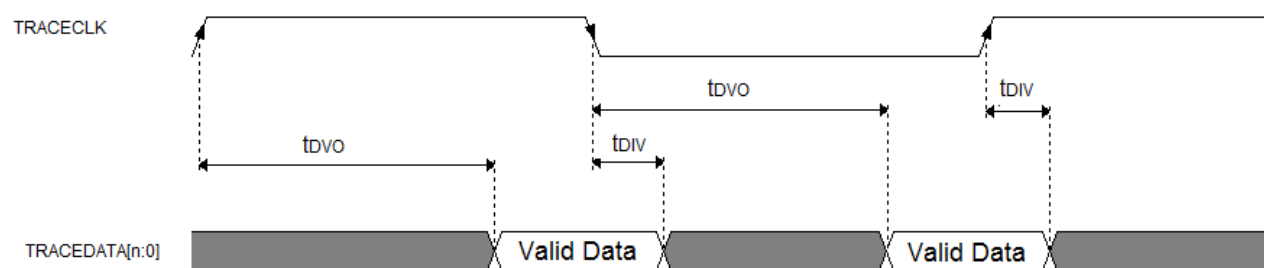


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top ⁷	Natural Convection	ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package ($^{\circ}\text{C}$)
- Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to <http://www.nxp.com> and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 ¹
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100-pin MAPBGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated note 'All the limits defined ...' - Updated parameter 'I_{INJPAD_DC_ABS}', 'V_{IN_DC}', I_{INJSUM_DC_ABS}. - In Table 2, - Updated parameter I_{INJPAD_DC_OP} and I_{INJSUM_DC_OP}. - In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and V_{LVW_HYST} - In Power mode transition operating behaviors, - Added VLPR → VLPS - Added VLPS → VLPR - Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup - In Table 7, updated the specifications for S32K144. - Updated the attachment S32K1xx_Power_Modes_Configuration.xlsx. - In Table 15, removed C_{IN_A}. - In Table 17, - Updated specificatins for g_{mXOSC}. - Removed I_{DDOSC} - In Table 19, - Added parameter ΔF125. - Removed I_{DDFIRC} - In Table 20, - Added parameter ΔF125. - Removed I_{DDSIRC} - In Table 21, removed I_{LPO} - Updated section: Flash memory module (FTFC) electrical specifications - In section: 12-bit ADC operating conditions, - Updated TBDs for I_{DDA_ADC} and TUE in Table 28 - Updated TBDs for I_{DDA_ADC} and TUE in Table 29 - In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. - In section: 12-bit ADC operating conditions, updated Table 27. - In section: CMP with 8-bit DAC electrical specifications, added note 'For comparator IN signals adjacent ...' - In table: Table 32, minor update in footnote 6. - In table: Table 41, updated specifications for S32K146.
5	06 Dec 2017	- Removed S32K148 from 'Caution' - Updated figure: S32K1xx product series comparison for 'EEPROM emulated by FlexRAM' of S32K148 (Added content to footnote) - Added support for LIN protocol version 2.2 A - In Absolute maximum ratings : - Added note 'Unless otherwise ...' - Added parameter 'Added note 'T_{ramp_MCU}' - Updated footnote for 'T_{ramp}' - In Voltage and current operating requirements : - Added footnote 'V_{DD} and V_{DDA} must be shorted ...' against parameter 'V_{DD} - V_{DDA}' - Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' - In Power and ground pins - Added diagrams for 32-QFN and 48-LQFP and footnote below the diagrams. - Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' - In Power mode transition operating behaviors :

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Fixed the typo in R_{SW1} - In LPSPi electrical specifications : - Updated t_{Lead} and t_{Lag} - Added footnote in Figure: LPSPi slave mode timing (CPHA = 0) and Figure: LPSPi slave mode timing (CPHA = 1) - In Thermal characteristics : - Updated the name of table: Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package - Deleted specs for $R_{\theta JC}$ for 32 QFN package - Added '$R_{\theta JCBottom}$'
8	18 June 2018	- In attachment 'S32K1xx_Power_Modes_Configuration': - Updated VLPR peripherals disabled and Peripherals Enabled use case #1, using 4 Mhz for System clock, 2 Mhz for bus clock, and 1Mhz for flash. - Removed S32K116 from Notes - In figure: S32K1xx product series comparison : - Added note 'Availability of peripherals depends on the pin availability ...' - Updated 'Ambient Operation Temperature' row - Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148 - In Ordering information : - Updated figure for 'Y: Optional feature' - Updated footnote 3 - In Power and ground pins : - In figure 'Power diagram', updated V_{Flash} frequency to 3.3 V - In Power mode transition operating behaviors : - Updated footnote for 'VLPS Mode: All clock sources disabled' - In Power consumption : - Added IDD's for S32K116 - Added VLPR Peripherals enabled use case 2 at 125 °C/Typicals - Renamed VLPR 'Peripherals enabled' to 'Peripherals enabled use case 1' - Added footnote 'Data collected using RAM' to VLPR 'Peripherals disabled' and VLPR 'Peripherals enabled use case 1' - Updated VLPS Peripherals enabled at 25 °C/Typicals for S32K142 and S32K144 to 40 μA and 42 μA respectively - Added table 'VLPS additional use-case power consumption at typical conditions' - In DC electrical specifications at 3.3 V Range : - Updated naming conventions - Added specs for GPIO-FAST pad - In DC electrical specifications at 5.0 V Range : - Updated naming conventions - Added specs for GPIO-FAST pad - In AC electrical specifications at 3.3 V range : - Updated naming conventions - Added specs for GPIO-FAST pad - In AC electrical specifications at 5 V range : - Updated naming conventions - Added specs for GPIO-FAST pad - In External System Oscillator electrical specifications : - Clarified description of g_{mXOSC} - Updated V_{IL} max. to 1.15 V - In Fast internal RC Oscillator (FIRC) electrical specifications :