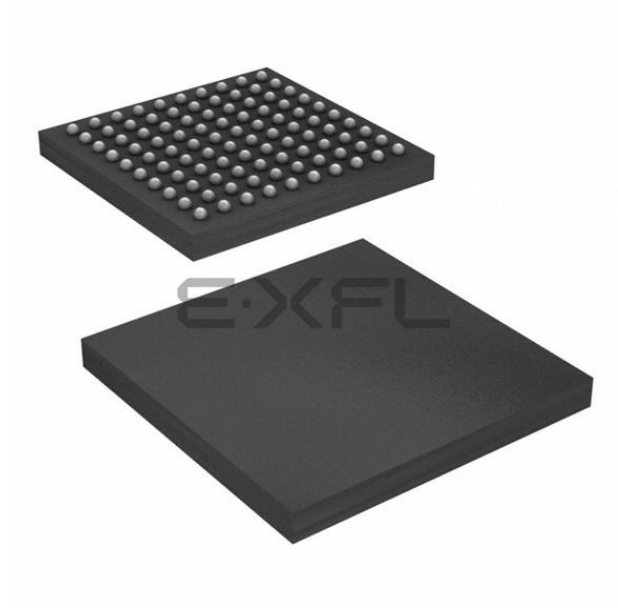


Welcome to E-XFL.COM

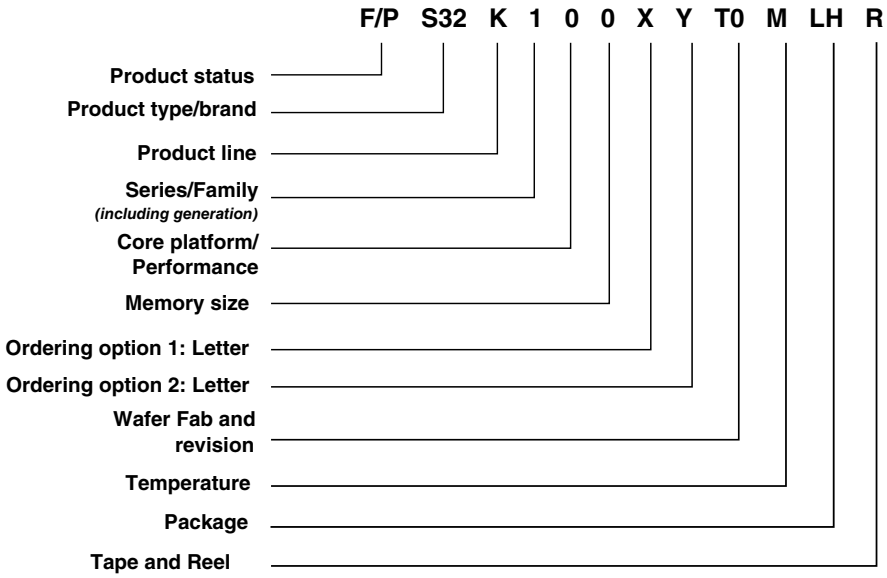
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144hrt0vmhr

3.2 Ordering information



Product status
P: Prototype
F: Qualified

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: Arm Cortex MCUs

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: Arm Cortex M0+
4: Arm Cortex M4F

Memory size

	2	4	6	8
S32K11x			128K	256K
S32K14x	256K	512K	1M	2M

Ordering option
X: Speed
B: 48 MHz without DMA (S32K11x only)
L: 48 MHz with DMA (S32K11x only)
H: 80 MHz
U[1]: 112 MHz (Not valid with M temperature/125C)

Y: Optional feature
R: Base feature set
F: CAN FD, FlexIO
A[1]: CAN FD, FlexIO, Security
E: Ethernet, Serial Audio Interface (S32K148 only)
J[1]: Ethernet, Serial Audio Interface, CAN FD, FlexIO, Security (S32K148 only)

Wafer, Fab and revision
Fx: ATMC[2]
Tx: GF
XX: Flex #[2]

x0: 1st revision

Temperature
V: -40C to 105C
M: -40C to 125C
W: -40C to 150C[2]

Package

Pins	LQFP	QFN	BGA
32	-	FM	-
48	LF	-	-
64	LH	-	-
100	LL	-	MH
144	LQ	-	-
176	LU	-	-

Tape and Reel
T: Trays/Tubes
R: Tape and Reel

1. CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
2. Not supported yet
3. Part numbers no longer offered as standard include:
   Ordering Option X (M:64MHz); Ordering Option Y (N: limited RAM. 16KB for K142, 48KB for K144, 96KB for K146, 192KB for K148 S: Security); Temperature (C: -40C to 85C)

NOTE
Not all part number combinations are available. See S32K1xx_Orderable_Part_Number_List.xlsx attached with the Datasheet for list of standard orderable parts.

Figure 4. Ordering information

4 General

4.1 Absolute maximum ratings

NOTE

- Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.
- Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.
- All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation.
- Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.7 V - 5. 5V input supply voltage	—	-0.3	5.8 [3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8 [3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	—	-3	+3	mA
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to V_{SS}	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	ECU supply ramp rate	—	0.5 V/min	500 V/ms	—
T_{ramp_MCU}[7]	MCU supply ramp rate	—	0.5 V/min	100 V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	165	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$	—	—	6.8 [9]	V

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. 60 s lifetime – No restrictions i.e. The part can switch.

   10 hours lifetime – Device in reset i.e. The part cannot switch.

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.
   - No trace exceeding 1 mm from the protection to the trace or to the ground.
   - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
   - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA)[1]	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 18. External System Oscillator frequency specifications

Symbol	Description	Min.		Typ.		Max.		Unit	Notes
		S32K14x	S32K11x	S32K14x	S32K11x	S32K14x	S32K11x		
f_{osc_hi}	Oscillator crystal or resonator frequency	4		—		40		MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—		—		50	48	MHz	1
t_{dc_extal}	Input clock duty cycle (external clock mode)	48		50		52		%	1
t_{cst}	Crystal Start-up Time								
	8 MHz low-gain mode (HGO=0)	—		1.5		—		ms	2
	8 MHz high-gain mode (HGO=1)	—		2.5		—			
	40 MHz low-gain mode (HGO=0)	—		2		—			
	40 MHz high-gain mode (HGO=1)	—		2		—			

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

Table 26. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	-	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

6.4.2 CMP with 8-bit DAC electrical specifications

Table 31. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs
	-40 - 125 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	

Table continues on the next page...

Table 32. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph} [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14 [7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14 [7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													

Table continues on the next page...

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32[12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock
4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. This is the maximum operating frequency (f_{op}) for LPSPI0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
10. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
11. Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPI instance.
12. Applicable for LPSPI0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.

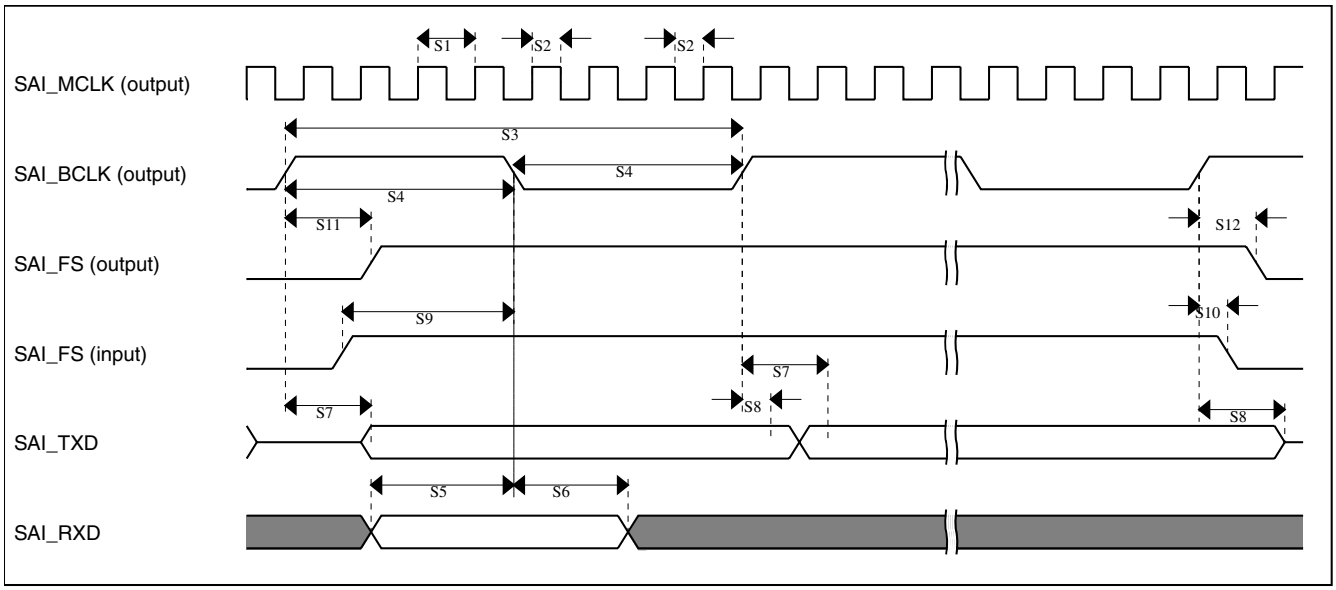


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 36. RMII signal switching specifications (continued)

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

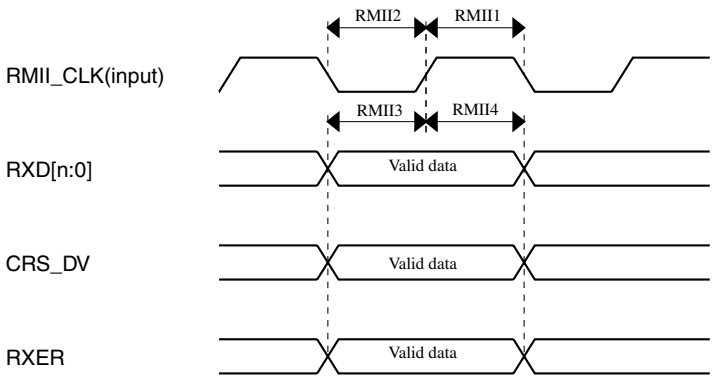


Figure 26. RMII receive diagram

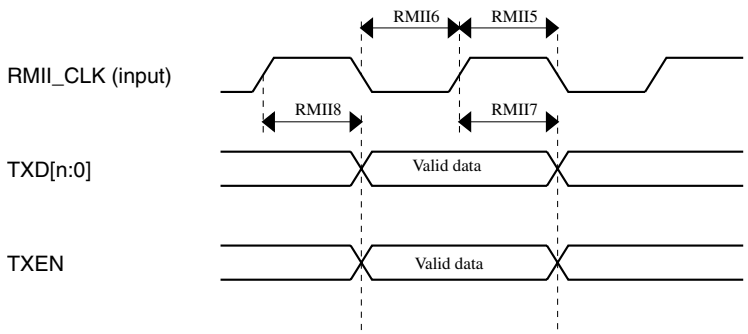


Figure 27. RMII transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 37. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

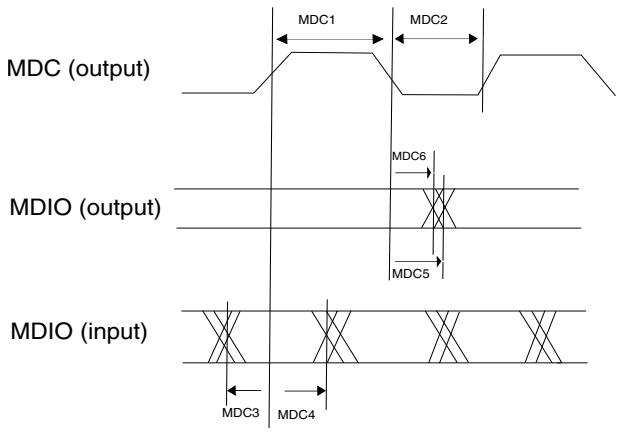


Figure 28. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

Table 40. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
JI	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
			144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnotes V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		• Updated table: AC electrical specifications at 3.3 V range
		• Updated table: AC electrical specifications at 5 V range
		• In table: Standard input pin capacitance
		  • Added footnote to Normal run mode (S32K14x series)
		• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme
		• In table: External System Oscillator electrical specifications
		  • Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz
		  • Removed rows for I_{lk_ext} EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL}
		  • Updated Typ. of R_S low-gain mode
		  • Updated description of R_F, R_S, and V_{PP}
		  • Removed footnote from R_F Feedback resistor
		  • Updated footnote for C_1 C_2 and R_F
		• In table: Table 18
		  • Removed mention of high-frequency
		  • Added HGO 0, 1 information
		• In table: Fast internal RC Oscillator electrical specifications
		  • Updated F_{FIRC}
		  • Updated description of ΔF
		  • Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Updated naming convention of I_{DDFIRC} Supply current
		  • Added footnote to I_{DDFIRC} Supply current
		  • Added footnote to column Parameter
		• In table: Slow internal RC oscillator (SIRC) electrical specifications
		  • Removed V_{DD} Supply current in 2 MHz Mode
		  • Removed footnote and updated description of ΔF
		  • Updated footnote to F_{SIRC} and I_{DDSIRC}
		• In table: SPLL electrical specifications
		  • Added row for F_{SPLL_REF} PLL Reference
		  • Updated naming convention throughout the table
		  • Updated the max value of T_{SPLL_LOCK} Lock detector detection time
		• In table: Flash timing specifications — commands
		  • Added footnotes:
		  • All command times assumes ...
		  • For all EEPROM Emulation terms ...
		  • 'First time' EERAM writes after a POR ...
		  • Removed footnote 'Assumes 25 MHz or ...'
		  • Updated Max of $t_{eewr32bers}$
		  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$
		• In table: Reliability specifications
		  • Removed Typ. values for all parameters
		  • Removed footnote 'Typical values represent ... '
		  • Added footnote 'Any other EEE driver usage ... '
		• Updated QuadSPI AC specifications
		• Removed topic: Reliability, Safety and Security modules
		• In table: 12-bit ADC operating conditions
		  • Updated V_{DDA}

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, ans t_V in HSRUN Mode • Added footnote to 't_{WSPSCK}' • Updated Thermal characteristics for S32K11x
6	31 Jan 2018	• Changed the representation of ARM trademark throughout. • Removed S32K142 from 'Caution' • In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': • No write or erase access to ... • In High-level architecture diagram for the S32K14x family, added the following footnote: • No write or erase access to ... • In High-level architecture diagram for the S32K11x family : • Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block • Updated figure: S32K1xx product series comparison : • Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. • Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. • Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. • Updated Ordering information • Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	• Changed Caution to Notes • Updated the wordings of Notes and removed S32K146 • Added 'Following two are the available ...' • In 'Key features' : • Editorial updates • Updated the note under Power management, Memory and memory interfaces, and Safety and security. • Updated FlexIO under Communications interfaces • Added ENET and SAI under Communications interfaces • Updated Cryptographic Services Engine (CSEc) under 'Safety and security' • In High-level architecture diagram for the S32K14x family : • Minor editorial updates • Updated note 3 • In High-level architecture diagram for the S32K11x family : • Minor editorial updates • In figure: S32K1xx product series comparison : • Editorial updates • Updated Frequency for S32K14x • Updated footnote 4 • Added footnote 5 • In Ordering information : • Renamed section, updated the starting paragraph • Updated the figure • In Voltage and current operating requirements, updated the note • In Power consumption : • Updated specs for S32K146 • Removed section 'Modes configuration', amd moved its content under the fisrt paragraph. • In 12-bit ADC operating conditions :

Table continues on the next page...