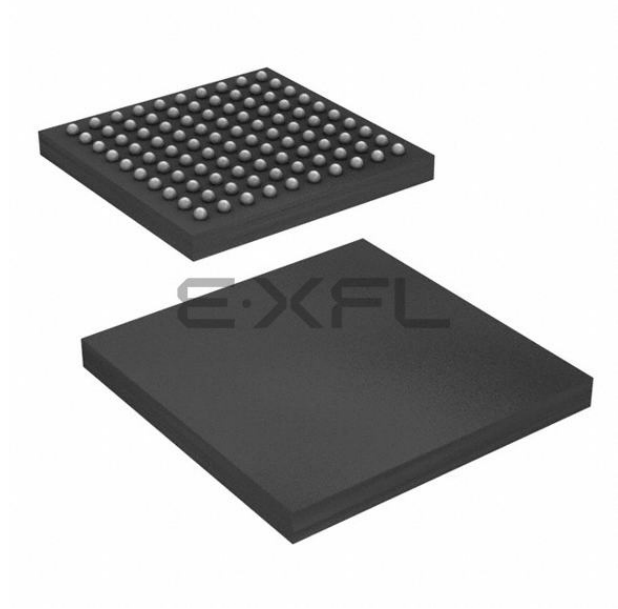

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-MAPBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144hrt0vmht

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

Description Input Multiplexing sheet(s) attached with Reference Manual.

		S32K11x		S32K14x			
	Parameter	K116	K118	K142	K144	K146	K148
	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode)[1]			
System	IEEE-754 FPU	○		●			
System	Cryptographic Services Engine (CSEc)[1]	●		●			
System	CRC module	1x		1x			
System	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
System	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
System	Crossbar	●		●			
System	DMA	●		●			
System	External Watchdog Monitor (EWM)	○		●			
System	Memory Protection Unit (MPU)	●		●			
System	FIRC CMU	●		○			
System	Watchdog	1x		1x			
System	Low power modes	●		●			
System	HSRUN mode[1]	○		●			
System	Number of I/Os	up to 43	up to 58	up to 89		up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
System	Ambient Operation Temperature (T_A)	-40ºC to +105ºC / +125ºC		-40ºC to +105ºC / +125ºC			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB[2]
Memory	Error Correcting Code (ECC)	●		●			
Memory	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	2 KB		4 KB			
Memory	Cache	○		4 KB			
Memory	EEPROM emulated by FlexRAM[1]	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
Memory	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
Timer	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
Timer	Low Power Timer (LPTMR)	1x		1x			
Timer	Real Time Counter (RTC)	1x		1x			
Timer	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
Analog	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)		2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
Communication	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
Communication	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
Communication	Low Power SPI (LPSPI)	1x	2x	2x	3x		
Communication	Low Power I2C (LPI2C)	1x		1x			2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG[4]		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages[5]	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for Boundary Scan Register
5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

4 General

4.1 Absolute maximum ratings

NOTE

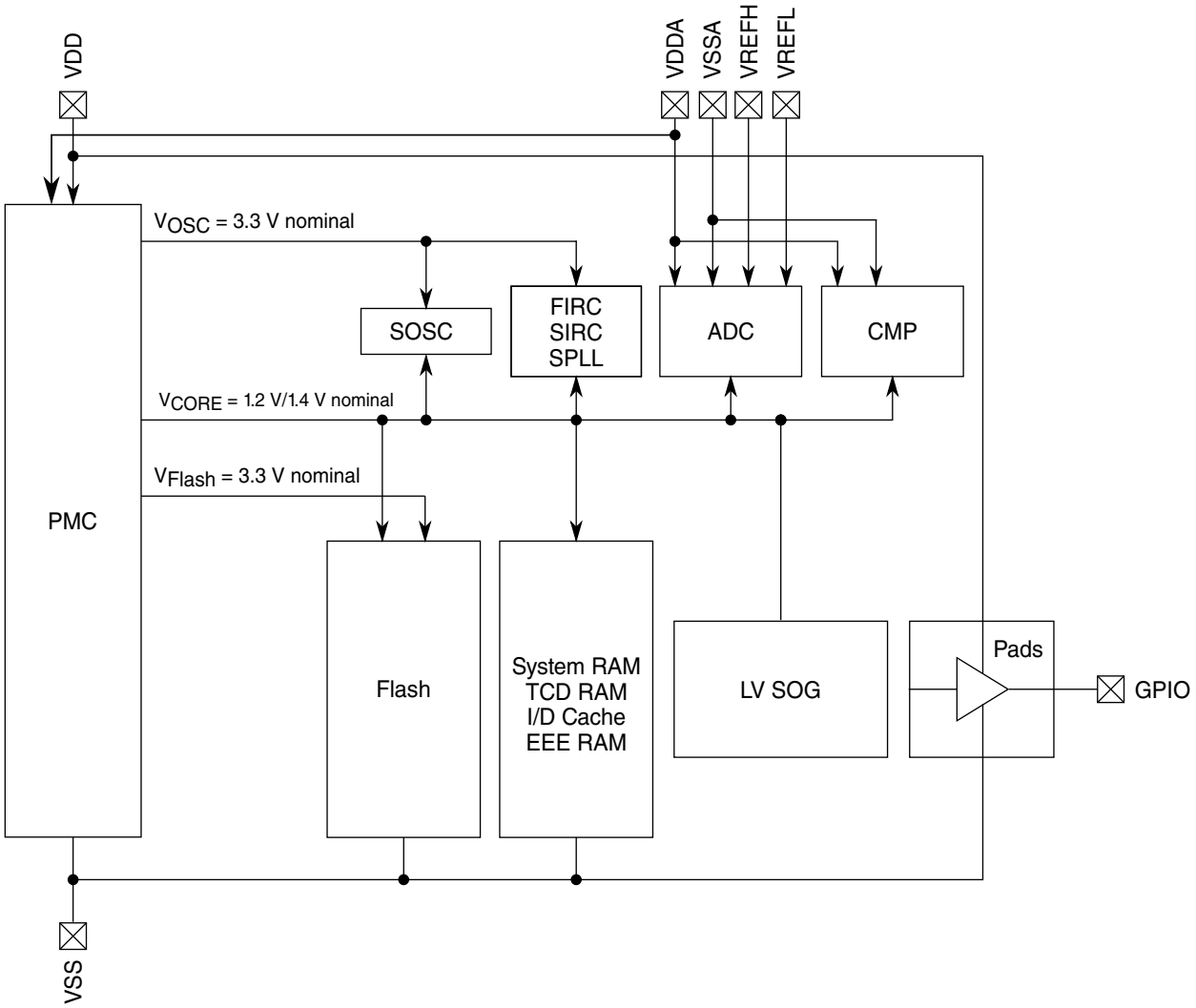
- Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.
- Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.
- All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation.
- Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.7 V - 5. 5V input supply voltage	—	-0.3	5.8 [3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8 [3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	—	-3	+3	mA
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to V_{SS}	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	ECU supply ramp rate	—	0.5 V/min	500 V/ms	—
T_{ramp_MCU}[7]	MCU supply ramp rate	—	0.5 V/min	100 V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	165	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$	—	—	6.8 [9]	V

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. 60 s lifetime – No restrictions i.e. The part can switch.

   10 hours lifetime – Device in reset i.e. The part cannot switch.



*Note: VSSA and VSS are shorted at package level

Figure 6. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1

Table continues on the next page...

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	• Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	µA
		85	TBD	TBD	110	170	180	240	µA
		105	TBD	TBD	230	330	350	490	µA
		125	TBD	TBD	570	680	810	1250	µA
VLPS and LPUART TX/RX	• Clock source: SIRC • Transmiting or receiving continuously using DMA • Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	µA
		85	TBD	TBD	320	400	410	490	µA
		105	TBD	TBD	490	550	600	850	µA
		125	TBD	TBD	890	1070	1250	1960	µA
VLPS and LPUART wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	µA
		85	TBD	TBD	170	240	280	350	µA
		105	TBD	TBD	260	400	480	600	µA
		125	TBD	TBD	530	580	1000	1280	µA
VLPS and LPI2C master	• Clock Source: SIRC • Transmit/receive using DMA • Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	µA
		85	TBD	TBD	880	960	1220	1370	µA
		105	TBD	TBD	1080	1250	1660	2060	µA
		125	TBD	TBD	1970	1980	2860	3690	µA
VLPS and LPI2C slave wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	µA
		85	TBD	TBD	340	340	410	510	µA
		105	TBD	TBD	430	430	610	810	µA
		125	TBD	TBD	740	760	1170	1540	µA
VLPS and LPSPI master	• Clock source: SIRC • Transmit/receive using DMA • Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPIT	• Clock source: SIRC • 1 channel enable • Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	µA
		85	TBD	TBD	190	250	260	320	µA
		105	TBD	TBD	310	410	440	570	µA
		125	TBD	TBD	640	750	910	1280	µA

Table 16. Device clock specifications [1] (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 26. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	0		0		0		0		0		0		0		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f_{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20[4]
SCK Clock Period	t_{SCK}	ns	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	50.0	-	50.0[4]	-

Table continues on the next page...

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32[12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

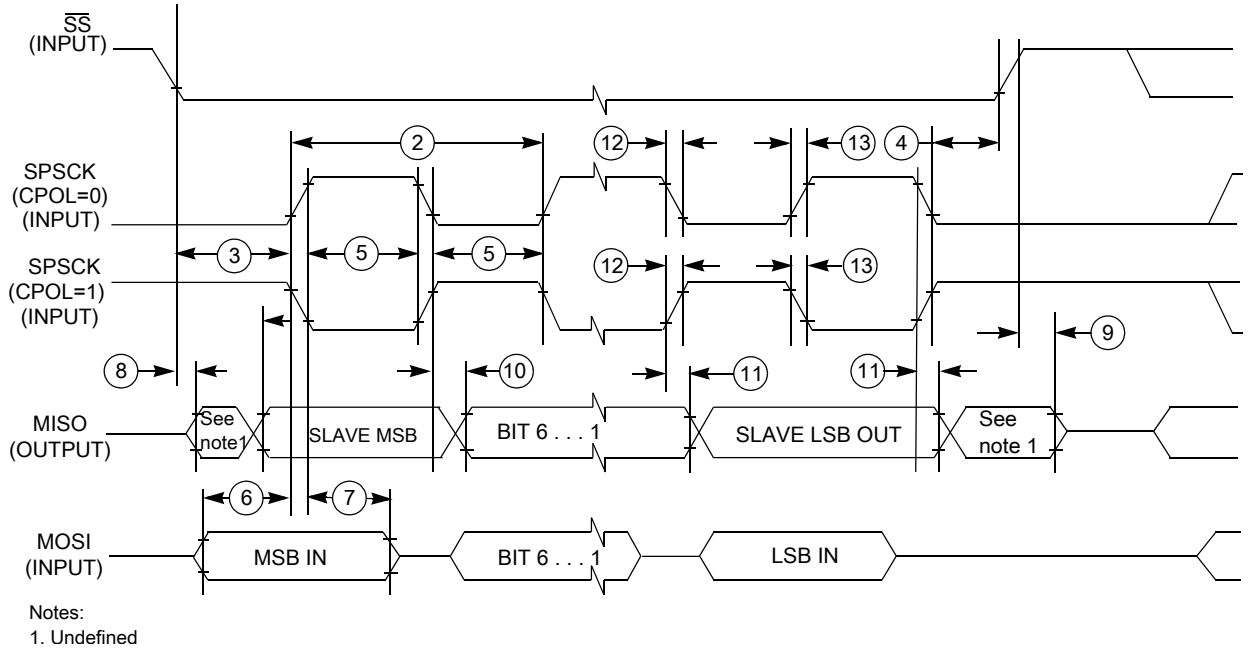


Figure 20. LPSPI slave mode timing (CPHA = 0)

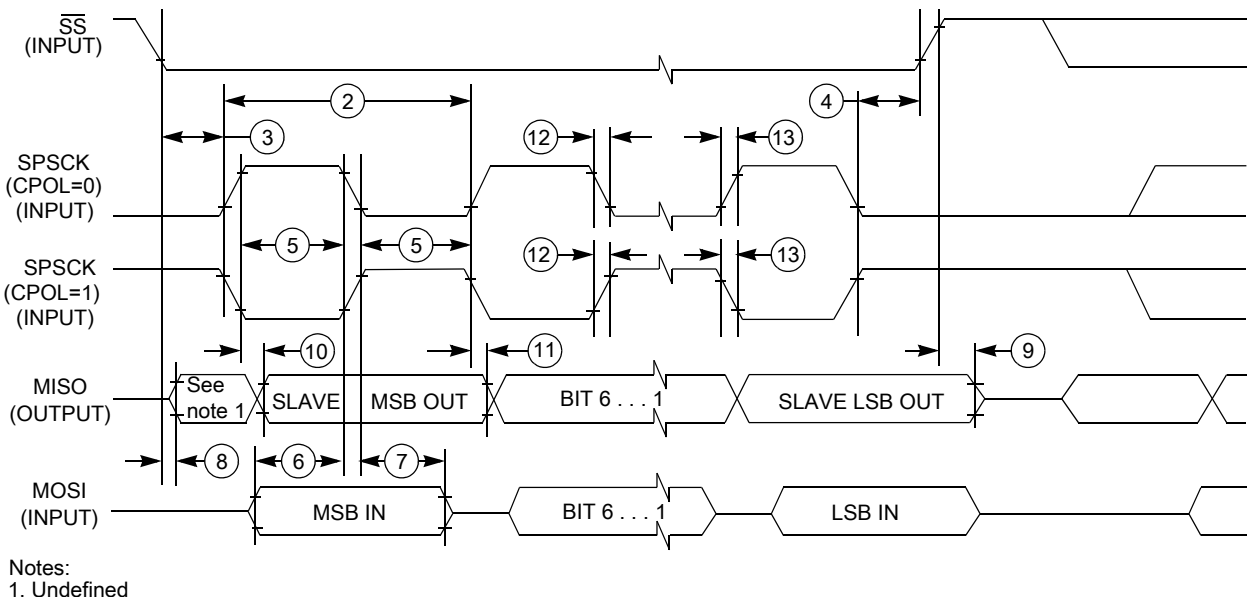


Figure 21. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

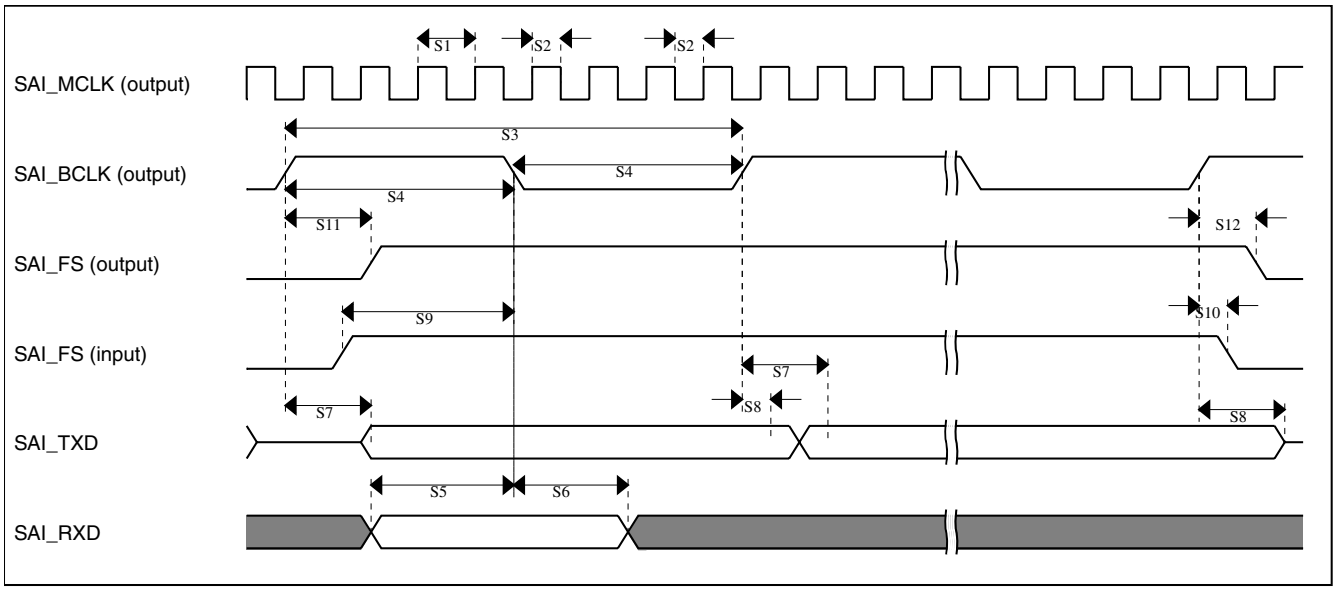


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

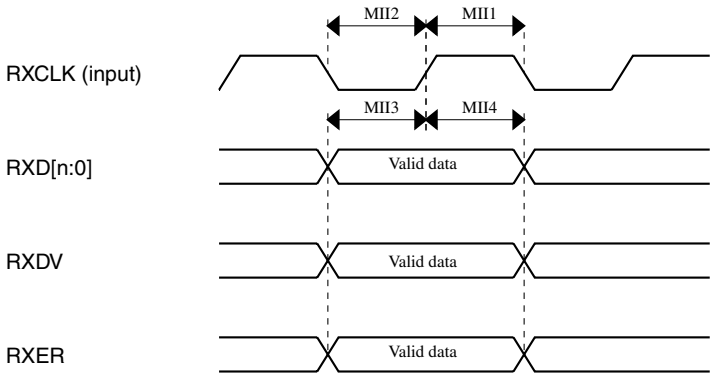


Figure 24. MII receive diagram

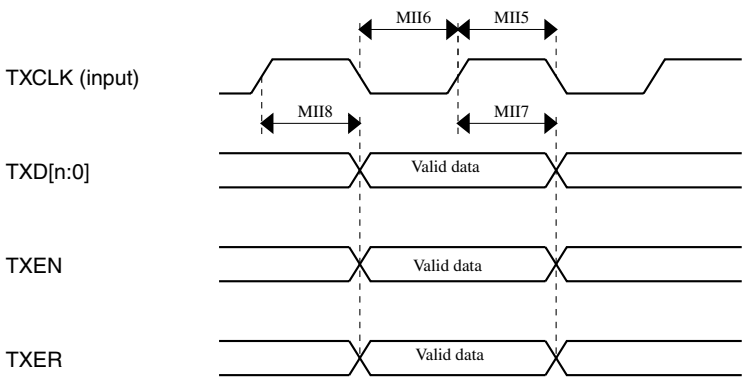


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

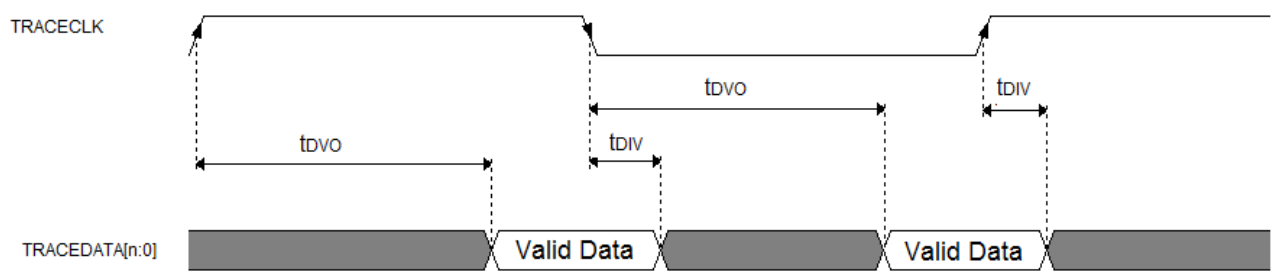


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

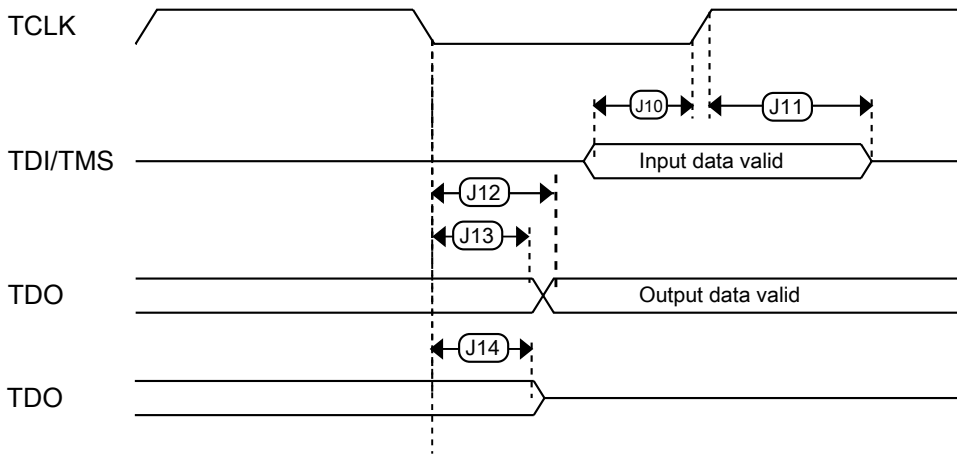


Figure 34. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release

2	03 March 2017	• Updated descpition of QSPI and Clock interfaces in Key Features section
		• Updated figure: High-level architecture diagram for the S32K1xx family
		• Updated figure: S32K1xx product series comparison
		• Added note in section Selecting orderable part number
		• Updated figure: Ordering information
		• In table: Absolute maximum ratings :
		  • Added footnote to I_{INJPAD_DC}
		  • Updated min and max value of I_{INJPAD_DC}
		  • Updated description, max and min values for I_{INJSUM}
		  • Updated $V_{IN\_TRANSIENT}$
		• In table: Voltage and current operating requirements :
		  • Renamed V_{SUP_OFF}
		  • Updated max value of V_{DD_OFF}
		  • Removed V_{INA} and V_{IN}
		  • Added V_{REFH} and V_{REFL}
		  • Updated footnote "Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V ...
		  • Removed I_{NJSUM_AF}
		• Updated footnotes in table Table 4
		• Updated section Power mode transition operating behaviors
		• In table: Power consumption
		  • Added footnote "With PMC_REGSC[CLKBIASDIS] ... "
		  • Updated conditions for VLPR
		  • Removed Idd/MHz for S32K144
		  • Updated numbers for S32K142 and S32K148
		  • Removed use case footnotes
		• In section Modes configuration :
		  • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet'
		• In table: DC electrical specifications at 3.3 V Range :
		  • Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		  • Added footnote to High drive port pins
		• In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, ans t_V in HSRUN Mode • Added footnote to 't_{WSPSCK}' • Updated Thermal characteristics for S32K11x
6	31 Jan 2018	• Changed the representation of ARM trademark throughout. • Removed S32K142 from 'Caution' • In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': • No write or erase access to ... • In High-level architecture diagram for the S32K14x family, added the following footnote: • No write or erase access to ... • In High-level architecture diagram for the S32K11x family : • Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block • Updated figure: S32K1xx product series comparison : • Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. • Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. • Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. • Updated Ordering information • Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	• Changed Caution to Notes • Updated the wordings of Notes and removed S32K146 • Added 'Following two are the available ...' • In 'Key features' : • Editorial updates • Updated the note under Power management, Memory and memory interfaces, and Safety and security. • Updated FlexIO under Communications interfaces • Added ENET and SAI under Communications interfaces • Updated Cryptographic Services Engine (CSEc) under 'Safety and security' • In High-level architecture diagram for the S32K14x family : • Minor editorial updates • Updated note 3 • In High-level architecture diagram for the S32K11x family : • Minor editorial updates • In figure: S32K1xx product series comparison : • Editorial updates • Updated Frequency for S32K14x • Updated footnote 4 • Added footnote 5 • In Ordering information : • Renamed section, updated the starting paragraph • Updated the figure • In Voltage and current operating requirements, updated the note • In Power consumption : • Updated specs for S32K146 • Removed section 'Modes configuration', amd moved its content under the fisrt paragraph. • In 12-bit ADC operating conditions :

Table continues on the next page...

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Revision 8, 06/2018