Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

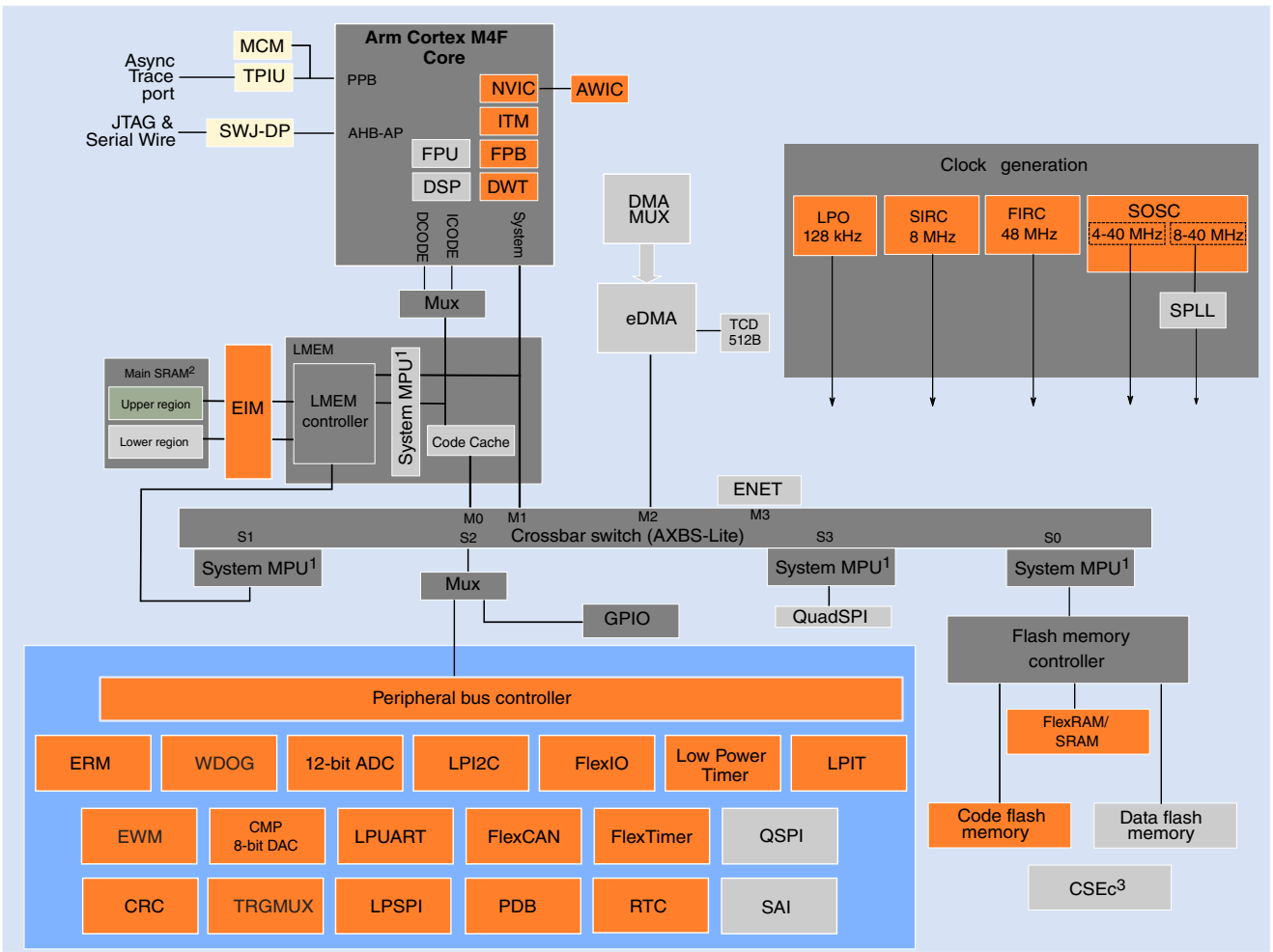
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mat0vlht

1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

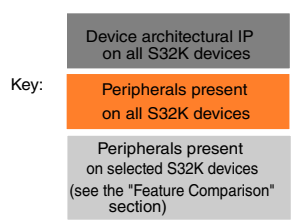
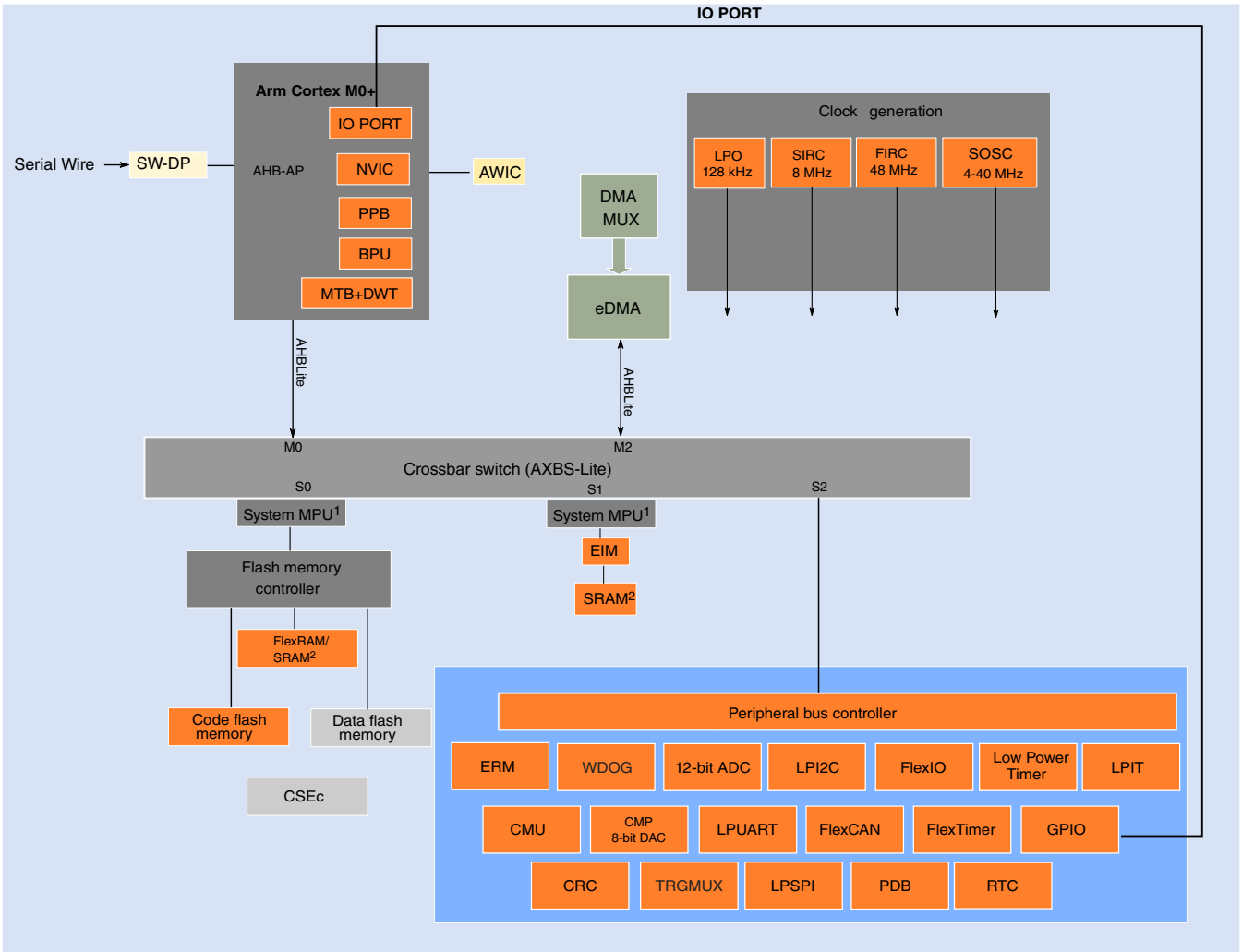


Figure 1. High-level architecture diagram for the S32K14x family



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The Arm M0+ core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

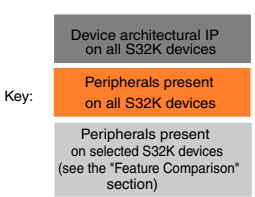


Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the S32K1xx devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

Description Input Multiplexing sheet(s) attached with Reference Manual.

		S32K11x		S32K14x			
	Parameter	K116	K118	K142	K144	K146	K148
	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode)[1]			
System	IEEE-754 FPU	○		●			
System	Cryptographic Services Engine (CSEc)[1]	●		●			
System	CRC module	1x		1x			
System	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
System	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
System	Crossbar	●		●			
System	DMA	●		●			
System	External Watchdog Monitor (EWM)	○		●			
System	Memory Protection Unit (MPU)	●		●			
System	FIRC CMU	●		○			
System	Watchdog	1x		1x			
System	Low power modes	●		●			
System	HSRUN mode[1]	○		●			
System	Number of I/Os	up to 43	up to 58	up to 89		up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
System	Ambient Operation Temperature (T_A)	-40ºC to +105ºC / +125ºC		-40ºC to +105ºC / +125ºC			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB[2]
Memory	Error Correcting Code (ECC)	●		●			
Memory	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	2 KB		4 KB			
Memory	Cache	○		4 KB			
Memory	EEPROM emulated by FlexRAM[1]	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
Memory	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
Timer	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
Timer	Low Power Timer (LPTMR)	1x		1x			
Timer	Real Time Counter (RTC)	1x		1x			
Timer	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
Analog	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)		2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
Communication	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
Communication	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
Communication	Low Power SPI (LPSPI)	1x	2x	2x	3x		
Communication	Low Power I2C (LPI2C)	1x		1x			2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG[4]		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages[5]	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for Boundary Scan Register
5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	85[1]	℃
$T_{J\ C\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	105[1]	℃
$T_{A\ V\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	105[1]	℃
$T_{J\ V\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	125[1]	℃
$T_{A\ M\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	125[2]	℃
$T_{J\ M\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	135[2]	℃

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.
   - No trace exceeding 1 mm from the protection to the trace or to the ground.
   - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
   - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					5
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	6
R_{PD}	Internal pulldown resistors	20		50	kΩ	7

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

6.3.1.1 Flash timing specifications — commands

Table 23. Flash command timing specifications for S32K14x

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	—	2	—	—	—	—	—	—		
		512 KB flash	—	—	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	—	75	µs	
		4 KB flash	—	100	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	95	—	100	µs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	90	225	µs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	250	2125	—	—	—	—	—	—		
		512 KB flash	—	—	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	—	35	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	70	—	—	—	ms	3
		64 KB EEPROM backup	71	—	71	—	71	—	150	—		

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

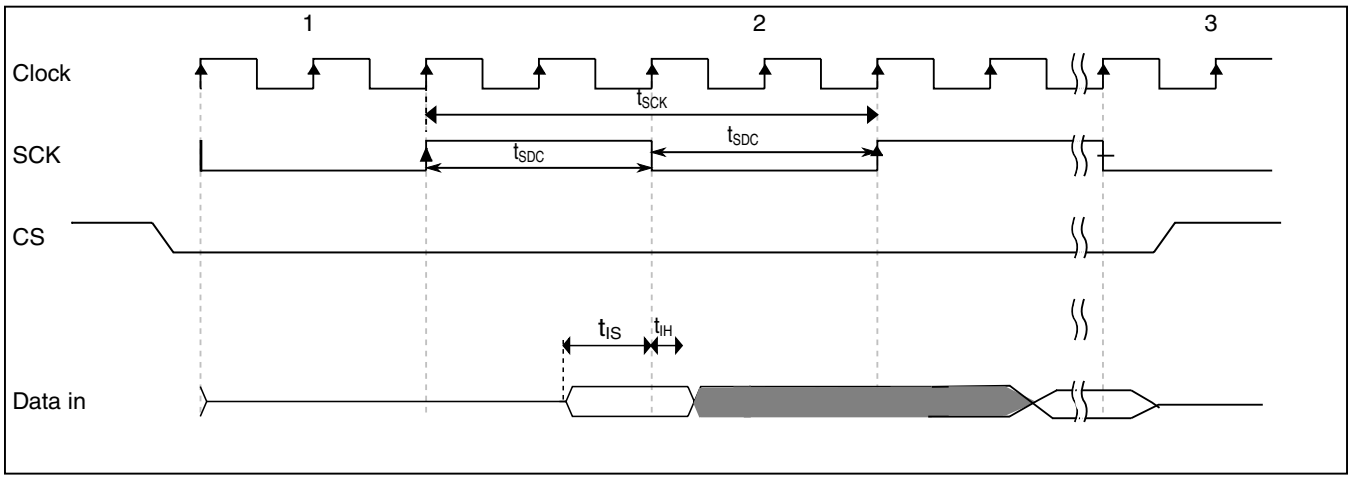


Figure 9. QuadSPI input timing (SDR mode) diagram

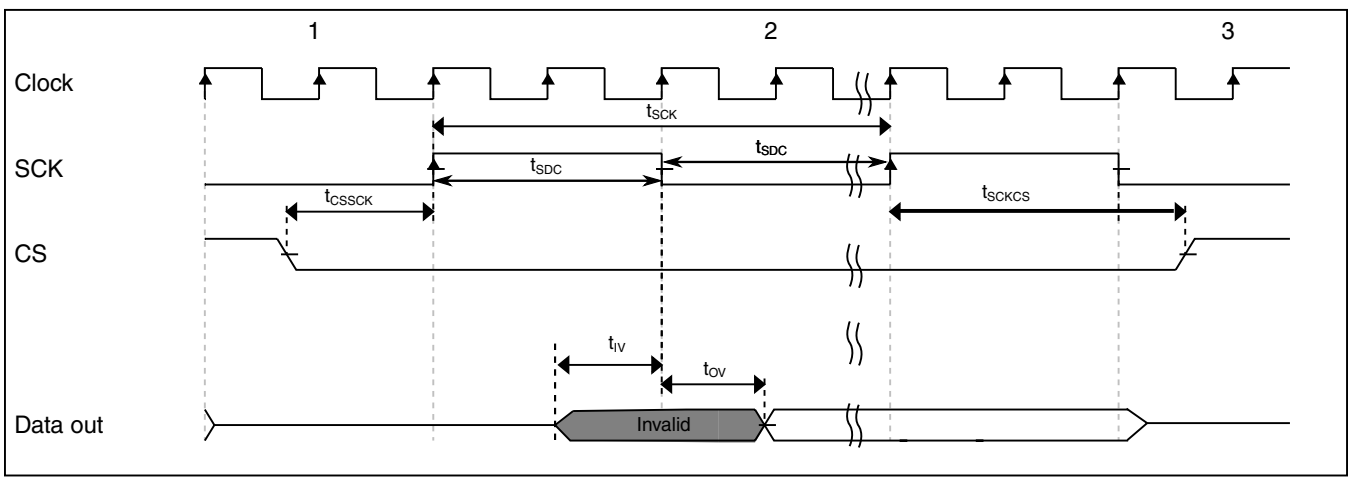
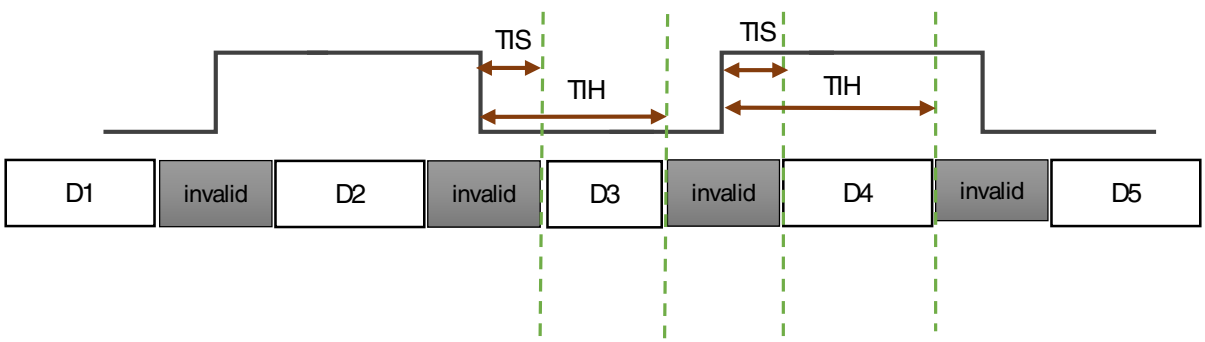


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity	–0.75	—	0.75	LSB[6]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

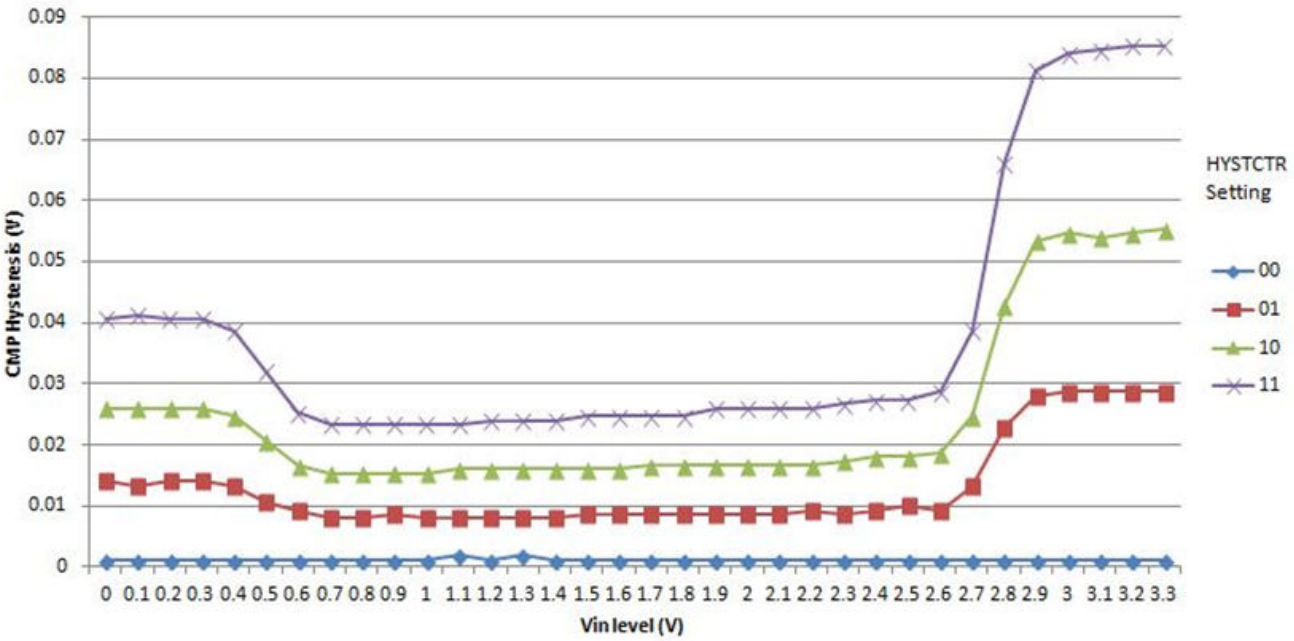


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

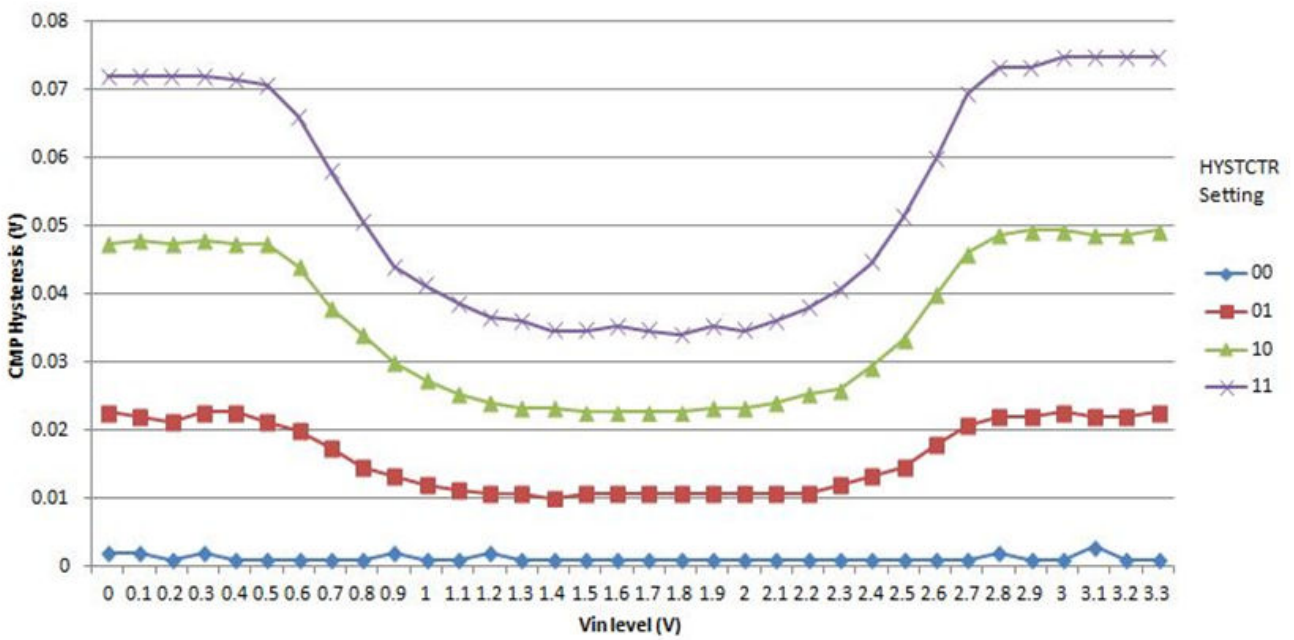


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

Table 32. LPSPI electrical specifications[1] (continued)

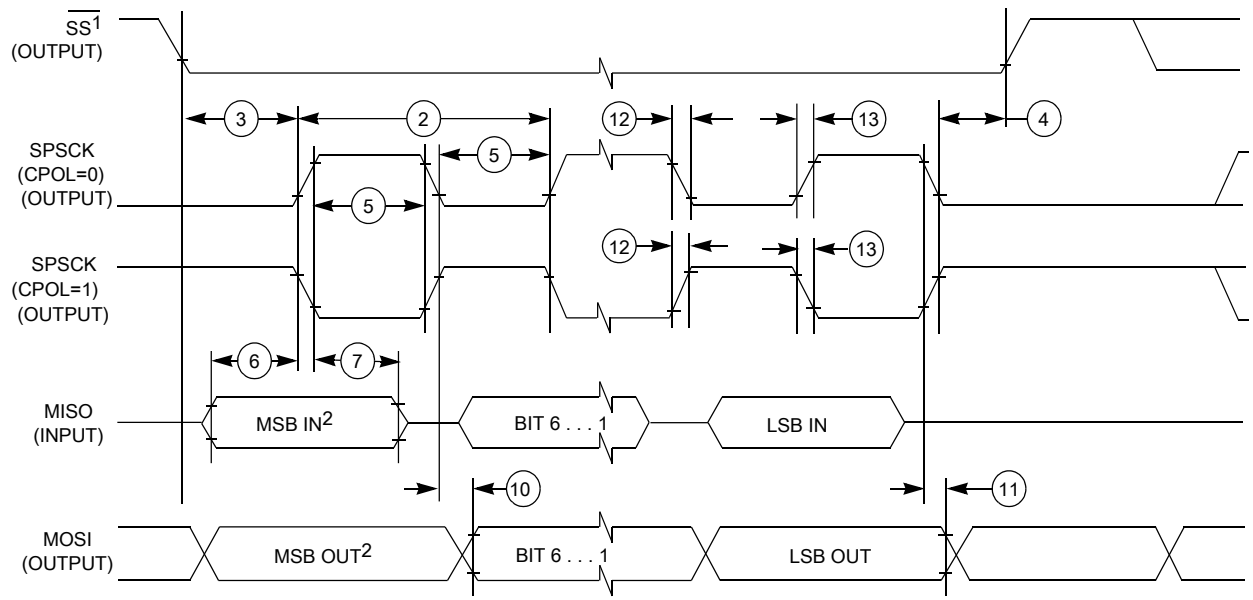
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32[12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

Table 32. LPSPI electrical specifications[1] (continued)

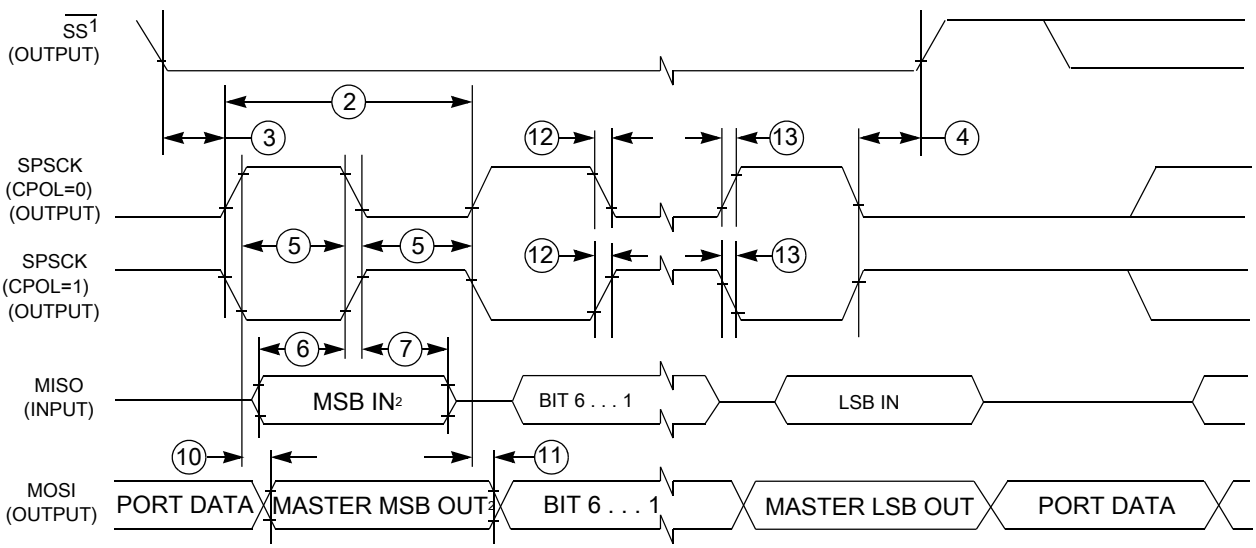
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock
4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. This is the maximum operating frequency (f_{op}) for LPSPI0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
10. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
11. Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPI instance.
12. Applicable for LPSPI0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

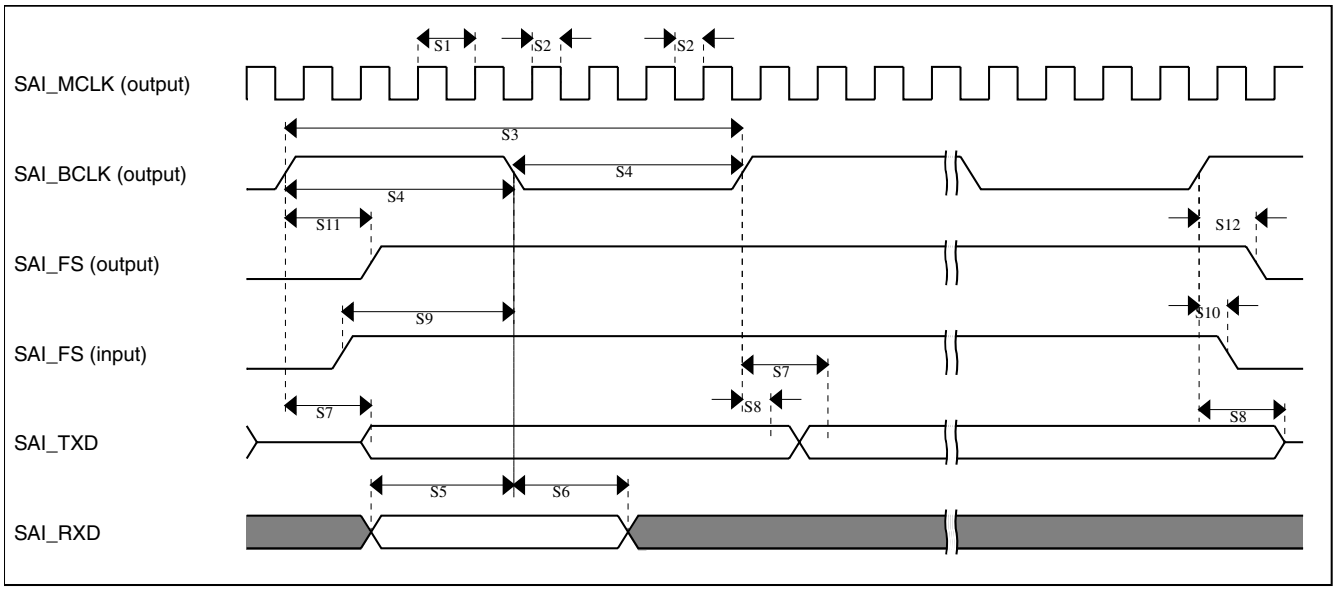


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2]	Single layer board (1s)	$R_{\theta JA}$	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) [1, 2, 3]	Single layer board (1s)	$R_{\theta JMA}$	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Two layer board (2s2p)	$R_{\theta JMA}$	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center[6]	—	Ψ_{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center[7]	—	Ψ_{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, ans t_V in HSRUN Mode • Added footnote to 't_{WSPSCK}' • Updated Thermal characteristics for S32K11x
6	31 Jan 2018	• Changed the representation of ARM trademark throughout. • Removed S32K142 from 'Caution' • In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': • No write or erase access to ... • In High-level architecture diagram for the S32K14x family, added the following footnote: • No write or erase access to ... • In High-level architecture diagram for the S32K11x family : • Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block • Updated figure: S32K1xx product series comparison : • Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. • Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. • Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. • Updated Ordering information • Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	• Changed Caution to Notes • Updated the wordings of Notes and removed S32K146 • Added 'Following two are the available ...' • In 'Key features' : • Editorial updates • Updated the note under Power management, Memory and memory interfaces, and Safety and security. • Updated FlexIO under Communications interfaces • Added ENET and SAI under Communications interfaces • Updated Cryptographic Services Engine (CSEc) under 'Safety and security' • In High-level architecture diagram for the S32K14x family : • Minor editorial updates • Updated note 3 • In High-level architecture diagram for the S32K11x family : • Minor editorial updates • In figure: S32K1xx product series comparison : • Editorial updates • Updated Frequency for S32K14x • Updated footnote 4 • Added footnote 5 • In Ordering information : • Renamed section, updated the starting paragraph • Updated the figure • In Voltage and current operating requirements, updated the note • In Power consumption : • Updated specs for S32K146 • Removed section 'Modes configuration', amd moved its content under the fisrt paragraph. • In 12-bit ADC operating conditions :

Table continues on the next page...