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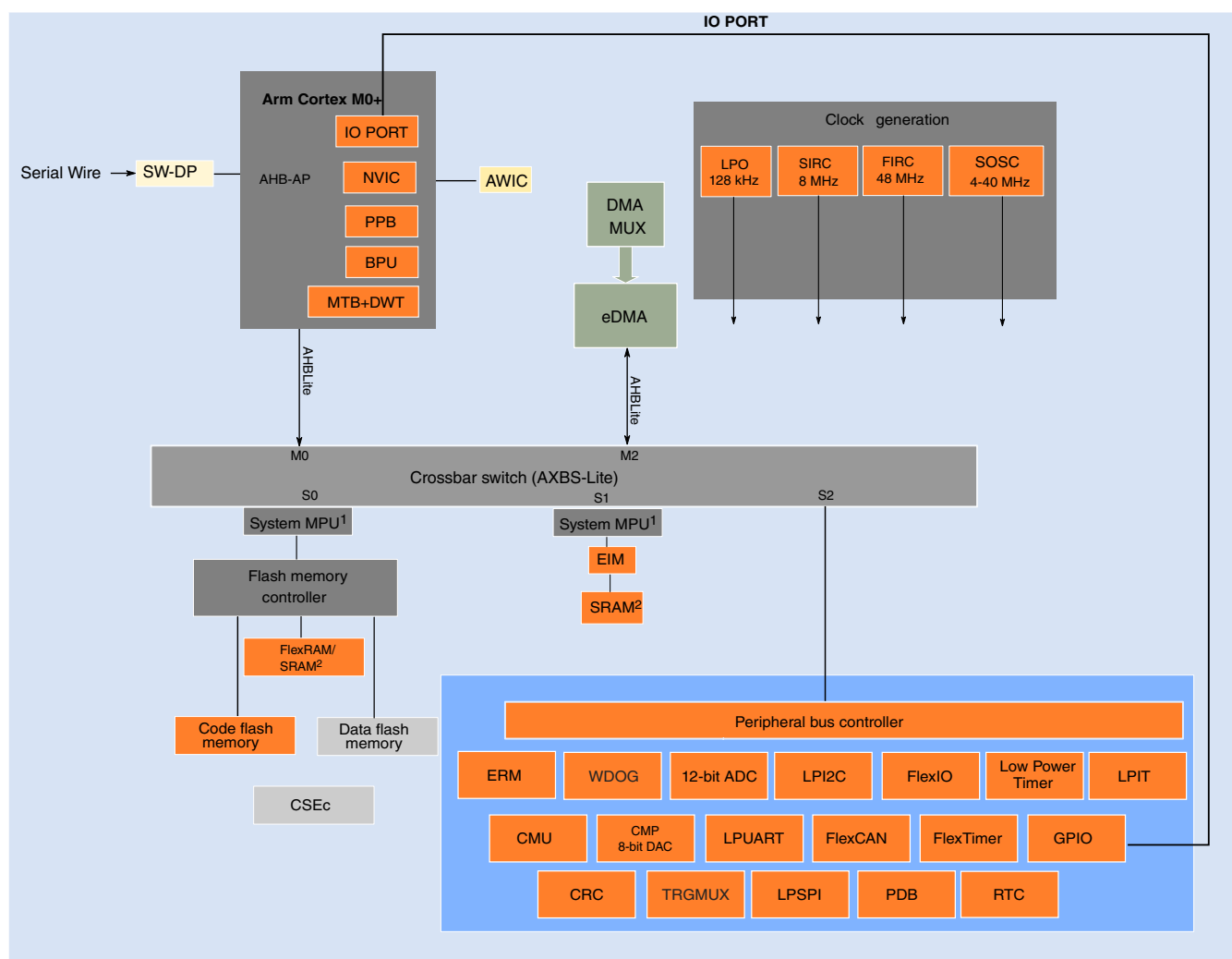
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mft0cllt

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1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The Arm M0+ core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

Key:

Device architectural IP on all S32K devices
Peripherals present on all S32K devices
Peripherals present on selected S32K devices (see the "Feature Comparison" section)

Figure 2. High-level architecture diagram for the S32K11x family

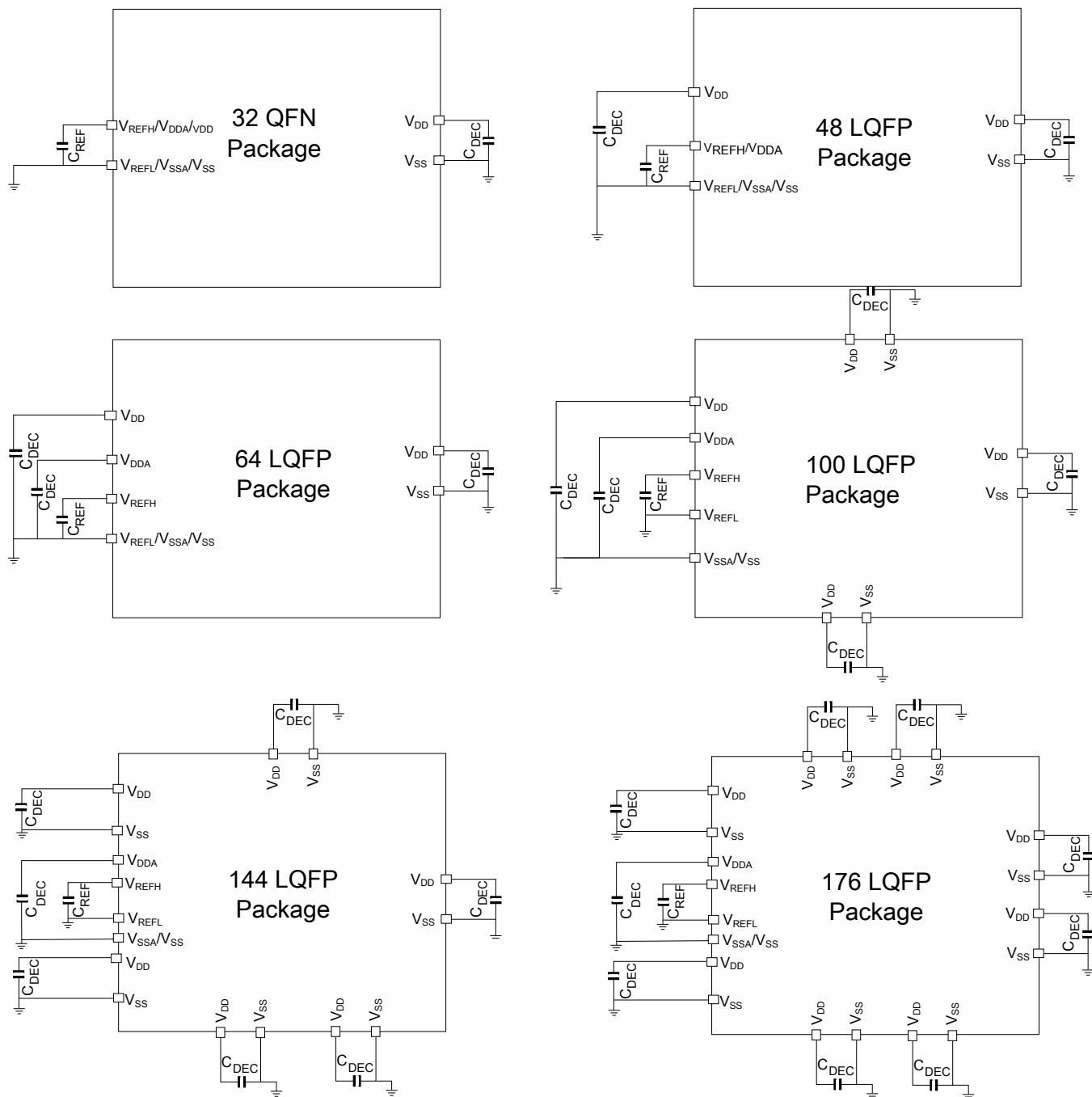
2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the S32K1xx devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling

Table 7. Power consumption (Typicals unless stated otherwise) ¹

Chip/Device	Ambient Temperature (°C)		VLPS (μA) ²		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ³		IDD/MHz (μA/MHz) ⁴
			Peripherals disabled ⁵	Peripherals enabled	Peripherals disabled ⁶	Peripherals enabled use case 1 ⁶	Peripherals enabled use case 2 ⁷			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
S32K116	25	Typ	26	40	1.05	1.07	TBD	6.3	7.2	11.8	20.3	NA						245
	85	Typ	76	93	1.1	1.11	TBD	6.6	7.5	12	20.6							251
		Max	287	300	1.39	1.4	NA	8	8.9	13.4	22.1							279
	105	Typ	139	164	1.15	1.16	TBD	6.8	7.7	12.3	20.8							255
		Max	590	603	1.68	1.69	NA	9.2	10.1	14.5	23.1							302
	125	Typ	NA	NA	NA	NA	TBD	NA	NA	NA	NA							NA
		Max	891	904	2.02	2.04	NA	10.4	11.3	15.6	24.1							325
S32K118	25	Typ	26	38	1.9	2.5	TBD	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
S32K142	25	Typ	29	40	1.17	1.21	2.19	6.4	7.4	17.3	24.6	24.5	31.3	28.8	37.5	40.5	52.2	360
	85	Typ	128	137	1.48	1.51	2.31	7	8	17.6	24.9	25	31.6	29.1	37.7	41.1	52.5	364
		Max	335	360	1.87	1.89	NA	8.6	9.4	22	28.2	26.9	33.5	32	40	44	55.6	400
	105	Typ	240	257	1.58	1.61	2.44	7.6	8.3	18.3	25.7	25.5	31.9	29.8	38	41.5	53.1	373
		Max	740	791	2.32	2.34	NA	9.9	10.9	23.1	30.2	27.8	35.3	33.8	40.7	44.9	57.4	423
	125	Typ	NA	NA	NA	NA	2.84	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

Table continues on the next page...

I/O parameters

- Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
- When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
- Measured at input $V = V_{SS}$
- Measured at input $V = V_{DD}$

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	$0.65 \times V_{DD}$	—	$V_{DD} + 0.3$	V	1
V_{il}	Input Buffer Low Voltage	$V_{SS} - 0.3$	—	$0.35 \times V_{DD}$	V	2
V_{hys}	Input Buffer Hysteresis	$0.06 \times V_{DD}$	—	—	V	
I_{ohGPIO} $I_{ohGPIO-HD_DSE_0}$	I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$	5	—	—	mA	
I_{olGPIO} $I_{olGPIO-HD_DSE_0}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	5	—	—	mA	
$I_{ohGPIO-HD_DSE_1}$	I/O current source capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	20	—	—	mA	3
$I_{olGPIO-HD_DSE_1}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	20	—	—	mA	3
$I_{ohGPIO-FAST_DSE_0}$	I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	14.0	—	—	mA	4
$I_{olGPIO-FAST_DSE_0}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	14.5	—	—	mA	4
$I_{ohGPIO-FAST_DSE_1}$	I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	21	—	—	mA	4
$I_{olGPIO-FAST_DSE_1}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at $V_{DD} = 5.5 \text{ V}$					5
	All pins other than high drive port pins		0.005	0.5	μA	
	High drive port pins		0.010	0.5	μA	
R_{PU}	Internal pullup resistors	20		50	$k\Omega$	6
R_{PD}	Internal pulldown resistors	20		50	$k\Omega$	7

- For reset pads, same V_{ih} levels are applicable
- For reset pads, same V_{il} levels are applicable
- The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
- For reference only. Run simulations with the IBIS model and custom board for accurate results.

**Table 17. External System Oscillator electrical specifications
(continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC} > 5 * gm_crit$. The gm_crit is defined as:

$$gm_crit = 4 * ESR * (2\pi F)^2 * (C_0 + C_L)^2$$

where:

- g_{mXOSC} is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2 / (C_1 + C_2)]$
- C_s is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

- When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
 - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

6.3.1.1 Flash timing specifications — commands

Table 23. Flash command timing specifications for S32K14x

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	—	2	—	—	—	—	—	—		
		512 KB flash	—	—	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	—	75	μ s	
		4 KB flash	—	100	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	95	—	100	μ s	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	90	225	μ s	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	250	2125	—	—	—	—	—	—		
		512 KB flash	—	—	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	—	30	μ s	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	90	—	μ s	
t_{ersall}	Erase All Blocks execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	—	35	—	35	μ s	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	70	—	—	—	ms	3
		64 KB EEPROM backup	71	—	71	—	71	—	150	—		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description ¹		S32K116		S32K118		Unit		Notes
			Typ	Max	Typ	Max			
t _{eewr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	μs		3·4
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	200	550	200	550	μs		4·5·6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550			
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550			
t _{quickwrClnup}	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms		7

1. All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	—	—	years	1
η _{nvmcycp}	Cycling endurance	1 K	—	—	cycles	2, 3

Table continues on the next page...

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging. ⁵ Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. ⁵ Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

1. Typical values assume $V_{\text{DDA}} = 5 \text{ V}$, $\text{Temp} = 25 \text{ }^{\circ}\text{C}$, $f_{\text{ADCK}} = 40 \text{ MHz}$, $R_{\text{AS}} = 20 \text{ } \Omega$, and $C_{\text{AS}} = 10 \text{ nF}$ unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA} , and V_{REFL} is internally tied to V_{SS} . To get maximum performance, reference supply quality should be better than SAR ADC. See application note [AN5032](#) for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual*.
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'

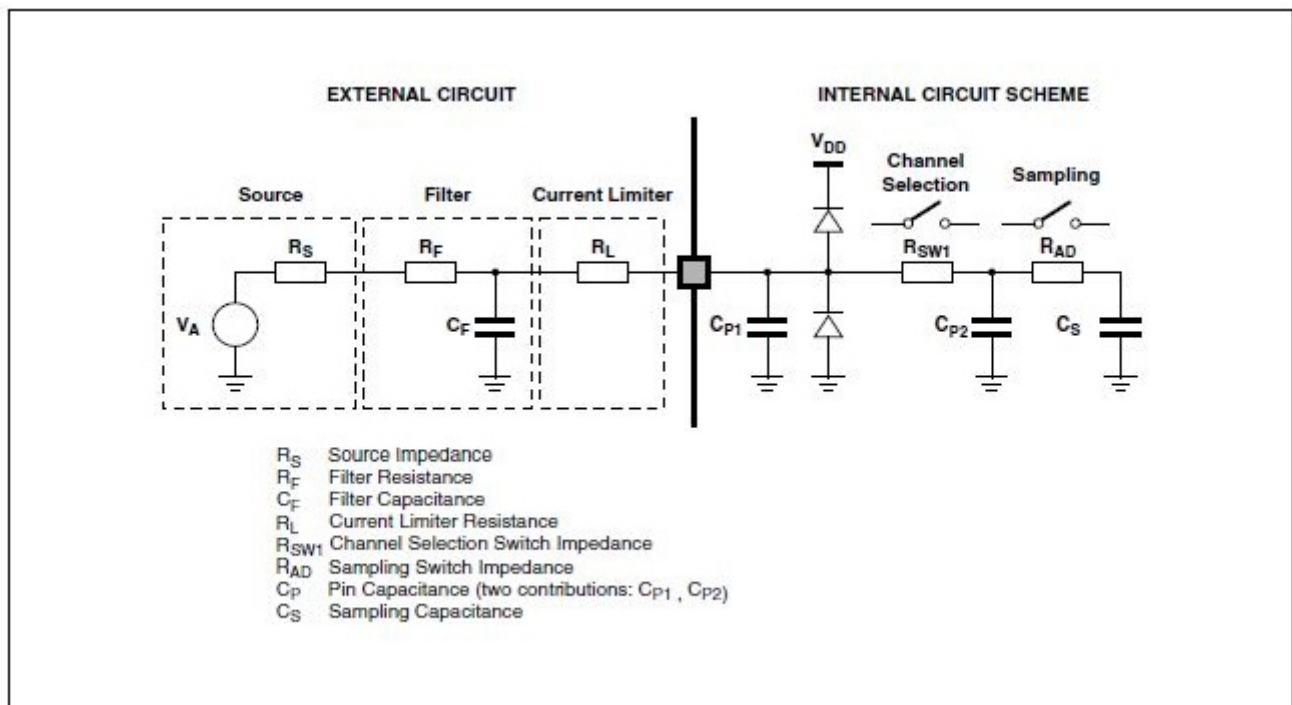
**Figure 13. ADC input impedance equivalency diagram**

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the <i>Reference Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB ⁵	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 40$ MHz, $R_{AS}=20$ Ω, and $C_{AS}=10$ nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Table 32. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t _a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t _{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
10	t _v	Data valid (after SPSCCK edge)	Slave	-	30	-	39	-	26	-	36 ¹¹ 31 ¹²	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback ⁵	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) ⁶	-	8	-	10	-	7	-	9	-	44	-	44	
11	t _{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback ⁵	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) ⁶	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	t _{RI/FI}	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		
			Master Loopback(slow) ⁶	-		-		-		-		-		-		
13	t _{RO/FO}	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		

Table continues on the next page...

Table 32. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master Loopback(slow) ⁶	-		-		-		-		-		-		

- Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
- While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
- f_{periph} = LPSPI peripheral clock
- $t_{\text{periph}} = 1/f_{\text{periph}}$
- Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
- Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
- This is the maximum operating frequency (f_{op}) for LPSPI0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
- Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
- Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
- While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
- Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPI instance.
- Applicable for LPSPI0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.

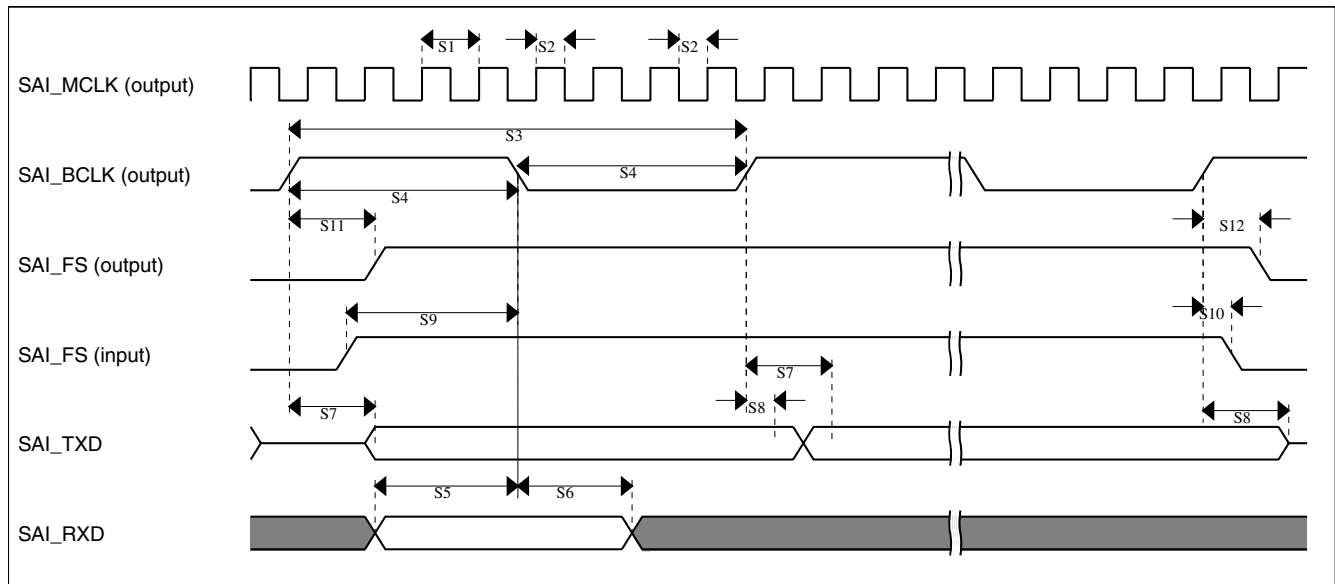


Figure 22. SAI Timing — Master modes

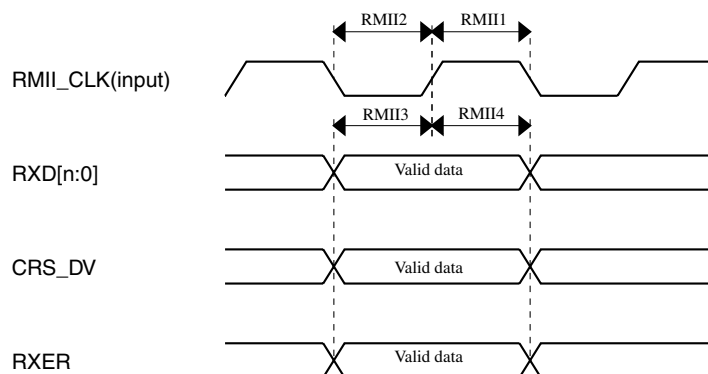
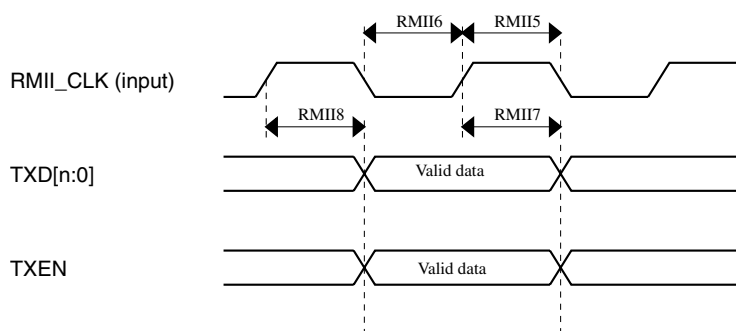
Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14 ¹	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

**Table 36. RMI signal switching specifications
(continued)**

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

**Figure 26. RMI receive diagram****Figure 27. RMI transmit diagram**

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

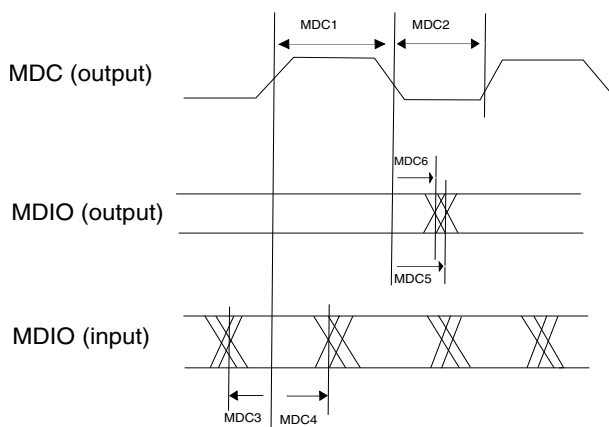
Table 37. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

**Figure 28. MII/RMII serial management channel timing diagram**

6.5.7 Clockout frequency

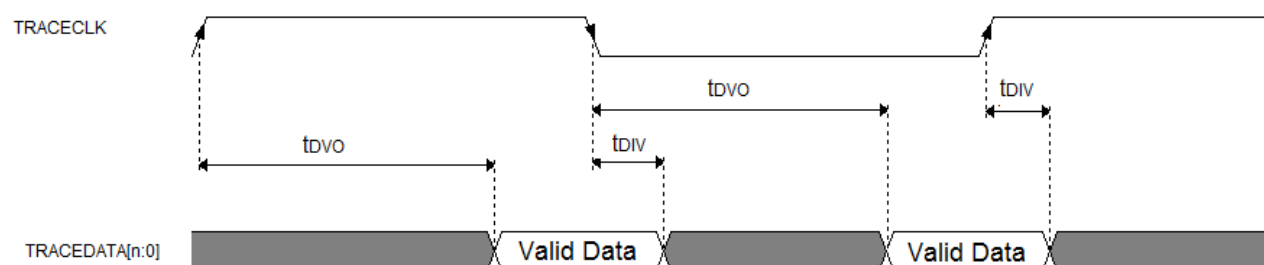
Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specifications

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

**Figure 31. TRACE CLKOUT specifications**

6.6.3 JTAG electrical specifications

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection) ¹	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min) ¹	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	R _{θJA}	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2, 3}	Four layer board (2s2p)	R _{θJA}	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 2, 3}	Single layer board (1s)	R _{θJMA}	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Two layer board (2s2p)	R _{θJMA}	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board ⁴	—	R _{θJB}	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case ⁵	—	R _{θJC}	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center ⁶	—	Ψ _{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center ⁷	—	Ψ _{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to <http://www.nxp.com> and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 ¹
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100-pin MAPBGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	- Updated description of QSPI and Clock interfaces in Key Features section - Updated figure: High-level architecture diagram for the S32K1xx family - Updated figure: S32K1xx product series comparison - Added note in section Selecting orderable part number - Updated figure: Ordering information - In table: Absolute maximum ratings : - Added footnote to I_{INJPAD_DC} - Updated min and max value of I_{INJPAD_DC} - Updated description, max and min values for I_{INJSUM} - Updated $V_{IN_TRANSIENT}$ - In table: Voltage and current operating requirements : - Renamed V_{SUP_OFF} - Updated max value of V_{DD_OFF} - Removed V_{INA} and V_{IN} - Added V_{REFH} and V_{REFL} - Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." - Removed I_{NJSUM_AF} - Updated footnotes in table Table 4 - Updated section Power mode transition operating behaviors - In table: Power consumption - Added footnote "With PMC_REGSC[CLKBIASDIS] ..." - Updated conditions for VLPR - Removed I_{dd}/MHz for S32K144 - Updated numbers for S32K142 and S32K148 - Removed use case footnotes - In section Modes configuration : - Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' - In table: DC electrical specifications at 3.3 V Range : - Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage - Added footnote to High drive port pins - In table: DC electrical specifications at 5.0 V Range :

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