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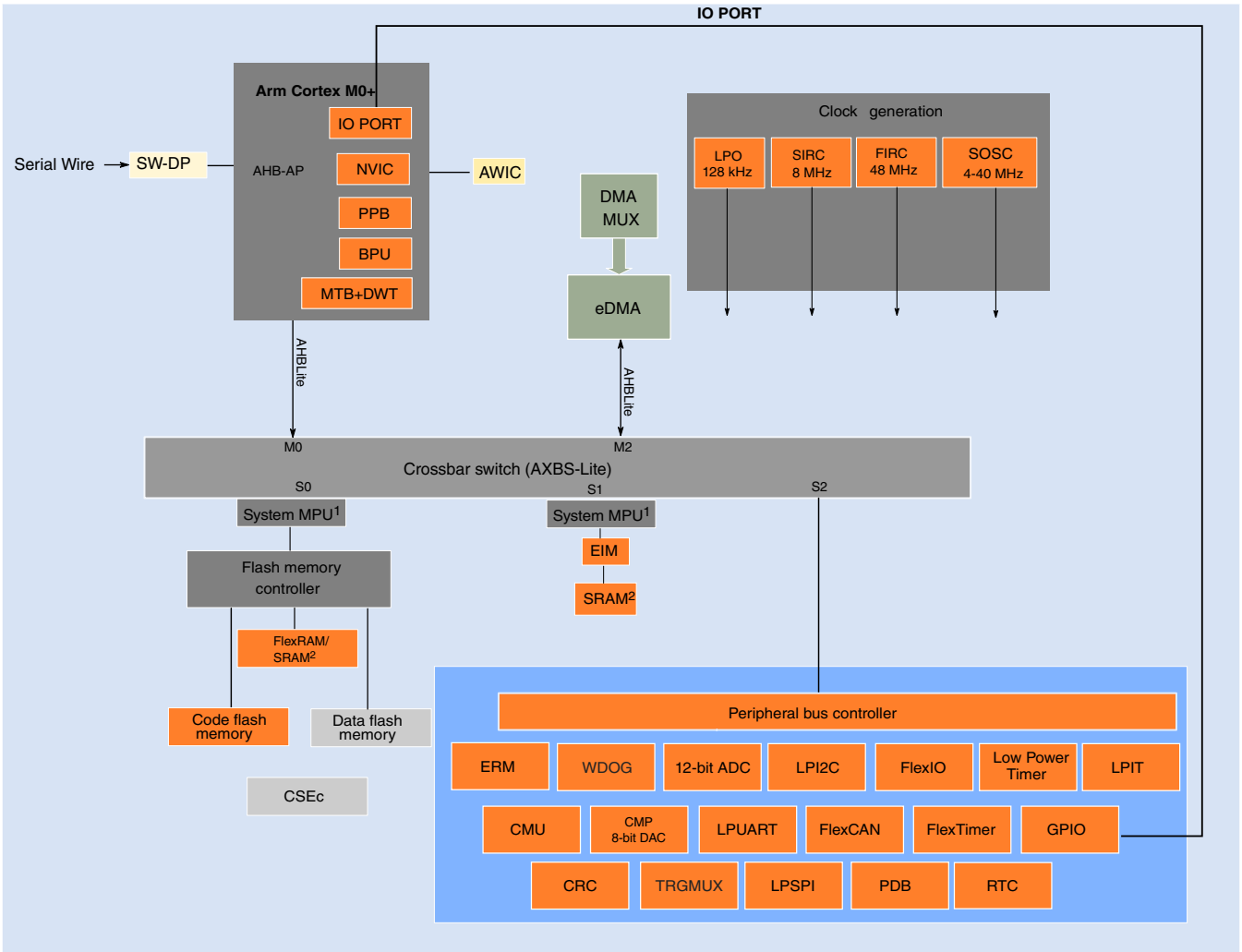
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0cllt



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The Arm M0+ core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

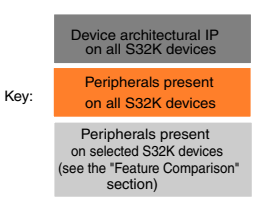


Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the S32K1xx devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

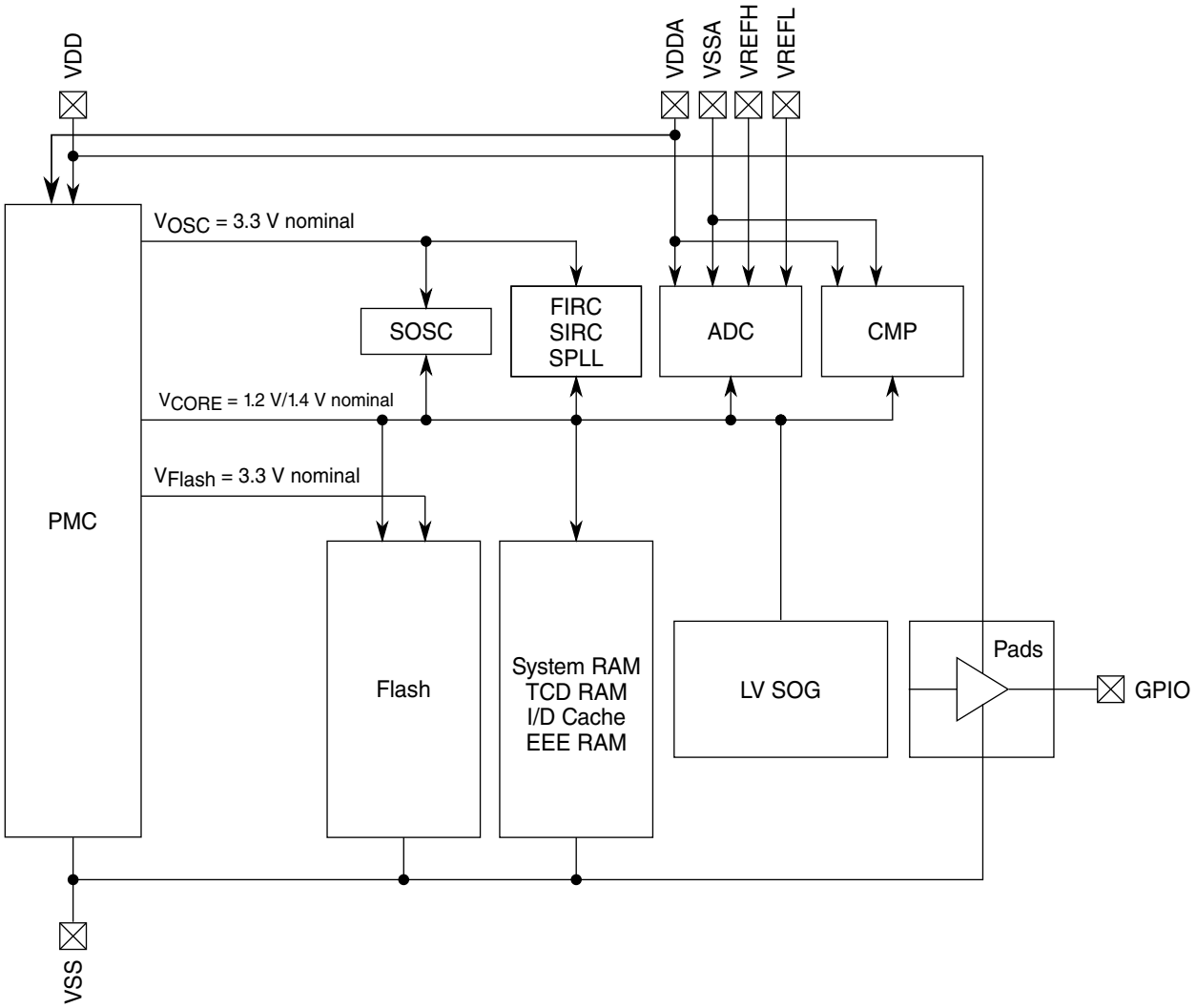
NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements 1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.



*Note: VSSA and VSS are shorted at package level

Figure 6. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1

Table continues on the next page...

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.1	5.7	6.5	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	3.5	3.8	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table Table 7. For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

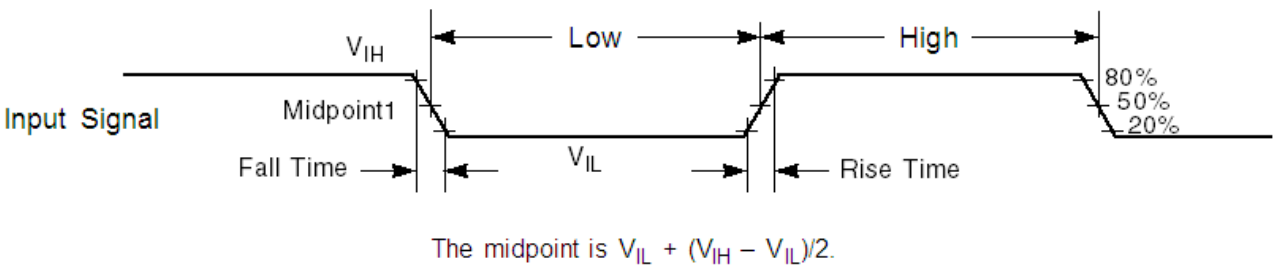


Figure 7. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be filtered by internal filter.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 11 and Table 12, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 11. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	14	—	—	mA	4
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	5
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [7]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

Table 16. Device clock specifications [1] (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

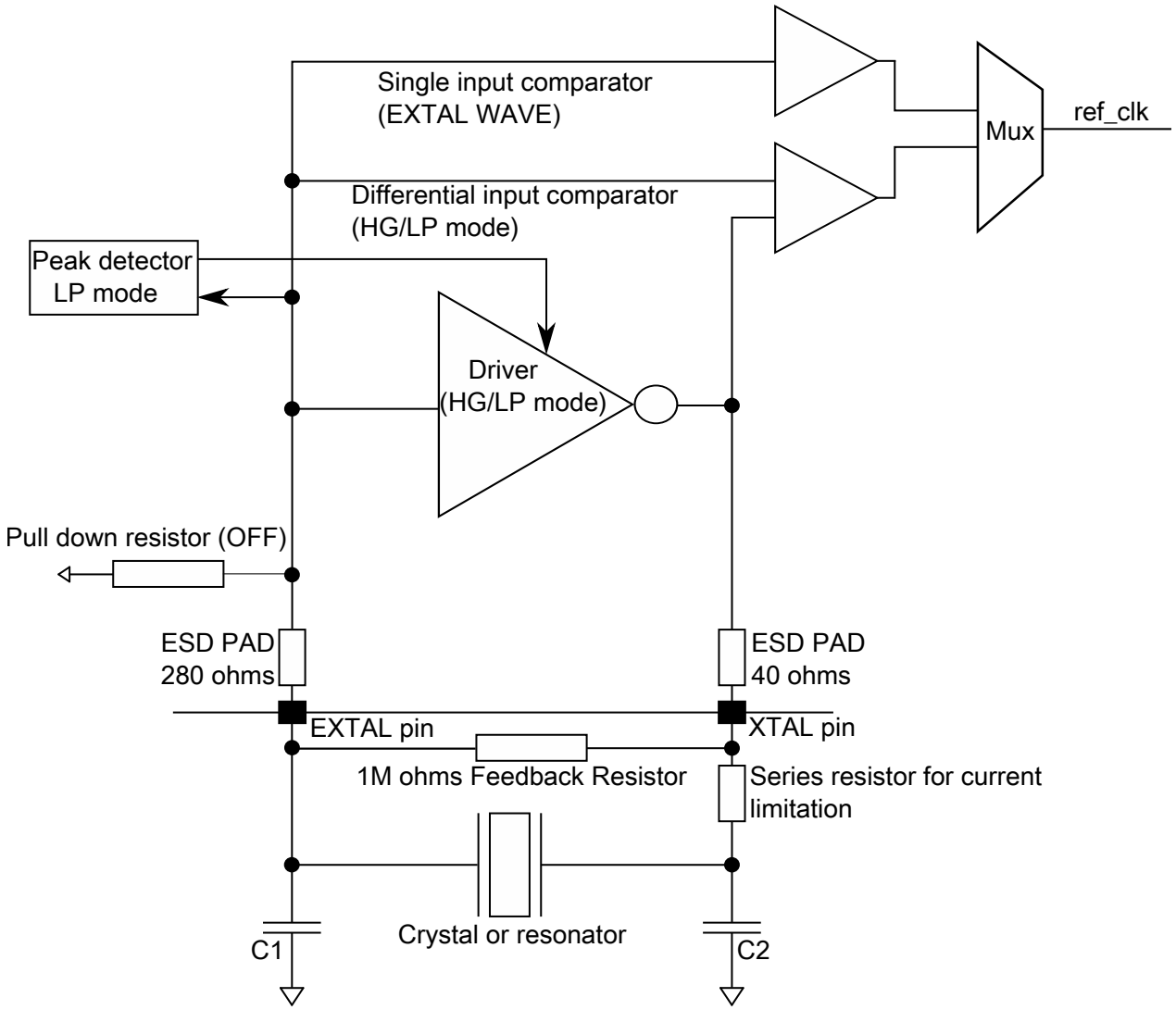


Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 21. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
$T_{startup}$	Startup Time	—	—	20	µs

6.2.5 SPLL electrical specifications

Table 22. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPLL_REF}[1]	PLL Reference Frequency Range	8	—	16	MHz
F_{SPLL_Input}[2]	PLL Input Frequency	8	—	40	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320	MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	120	—	ps
	at F_{VCO_CLK} 320 MHz	—	75	—	ps
J_{ACC_SPLL}	PLL accumulated jitter over 1µs (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	1350	—	ps
	at F_{VCO_CLK} 320 MHz	—	600	—	ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{SPLL_LOCK}	Lock detector detection time[4]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — commands

Table 23. Flash command timing specifications for S32K14x

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	—	2	—	—	—	—	—	—		
		512 KB flash	—	—	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	—	75	µs	
		4 KB flash	—	100	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	95	—	100	µs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	90	225	µs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	250	2125	—	—	—	—	—	—		
		512 KB flash	—	—	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	—	35	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	70	—	—	—	ms	3
		64 KB EEPROM backup	71	—	71	—	71	—	150	—		

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

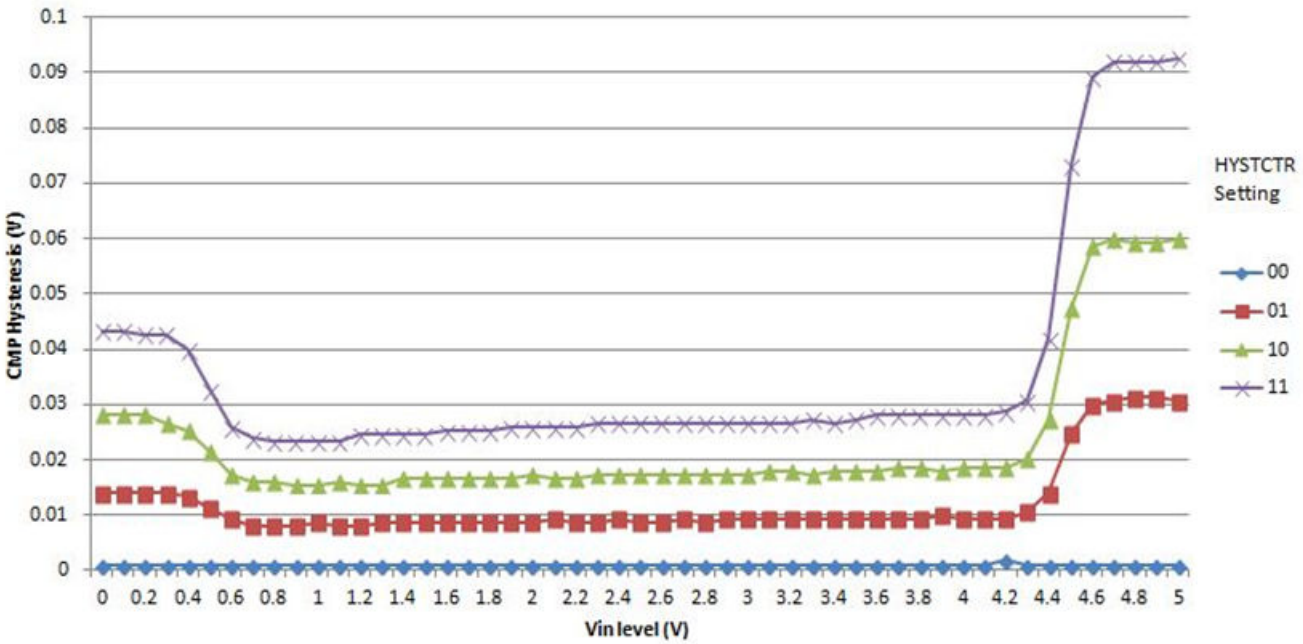


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

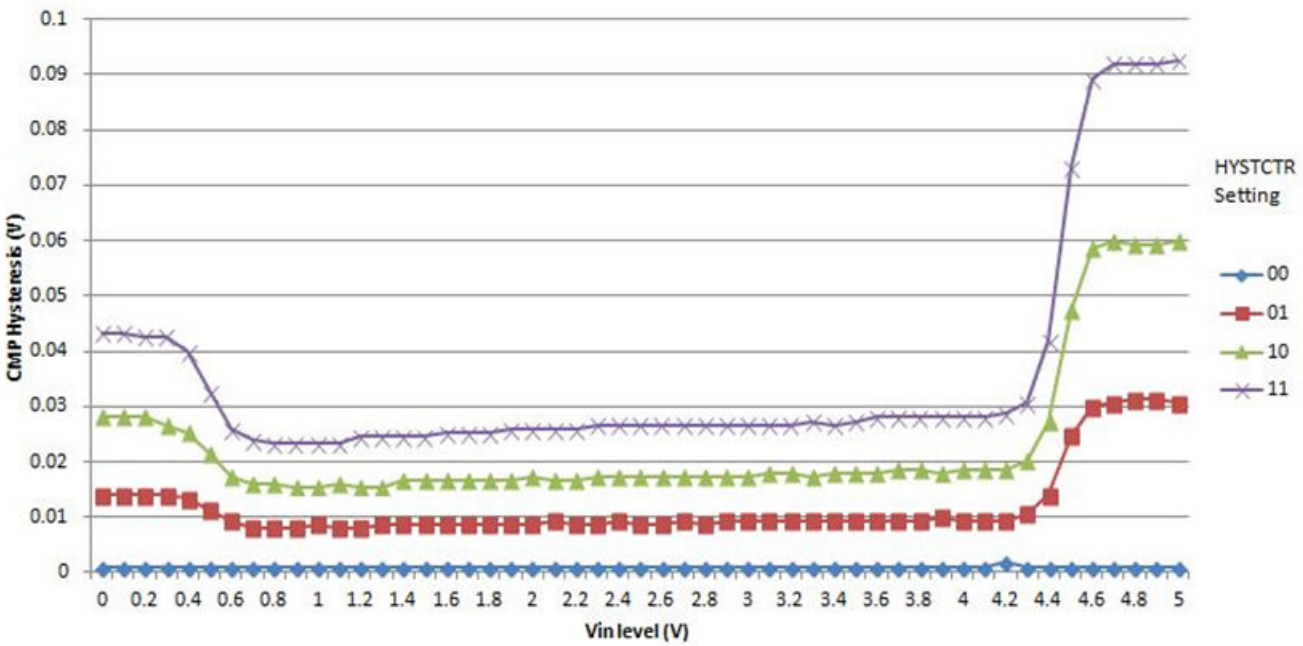


Figure 17. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 32. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph} [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14 [7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14 [7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													

Table continues on the next page...

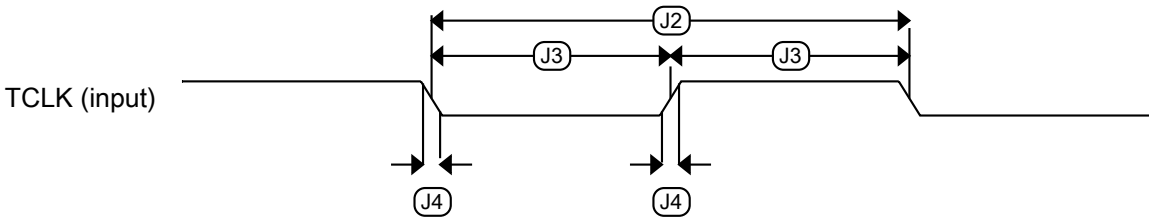


Figure 32. Test clock input timing

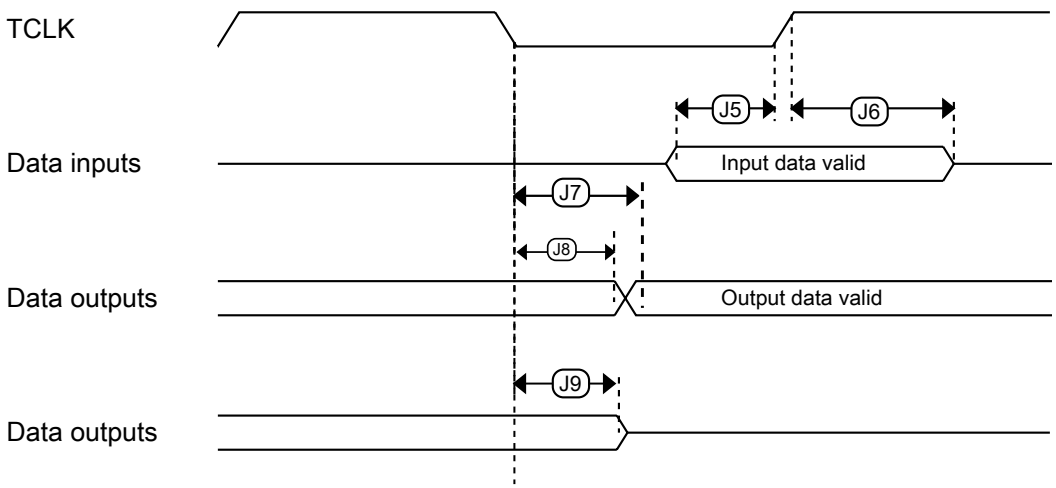


Figure 33. Boundary scan (JTAG) timing

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release

2	03 March 2017	• Updated descpition of QSPI and Clock interfaces in Key Features section
		• Updated figure: High-level architecture diagram for the S32K1xx family
		• Updated figure: S32K1xx product series comparison
		• Added note in section Selecting orderable part number
		• Updated figure: Ordering information
		• In table: Absolute maximum ratings :
		  • Added footnote to I_{INJPAD_DC}
		  • Updated min and max value of I_{INJPAD_DC}
		  • Updated description, max and min values for I_{INJSUM}
		  • Updated $V_{IN\_TRANSIENT}$
		• In table: Voltage and current operating requirements :
		  • Renamed V_{SUP_OFF}
		  • Updated max value of V_{DD_OFF}
		  • Removed V_{INA} and V_{IN}
		  • Added V_{REFH} and V_{REFL}
		  • Updated footnote "Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V ...
		  • Removed I_{NJSUM_AF}
		• Updated footnotes in table Table 4
		• Updated section Power mode transition operating behaviors
		• In table: Power consumption
		  • Added footnote "With PMC_REGSC[CLKBIASDIS] ... "
		  • Updated conditions for VLPR
		  • Removed Idd/MHz for S32K144
		  • Updated numbers for S32K142 and S32K148
		  • Removed use case footnotes
		• In section Modes configuration :
		  • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet'
		• In table: DC electrical specifications at 3.3 V Range :
		  • Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		  • Added footnote to High drive port pins
		• In table: DC electrical specifications at 5.0 V Range :

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